Application Note

OSPI Memory Interface Configuration

Version 1.0

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Overview

This app note covers details of configuring the OSPI and HSPI external memory interfaces in the Ensemble and Balletto families of devices.

The Alif Semiconductor Ensemble and Balletto families of devices provide high-speed address-mapped access to external memories via dedicated OSPI (8-bit/Octal SPI) and HSPI (16-bit/Hexadeca SPI) peripherals.

These interfaces enable Execute-in-Place (XIP) as well as memory-mapped read/write access to external memory devices such as:

- NOR Flash (read only)
- PSRAM (i.e., with array addressing)
- Xccela PSRAM
- HyperBus PSRAM (aka HyperRAM)

All Ensemble and Balletto devices support SDR (single data rate) and DDR (double data rate) modes of data sampling.

Maximum Interface Speed

The maximum speed of the interface varies depending on the family.

Device Family	Maximum Interface Speed
Ensemble E1, E3, E5, and E7	100 MHz
Ensemble E1C and Balletto B1	80 MHz
Ensemble E4, E6, and E8	200 MHz

All devices support DDR/DTR at maximum speed

Supported Features

SoC Family	Instances	Interface Width	PSRAM Support	Delay Calibration
Ensemble E4, E6, E8	2	16-bit	full	all signals
Ensemble E3, E5, E7	2	8-bit	partial	RXDS only
Ensemble E1	1	8-bit	partial	RXDS only
Ensemble E1C	1	8-bit	partial	RXDS only
Balletto B1	1	8-bit	partial	RXDS only

Note: 16-bit HSPI implicitly supports lower-width variants such as OSPI, QSPI, Dual, and standard SPI. Likewise, 8-bit OSPI will support all of the above except HSPI.

Note: Devices with partial PSRAM support cannot be used with array-addressable PSRAM memories (e.g., where column and row addresses are separated by a gap of one or more unused bits)

Memory Map – OSPI/HSPI Address Ranges

Ensemble E1, E3, E5, and E7 only:

Instance	Register Base Address	XIP Address Range
OSPI0	xSPI: `0x8300_0000` AES: `0x8300_1000`	`0xA000_0000` - `0xBFFF_FFFF`
OSPI1	xSPI: `0x8300_2000` AES: `0x8300_3000`	`0xC000_0000` - `0xDFFF_FFFF`

Note: Ensemble E1, E3, E5, and E7 devices implement manual SS control in XIP mode. The SSn pin asserted during the XIP transaction is selected in the OSPI registers.

Ensemble E4, E6, E8, E1C (OSPI0 only) and Balletto B1 (OSPI0 only):

Instance	Register Base Address	XIP SS0 Address Range	XIP SS1 Address Range
OSPI/HSPI0	xSPI: `0x8300_0000` AES: `0x8300_1000`	`0xA000_0000` - `0xAFFF_FFFF`	`0xB000_0000` - `0xBFFF_FFFF`
HSPI1	xSPI: `0x8300_2000` AES: `0x8300_3000`	`0xC000_0000` - `0xCFFF_FFFF`	`0xD000_0000` - `0xDFFF_FFFF`

Note: Ensemble E4, E6, E8, and E1C, as well as Balletto B1 devices, implement automatic SS control in XIP mode. The SSn pin asserted during the XIP transaction is selected based on bit 28 of the address being accessed. While this halves the address window from 512MB to 256MB for each memory device, it allows the application to use both SS0 and SS1 without the need to reconfigure the registers.

Note: If two memories sharing the same OSPI/HSPI bus are of different types, reconfiguring the registers is necessary when switching between SS0 and SS1.

Note: The actual usable size depends on the connected memory device.

Additionally, Ensemble E4, E6 and E8 devices provide aliases for HSPI0/1 to facilitate use of external memory as 'low memory' on Linux (i.e., ZONE_NORMAL). Accessing HSPI at these address ranges is only possible from A32 cores and from peripherals located in SYSTOP (e.g., DMA0, CPI...):

Instance	Aliased XIP SS0 Address Range	Aliased XIP SS1 Address Range
HSPI0	`0x2000_0000` - `0x23FF_FFFF`	`0x2400_0000` - `0x27FF_FFFF`
HSPI1	`0x2800_0000` - `0x2BFF_FFFF`	`0x2C00_0000` - `0x2FFF_FFFF`

Note: Accessing external memory through this alias limits maximum amount of addressable memory to 64MB per instance, per SSn pin.

XIP access and its restrictions

Support for Incrementing and Wrapping reads and writes

Compared to accessing internal on-chip memories (TCM, SRAM, MRAM), using address-mapped (XIP) accesses to the external memory comes with certain limitations.

Bus transactions may appear different, depending on which bus master is accessing the external memory. These accesses can be split into 3 main categories:

Access Type	Bus Master(s)	Details
32-byte Wrap	M55 cores with cache enabled	Cortex-M55 cache line is 32-bytes
64-byte Wrap	A32 cores with cache enabled	Cortex-A32 cache line is 64 bytes
Incrementing	All other bus masters	Some bus masters will still align the access to a specific boundary

While OSPI/HSPI peripherals allow applications to specify different instructions for incrementing access, many memories (e.g., NOR flashes) do not support it. Instead, the same read instruction is used, and access type is determined by the setting in the configuration register on the memory IC. Due to this limitation, some use cases will require additional configuration on the Alif SoC side to mitigate this:

Bus master(s)	Functionality	Required Configuration
M55s only	Full	32-byte Wrap
A32s only	Full	64-byte Wrap
U85/U55 only	Makes sense only without CPU-side runtime	Increment
M55 + U55/U85	M55 must disable cache, U55 can issue 128-byte bursts, U85 can issue 256-byte bursts	Increment
A32 + U55/U85	U55/U85 must limit burst size to 64 bytes	64-byte Wrap
A32 + M55	M55 must disable cache	64-byte Wrap
A32 + M55 + U85/U55	M55 must disable cache, U55/U85 must limit burst size to 64 bytes	64-byte Wrap
M55 + other	Other bus master's access must not cross 32-byte boundary	32-byte Wrap
A32 + other	Other bus master's access must not cross 64-byte boundary	64-byte Wrap
A32 + M55 + other	M55 must disable cache, other bus master's access must not cross 64-byte boundary	64-byte Wrap

Note: Some external memories support "hybrid wrap" access mode which will perform wrapping access on the first segment and subsequently continue incrementally on the next boundary. Using this mode will avoid the need to limit the size of U55/U85 bursts, and also allow other bus masters (e.g. DMA) to cross the 32/64-byte boundary when used in conjunction with M55 or A32.

For memory devices that do support use of different commands for wrapping and incrementing accesses (e.g. HyperRAM/HyperFlash, Xccela PSRAM), the only applicable restriction is such that M55 core(s) must disable the cache, if A32 core(s) are also accessing this external memory.

Bus traffic for XIP transactions

While debugging communication on the external bus, i.e. with a logic analyzer, certain patterns may be observed, pertaining to the bus master issuing the access and their configuration.

M55-HE and M55-HP cores both have a 64-bit bus and therefore they'll perform cache fills using 4-word 64-bit wrapping access (i.e. 64b WRAP4). The accesses will appear aligned on the 8-byte (64-bit) boundary, e.g. WRAP4 0x00, WRAP4 0x08, WRAP4 0x10 or WRAP4 0x18.

Similar phenomenon takes place with the A32 cores, albeit using 128-bit bus and 64-byte cache line (WRAP4 0x00, WRAP4 0x10, WRAP4 0x20 or WRAP4 0x30).

Subsequently, these bursts will be translated to 8-word 32-bit accesses, but the alignment of the original request is preserved. These are the accesses that can be seen directly on the OSPI/HSPI bus from A.

Conclusion

For further details on the OPSI/HSPI interfaces, please refer to the Hardware Reference Manual (HWRM) for the particular series (E8, B1, etc.) being used.

If you need help configuring your external memory interface, please file a technical support ticket at https://alifsemi.com/support/technical-support/

Document History

Version	Date	Change Log
1.0	Oct 30,2026	Initial public release