DATASHEET

ENSEMBLE™ FAMILY
E3 SERIES
EMBEDDED MICROCONTROLLERS

EXTREME LOW POWER MCU: DUAL CORTEX-M55 CPU w/HELIUM VECTOR EXT, DUAL ETHOS-U55 NPU, DEEP SECURITY, 2D GPU, MIPI-DSI/CSI, UP TO 13.5MB SRAM, UP TO 5.5MB MRAM

Features

High-Performance Dual-Core MCU

- High-Performance (HP) Arm® Cortex®-M55 Core, up to 400 MHz, with Helium™ Vector Processing Extension, Double-Precision FPU, 1.25MB SRAM 0-wait State Tightly- Coupled Memory, 32KB Instruction and Data Caches, Armv8.1-M ISA with Arm TrustZone®, and 4.37 CoreMark®/MHz Performance Benchmark
- High-Efficiency (HE) Arm® Cortex®-M55 Core, up to 160 MHz, with Helium™ Vector Processing Extension, Double-Precision FPU, 512KB of SRAM 0-wait State Tightly Coupled Memory, 32KB Instruction and Data Caches, Armv8.1-M ISA with Arm TrustZone®, and 4.37 CoreMark®/MHz Performance Benchmark
- High-Performance 400-MHz 64-bit AXI Bus Fabric Common Across All CPUs

Efficient Micro NPUs for ML/AI Acceleration

- 1× Arm Ethos-U55 NPU (NPU-HP), 256 MAC/cycle up to 400 MHz and 204 GOPS, Supporting RNN and CNN Networks
- 1× Ethos-U55 NPU (NPU-HE), 128 MAC/cycle up to 160 MHz and 46 GOPS, Supporting RNN and CNN Networks
- 800× Performance Uplift from Cortex-M4 for Inference Time (Source: Arm. MobileNet V2 1.0 Model for Object Classification)
- 76× Less Energy Consumed when Using Ethos-U55 Together with Cortex-M55 (Source: Arm. Measured on Alif Semiconductor Ensemble Device. MobileNet V2 1.0 Model for Object Classification)

Extreme-Low Power Technology

- Autonomous Intelligent Power Management (*ai*PM™)
- FD-SOI Low Leakage Process
- 1.7 µA Consumed in STOP Mode with LPRTC, LPTIMER, LPCMP, BOR, 4KB Utility SRAM, Wake Pins
- As Low as 29 µA/MHz Dynamic Consumption for High-Efficiency Cortex-M55
- Multiple Power Domains, Dynamic Power Gating, Voltage and Clock Scaling, DC-DC Converter

On-Chip Application Memory

- High Endurance MRAM Non-Volatile Memory
  - Up to 5.5MB
- SRAM
  - Up to 13.5MB
  - Optional Data Retention of 256KB or 512KB TCM SRAM Consuming 2.25 µA or 4.5 µA
  - 4KB Always-On Utility SRAM

External Memory Interfaces

- 2× Octal SPI, each at up to 100 MHz for up to 100 MB/s SDR, 200 MB/s DDR, with Inline AES Decryption, XIP Mode Support, HyperBus Protocol Support, Enabling External Memory Expansion
- 1× SD® v4.2, eMMC™ v5.1 Channel with DMA

Secure Enclave

- Hardware-based Root-of-Trust (RoT) with Unique Device ID
- Secure Key Generation and Storage, Secure Certificate Storage
- Factory-provisioned Private Keys
- Crypto Accelerators—AES (up to AES-256), ECC (up to 384 bits), SHA (up to SHA-256), RSA (up to RSA-3072), and NIST compliant TRNG
- Secure Debugging with Certificate Authentication

Timing Control and Measurement

- 12× Universal High-Resolution 32-bit Timers Capable of Motor and LED Lighting Control
- 2× Watchdog Timers
- 4× Low-Power 32-bit Timers
- 1× Real-Time Counter
- 4× Quadrature Encoder Counters

Serial Communication Interfaces

- 1× 10/100 Ethernet with DMA
- 1× USB 2.0 HS/FS Host/Device with DMA
- 1× SDIO v4.1 Channel with DMA
- 1× CAN FD Channel up to 10 Mbps
- 1× MIPI® I3C® Channel

- 4× I2C Channels up to 3.4 Mbps Throughput
- 1× Low-Power I2C Channel
- 8× UART Channels up to 2.5 Mbps (4× with RS-485 Driver Control)
- 1× Low-Power UART Channel
- 4× SPI Channels up to 50 Mbps Throughput
- 1× Low-Power SPI Channel

Analog Interface Capabilities

- 3× 12-bit SAR ADC (18 Single-Ended Inputs)
- 1× 24-bit Sigma-Delta ADC (4 Differential Inputs)
  - Programmable Gain Instrumentation Amplifier (1× to 128×)
- 2× 12-bit DACs (2 channels)
- 4× High-Speed Analog Comparators with 2.5-ns Response (16 Inputs)
- 1× Low-Power Analog Comparator (4 Inputs)
- Internal Temperature Sensor
- Internal Precision Reference Voltage

Camera Interfaces

- 1× 2-Lane MIPI CSI-2®
- 1× Camera Parallel Interface (CPI), up to 16 bits
- 1× Low-Power CPI, up to 8 bits

Display Interfaces

- Graphics LCD Controller
- 1× Display Parallel Interface (DPI), up to 24-bit RGB
- 1× 2-Lane MIPI D-PHY DSI

Graphics

- D/AVE 2D Graphics Processing Unit

Audio Interfaces

- 4× I2S Synchronous Stereo Audio Interfaces
- 1× Low-Power I2S Stereo Audio Interface
- 4× 2-channel Pulse Density Modulation (PDM) Microphone Inputs (8 Mono Microphones)
- 4× 2-channel Low-Power Pulse Density Modulation (LPPDM) Microphone Inputs (8 Mono Microphones)

General Input/Output

- Up to 120× 1.8-V GPIOs (Shared with Peripherals)
- Up to 8× Selectable 1.8-V to 3.3-V GPIOs (Shared with Peripherals)

Clock Generation

- LFRC - Internal Low-Frequency RC Oscillator (32.7 kHz, ±4%)
- HFRC - Internal High-Frequency RC Oscillator (Up to 76.8 MHz, ±2%)
- LFXO - External Low-Power Crystal Oscillator or Quartz Crystal (32.768 kHz)
- HFXO - External High-Frequency Crystal Oscillator or Quartz Crystal (24 MHz to 38.4 MHz)
- One User Fractional Mode PLL

System

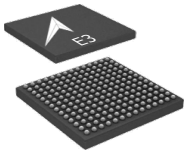
- Global Event Mapping to Configurable Triggers
- 3× 32-Channel General DMA Controllers
- CRC Calculation Accelerator with Programmable Polynomials
- Programmable Low Supply Voltage Detect Warning (Brown-Out Detect)
- Power-On Reset and Brown Out Reset
- Real-Time Clock
- JTAG/SWD Debug Interface

Operating Parameters

- 1.75 V to 4.2 V Primary Supply Range
- 1.08 V to 1.98 V I/O Supply Range (1.8 V I/O)
- 3.0 V to 4.2 V I/O Supply Range (3.3 V Flex I/O)
- -40 °C to 85 °C Extended Ambient Temperature Range
- -40 °C to 125 °C Extended Junction Temperature Range

Packages

- WLCSP208, 0.5 mm Pitch
- FBGA194, 0.5 mm Pitch



WLCSP

FBGA

1 Preface

This document contains fundamental technical information for the Alif Semiconductor E3 series devices.

Device information herein includes features description, electrical and mechanical characteristics with specifications, and ordering information.

There are references to third-party technical documents as noted within this document.

For more information on processors, peripheral functions, and programming settings, refer to the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

2 Device Overview

2.1 Device Description

The families of fusion processors and microcontrollers (MCUs) from Alif Semiconductor create a scalable and compatible continuum of highly integrated embedded processor devices for use in low-end to high-end intelligent IoT end-point applications. Architected for power efficiency and long battery life, these devices deliver high computation and ML/AI capability, multi-layered security, computer vision, and highly interactive human-machine interface.

Individual device selections within a family of devices scale up starting with single-core MCUs, dual-core MCUs, triple-core MCU/MPU fusion processors, and quad-core MCU/MPU fusion processors to match specific applications. Across all devices are common peripherals, common power management schemes, and a common interconnection fabric making it easy to re-use software and hardware over many varied projects.

This document covers the dual-core E3 embedded microcontrollers from the Ensemble™ family.

Power efficiency—In addition to the use of FD-SOI silicon process technology, *ai*PM provides fine granular control over the processing, memory, and peripheral resources of the device, resulting in extreme power conservation that consumes only what is needed, when its needed, at any given instant based on use case.

Computation and ML/AI—Dual-core design with two Arm Cortex-M55 Real-Time cores, with one Real-Time core optimized for extreme low power operation. Machine Learning and AI tasks are accelerated by dual Arm Ethos-U55 neural processing units generating as much as 250 GOPS. E3 devices can operate with an RTOS, while using only the on-chip memory resources. Additional RAM or Flash memory may be accessed externally through two high-speed Octal SPI interfaces supporting XIP mode and HyperBus protocol. An in-line AES decryption module in each Octal SPI interface ensures the confidentiality of the data and/or code stored in the external memory devices.

Connectivity—E3 devices support many wired interfaces including Ethernet, USB, SDIO, CANFD, I3C, I2C, and more.

Security—An isolated Secure Enclave manages the entire life cycle of the end application from manufacture, to deployment, to secure Firmware Over-The-Air updates, and to retirement. A unique Root-of-Trust existing in the enclave enables a trusted on-chip platform for key generation, secure storage, secure boot, cryptographic acceleration, and more. The Secure Enclave also enables certificate-based secure debugging.

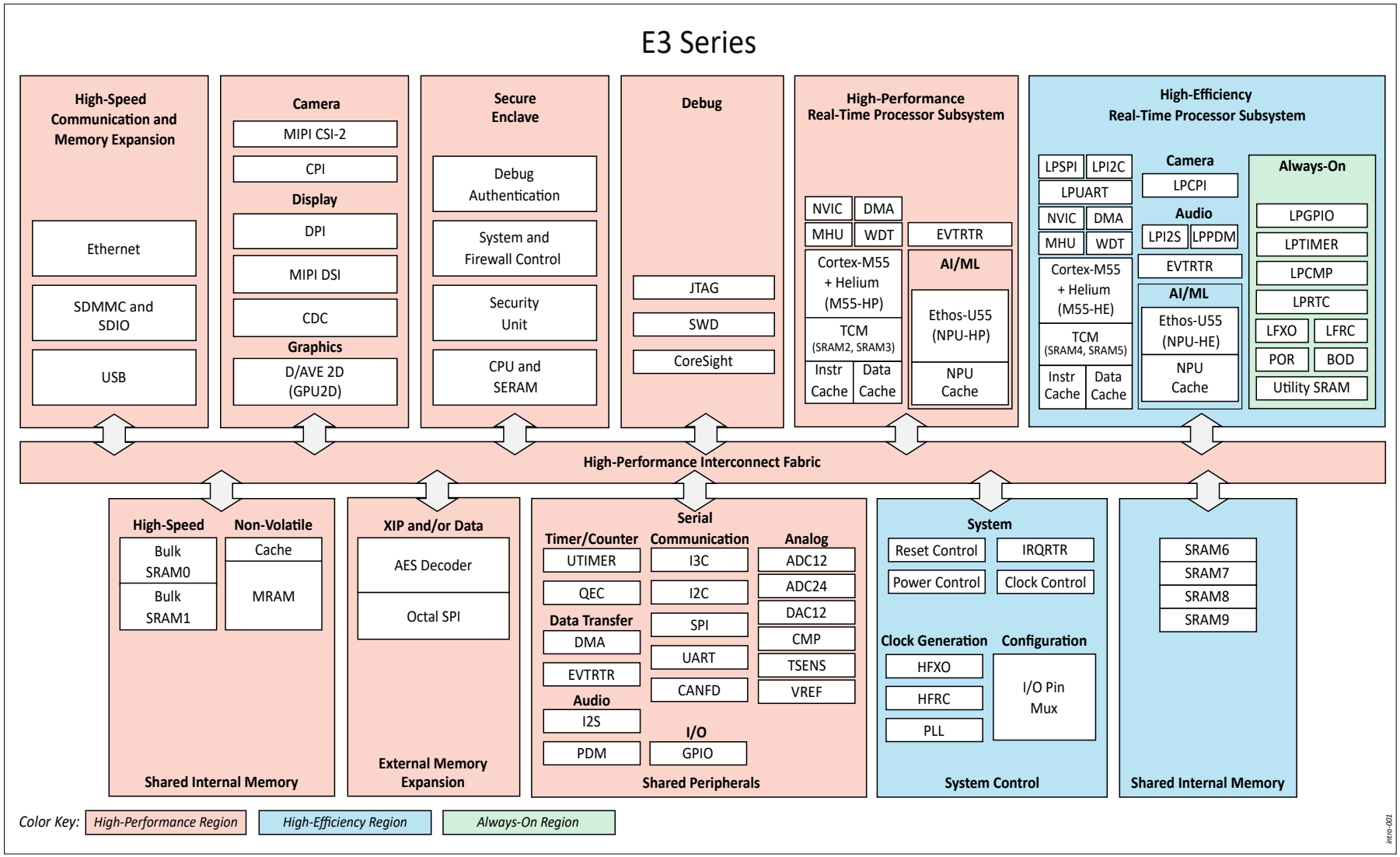
Computer Vision—Integrated camera interfaces, including MIPI CSI-2, enable easy connection of low-power image sensors for AI image classification using the Arm Ethos-U55 NPUs. Biometric ID, face detection, object classification, barcode reading, and other vision applications can execute while consuming very little energy.

Human Machine Interface—Integrated color display interfaces, including MIPI DSI, can drive a wide range of display panels with vivid graphics supported by the on-chip 2D graphics processing unit for attractive user interfaces. Digital audio inputs and outputs are supported by PDM and I2S interfaces. The Arm Ethos-U55 NPUs can apply ML inference to audio input streams for key word spotting, speech recognition, failure prediction, and more.

2.2 Device Block Diagram

Figure 2-1 presents a simplified diagram of the operating regions and main internal components of the Alif Semiconductor E3 Series of devices.

Figure 2-1 Device Block Diagram



2.3 Device Features Summary and Comparison

Table 2-1 presents device features supported and package options.

Table 2-1 Device Features and Peripherals

Feature		Definition
Package options		WLCSP208, FBGA194
Processors and Accelerators		
High-Performance Arm Cortex-M55	M55-HP	Up to 400 MHz
High-Efficiency Arm Cortex-M55	M55-HE	Up to 160 MHz
Arm Ethos-U55 Neural Processing Units	NPU-HP	Optional (3) Up to 204 GOPS
	NPU-HE	Up to 46 GOPS
D/AVE 2D Graphics Processing Unit	GPU2D	Yes
Security Subsystem		
Secure Enclave	SE	Yes
Memory		
On-Chip Non-volatile Application Memory	MRAM	Optional (3) Up to 5.5MB
On-Chip Application SRAM	SRAM	Optional (3) Up to 13.5MB
Timers and Counters		
Low-Power Timer	LPTIMER (2)	4 × 32-bit
Universal Timer	UTIMER	12 × 32-bit
Watchdog Timer	WDT	2
Quadrature Encoder Counter	QEC	4
Low-Power Real-Time Counter	LPRTC (2)	1
General Input and Output		
General Purpose I/O pins	GPIO	120 (1.8 V)
Low-Power General Purpose I/O pins	LPGPIO (2)	8 (1.8 V to 3.3 V)
Communication Peripherals		
Controller Area Network	CANFD	Optional (3)
Ethernet 10/100 Controller	ETH	1
Inter-Integrated Circuit	I2C	4
	LPI2C (2)	1
Inter-IC Sound	I2S	4
	LPI2S (2)	1
MIPI Improved Inter-Integrated Circuit	I3C	1
Pulse Density Modulation	PDM	4× 2-channel
	LPPDM (2)	4× 2-channel

Feature		Definition
Serial Peripheral Interface	SPI	4
	LPSPI (2)	1
Universal Asynchronous Receiver/Transmitter	UART	8
	LPUART (2)	1
Universal Serial Bus	USB	USB 2.0 HS/FS Host/Device
Secure Digital Input Output	SDIO	SDIO v4.1 (1)
External Memory Interfaces		
Octal SPI	OSPI	2
Secure Digital Multimedia Card	SDMMC	SD v4.2, eMMC v5.1 (1)
Camera Subsystem		
Camera Parallel Interface	CPI	Up to 16-bit
	LPCPI (2)	Up to 8-bit
MIPI Camera Serial Interface 2	CSI	2-Lane
Display Subsystem		
Graphics LCD Controller	CDC	1
Display Parallel Interface	DPI	Up to 24-bit RGB
MIPI Display Serial Interface	DSI	2-Lane
Analog Peripherals		
Analog-to-Digital Converter	ADC12	3 × 12-bit (Up to 18 inputs)
	ADC24	1 × 24-bit (Up to 4 differential inputs)
Digital-to-Analog Converter	DAC12	2 × 12-bit
High-Speed Comparator	CMP	4 (16 inputs)
Low Power Comparator	LPCMP (2)	1 (4 inputs)
Temperature Sensor	TSENS	Yes

1. SDIO, SD, and eMMC are functions of memory card controller. There is only one memory card controller in the device.
2. All Low Power (LP) peripherals are single-master accessible. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.
3. For devices supporting optional features, see Section 7 Ordering Information.

3 Functional Overview

3.1 Real-Time Processor

3.1.1 M55-HP Overview

The Cortex-M55 High-Performance (M55-HP) processor implements the Armv8.1-M Mainline architecture that includes support for the M-profile Vector Extension (MVE), also known as Helium™. The M55-HP achieves high compute performance across scalar and vector operations, operating up to 400 MHz.

The device includes a single M55-HP processor that resides in the High-Performance Real-Time Subsystem (RTSS-HP). The RTSS-HP also includes various memories and peripherals.

The M55-HP processor supports the following main features:

- CPU revision: r1p0
- CPU core logic that includes:
  - In-order, four-stage integer pipeline with early completion of common arithmetic instructions
  - Instruction Fetch Unit (IFU) with 32-bit instruction fetch data width
  - Data Processing Unit (DPU) with 64-bit load/store data width
  - Support for up to 2 × 32-bit vector load operations in parallel
- Extension Processing Unit (EPU) that works closely with the CPU core to support:
  - Scalar floating-point (VFPv5) operations: half-, single-, and double-precision
  - Vectored operations through MVE (Helium):
    - Integer
    - 128-bit SIMD floating-point: half- and single-precision
- Double-Precision FPU
- Support for other Extensions such as:
  - Armv8.1-M Main Extension (16-bit and 32-bit Thumb® instruction set)
  - Armv8-M Security Extension (TrustZone)
  - DSP Extension
  - DSP Debug Extension
  - Reliability, Availability, and Serviceability (RAS) Extension
  - Unprivileged Debug Extension (UDE)
- Memory architecture that includes:
  - Memory Authentication Unit (MAU) for memory access control:
    - Secure Memory Protection Unit (MPU) supporting 16 regions
    - Non-secure MPU supporting 16 regions
    - Security Attribution Unit (SAU) supporting 8 regions
    - TCM Gate Units (TGU):
      - Instruction TGU (ITGU) protecting 16 address regions, each 16KB in size
      - Data TGU (DTGU) protecting 64 address regions, each 16KB in size
  - Memory system:
    - 32KB L1 Instruction Cache (IRAM)
    - 32KB L1 Data Cache (DRAM)
    - 256KB Instruction TCM (ITCM); access to ITCM is over a single interface
    - 1024KB Data TCM (DTCM); access to DTCM is over four interfaces
    - Master AXI (M-AXI) interface for high latency memory or peripheral access

- Interrupt control:
  - Nested Vectored Interrupt Controller (NVIC) for low-latency interrupt processing:
    - Supports 480 external interrupts, with 256 priority levels per interrupt
  - Wakeup interrupt control to allow the processor to enter low-power state:
    - Internal Wakeup Interrupt Controller (IWIC)
    - External Wakeup Interrupt Controller (EWIC)
- Secure and non-secure Vector Table Offset Register (VTOR)
- Debug and trace support:
  - Full set debug:
    - Breakpoint Unit (BPU) with 8 comparators
    - Data Watchpoint and Trace (DWT) unit with 4 comparators and Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - CoreSight-compliant Debug Access Port (DAP):
    - Supports dynamic switching—Serial Wire / JTAG Debug Port (SWJ-DP)

3.1.2 M55-HE Overview

The Cortex-M55 High-Efficiency (M55-HE) processor implements the Armv8.1-M Mainline architecture that includes support for the M-profile Vector Extension (MVE), also known as Helium™. The M55-HE achieves high compute efficiency across scalar and vector operations, operating up to 160 MHz.

The M55-HE memories are based on ultra-low leakage memory cells which results in low power consumption in sleep mode. The choice of TCM retention allows application-optimized tradeoff between current leakage during sleep and fast wake-up time.

The device includes a single M55-HE processor that resides in the High-Efficiency Real-Time Subsystem (RTSS-HE). The RTSS-HE also includes various memories and peripherals.

The M55-HE processor supports the following main features:

- CPU revision: r1p0
- CPU core logic that includes:
  - In-order, four-stage integer pipeline with early completion of common arithmetic instructions
  - Instruction Fetch Unit (IFU) with 32-bit instruction fetch data width
  - Data Processing Unit (DPU) with 64-bit load/store data width
  - Support for up to 2 × 32-bit vector load operations in parallel
- Extension Processing Unit (EPU) that works closely with the CPU core to support:
  - Scalar floating-point (VFPv5) operations: half-, single-, and double-precision
  - Vectored operations through MVE (Helium)
    - Integer
    - 128-bit SIMD floating-point: half- and single-precision
- Double-Precision FPU
- Support for other Extensions such as:
  - Armv8.1-M Main Extension (16-bit and 32-bit Thumb instruction set)
  - Armv8-M Security Extension (TrustZone)
  - DSP Extension
  - DSP Debug Extension
  - Reliability, Availability, and Serviceability (RAS) Extension
  - Unprivileged Debug Extension (UDE)

- Memory architecture that includes:
  - Memory Authentication Unit (MAU) for memory access control:
    - Secure Memory Protection Unit (MPU) supporting 16 regions
    - Non-secure MPU supporting 16 regions
    - Security Attribution Unit (SAU) supporting 8 regions
    - TCM Gate Units (TGU):
      - Instruction TGU (ITGU) protecting 16 address regions, each 16KB in size
      - Data TGU (DTGU) protecting 16 address regions, each 16KB in size
  - Memory system:
    - 32KB L1 Instruction Cache (IRAM)
    - 32KB L1 Data Cache (DRAM)
    - 256KB Instruction TCM (ITCM); access to ITCM is over a single interface
    - 256KB Data TCM (DTCM); access to DTCM is over four interfaces
    - Master AXI (M-AXI) interface for high latency memory or peripheral access
- Interrupt control:
  - Nested Vectored Interrupt Controller (NVIC) for low-latency interrupt processing:
    - Supports 480 external interrupts, with 256 priority levels per interrupt
  - Wakeup interrupt control to allow the processor to enter low-power state:
    - Internal Wakeup Interrupt Controller (IWIC)
    - External Wakeup Interrupt Controller (EWIC)
- Secure and non-secure Vector Table Offset Register (VTOR)
- Debug and trace support:
  - Full set debug:
    - Breakpoint Unit (BPU) with 8 comparators
    - Data Watchpoint and Trace (DWT) unit with 4 comparators and Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - CoreSight-compliant Debug Access Port (DAP):
    - Supports dynamic switching—Serial Wire / JTAG Debug Port (SWJ-DP)

3.2 Neural Processing Unit (NPU)

The Arm Ethos-U55 Neural Processing Unit (NPU) is a Machine Learning (ML) coprocessor that improves the inference performance of neural networks (NN).

The NPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN). The NPU includes a Direct Memory Access (DMA) controller that can read and write to external memory. The DMA controller reads the neural network description and transfers the input and output feature maps.

The device includes:

- Up to one NPU coprocessor in the device High-Performance Region—NPU-HP
- One NPU coprocessor in the device High-Efficiency Region—NPU-HE

3.2.1 NPU-HP Overview

The NPU-HP supports the following main features:

- Up to 204 GOPS performance using up to 256 MAC/cycle
- Network support: CNN, RNN
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)

- Activation functions:
  - ReLU, ReLU1, ReLU6, and Leaky ReLU (LReLU)
  - Tanh
  - Sigmoid
  - Configurable Look-Up Table (LUT)
  - None or bypass
- Element-wise operations:
  - Element-wise ADD and SUB
  - Element-wise Multiplication (MUL)
  - Element-wise Min and Max
  - Element-wise ABS
  - Element-wise Shift Left (SHL) and Shift Right (SHR)
  - Element-wise Count-Leading Zero (CLZ)
- 48KB of internal shared cache memory (SHRAM)
- Integrated DMA controller
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

3.2.2 NPU-HE Overview

The NPU-HE supports the following main features:

- Up to 46 GOPS performance using up to 128 MAC/cycle
- Network support: CNN, RNN
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)
- Activation functions:
  - ReLU, ReLU1, ReLU6, and Leaky ReLU (LReLU)
  - Tanh
  - Sigmoid
  - Configurable Look-Up Table (LUT)
  - None or bypass
- Element-wise operations:
  - Element-wise ADD and SUB
  - Element-wise Multiplication (MUL)
  - Element-wise Min and Max
  - Element-wise ABS
  - Element-wise Shift Left (SHL) and Shift Right (SHR)
  - Element-wise Count-Leading Zero (CLZ)
- 24KB of internal shared cache memory (SHRAM)
- Integrated DMA controller
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

3.3 2D-Graphics Accelerator (GPU)

The D/AVE 2D Graphics Processing Unit (GPU2D) provides hardware acceleration for sophisticated vector-based graphical applications.

The device includes one GPU2D module.

The GPU2D supports the following main features:

- Subpixel accurate rendering
- Resolutions of up to 2048 × 2048 pixels

- Operating clock frequency at 400 MHz. GPU render pipeline produces one pixel per clock cycle.
- 16 blending modes
- Patterns and gradients with alpha channel on all primitives
- Render to texture
- Textures up to 2048 × 1024 pixels
- Texture blending
- Bilinear filtering
- Graphical primitives available:
  - Block Image Transfers (BLIT)—direct and stretch
  - Box
  - Circle—filled or empty (ring)
  - Convex polygon
  - Line
    - Supported caps:
      - Butt
      - Round
      - Square
    - Supported line joins:
      - Bevel
      - Miter
      - Round
    - Supporting different start and end widths
  - Quad
  - Triangle
  - Triangle fan
  - Triangle list
  - Triangle stripe
  - Wedge-filled or empty
- Graphical primitives attributes:
  - Anti-aliasing
  - Blend modes
  - Color
  - Edge blur
  - Linear alpha gradient
  - Pattern
  - Texture
    - U/V clamp, repeat support
    - No-, linear-, bilinear-filtering support
    - Run-Length Encoding (RLE)
- Supported color coding formats:
  - Input
    - ARGB8888, RGB565, ARGB4444, ARGB1555, ALPHA8, AI44, RGBA8888, RGBA4444, RGBA5551, I8, I4, I2, I1, ALPHA4, ALPHA2, ALPHA1
  - Output
    - ARGB8888, RGB565, ARGB4444, ALPHA8, RGBA8888, RGBA4444

3.4 Secure Enclave Subsystem (SESS)

3.4.1 Security Architecture Overview

The device contains an advanced Secure Enclave (SE) that is responsible for managing the device security. The SE is an isolated subsystem with its own dedicated resources. The isolated subsystem reduces the attack surface for the SE along with the minimal software interfaces that are restricted to the Inter-Process Communication (IPC) Message Handling Units (MHUs).

The SE boots first on Power-On-Reset (cold start). It runs the First Stage bootloader code from a private, immutable ROM. The SE performs certificate-based integrity and authenticity check on the Second Stage bootloader. It is loaded to the SE SRAM (SERAM) and the flow of execution is transferred to it. This mechanism enables the secure update of the Second Stage bootloader on the field. The boot process continues with processing of the application-specific device configuration. The SE applies configuration settings that partition the system resources (memory and peripherals) between the different application cores. Next, the SE bootloader performs a signature verification of the installed application binaries. If needed, it copies the specified binaries to their designated SRAM regions. Finally, a designated core is released from Reset to run its application. This completes the secure boot procedure. The remaining cores can be booted by the SE in response to a service request.

The SE is also involved in the process of waking up from STOP mode. When a wakeup event is triggered, the SE CPU boots first. It checks if the SERAM is retained and continues the execution flow there. The SERAM code maps the wakeup event to an application core and promptly boots it. If the SERAM is not retained, then the SE validates the wakeup source and boots the RTSS-HE core. The retention of SERAM in the Secure Enclave or the SRAM (M55-HE TCM) in the RTSS-HE offers trade-off options between the leakage current and the wakeup time of the device.

The SE provides traditional security functions such as:

- Secure boot
- Secure device configuration
- HW Root-of-Trust (RoT)
- Key management
- Signature validation
- Crypto operations
- Life cycle management

The Supervisor is responsible to:

- Manage the OEM provisioning process and the Life Cycle State (LCS)
- Apply the system configuration settings to the security firewalls and security HW in the system
- Securely boot the Real-time cores (M55-HP and M55-HE) as defined by the user's configuration file

3.4.2 Cryptographic Services

The Secure Enclave (SE) supports a variety of Runtime Security and Cryptographic services that enable the OEM’s application code to control security functions for the device and request cryptographic operations. These runtime services make use of IPC.

The Runtime Cryptographic services include the ability of the OEM application code to make requests for standard and device-specific cryptographic operations like:

- Creating keys
- Using the keys to encrypt or decrypt
- Return the device certificate

- Authenticate the device
- Validate the signature of images against the provisioned keys in the device
- Secure boot a core
- Write to MRAM memory
- Process Alif Semiconductor's firmware updates

3.5 Interconnect

The system interconnect provides the means of connecting bus masters (CPU cores, DMA controllers) to memory modules and peripherals. It is based on the Arm AMBA bus architecture utilizing a mix of AXI, AHB and APB buses.

The backbone of the device interconnect is based on an AXI4 bus, featuring multiple master and slave ports. The processing subsystems have their own local buses connected as masters to the main AXI bus. The memory blocks and the peripheral subsystems connect as slaves to the main AXI bus. Some peripherals (such as ETH, SDMMC, and USB) also can act as bus masters and connect via both master and slave ports. The master ports serve their DMA controllers to transfer data without CPU intervention, while the slave ports are intended for accessing their registers.

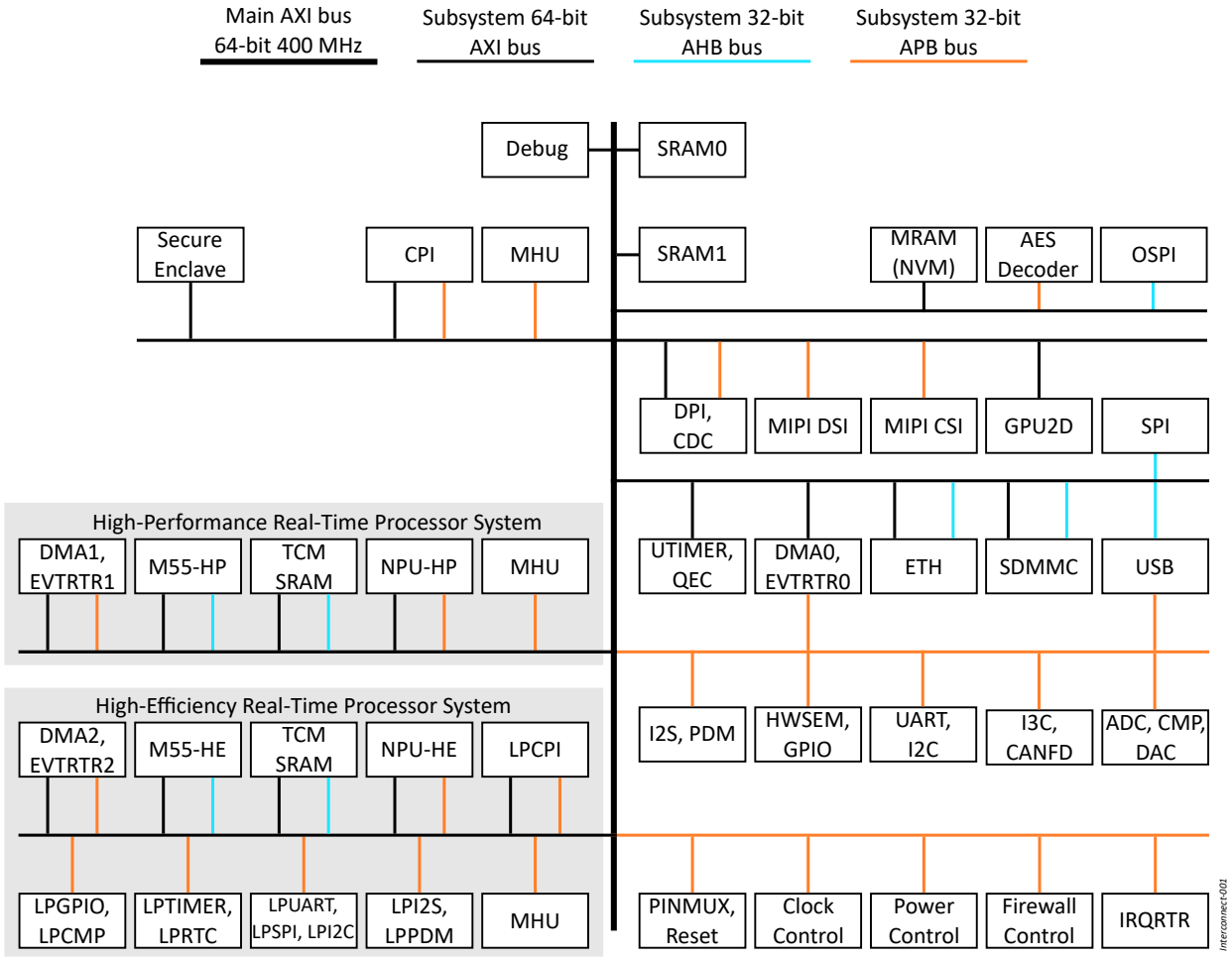
Each master and slave port connects to the main AXI bus through Firewall Components (FC). They enforce run-time configurable access rights policy and address translation. Transaction gating is based on master ID, transaction type (instruction or data fetch) and TrustZone-defined secure world context. The FC configuration settings are set by the SE during the secure boot process. The applications specify their desired access paths and address regions in a dedicated region of the on-chip Non-Volatile Memory (NVM), which is MRAM. The SE applies these settings during the device boot process.

The device interconnect supports the following main features:

- High-performance AXI4 bus protocol
- 64-bit wide read and write data paths
- 400 MHz bus clock frequency
- Burst-based transactions for optimizing bandwidth efficiency
- TrustZone aware
- Firewall controller and 14 firewall components to enforce secure policy constraining the bus master's access to the device resources
- Firewall security monitoring function raising an interrupt when unauthorized access is attempted

Figure 3-1 provides a high-level overview of the system interconnect implementation in the device.

Figure 3-1 Interconnect Overview



NOTE

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

3.6 Power Supply Management

The device has three operating regions that encapsulate top-level functions from a power consumption perspective:

- **Always-On (AON) Region**—a group of rudimentary functions that are always powered when a constant power source is connected to the VDD_BATT pin.
- **High-Efficiency (HE) Region**—a group of compute, sensing, AI functions designed to operate at the highest efficiency. Many tasks can be performed in this region to conserve power and/or extend battery life before waking up the HP Region.
- **High-Performance (HP) Region**—a group of compute, AI, Human-Machine Interface (HMI), and high-speed connectivity functions designed to operate at maximum performance. These functions are invoked only as required to conserve energy.

The device block diagram (see Figure 2-1) illustrates these three operating regions and the functions available within each of the regions.

A smart power management scheme named *ai*PM (autonomous intelligent Power Management) utilizes a hierarchy of multiple power domains, multiple internal voltage supplies, and multiple power modes to power on, in fine granularity, portions of the device only when they are needed based on use case, and off when not needed. Powering on and off portions of the device occurs automatically in hardware as required, but the power management policies are configured by software.

Multiple power domains—There are nine independent power domains in the device, each one with a dedicated power controller that is coordinated by digital logic and software configuration for automatic transitions—from power-up to full GO mode, and all modes in between. This scheme achieves optimum power efficiency based on the dynamic power demand of the device at any given moment in time.

Multiple voltage supplies—There are internal device voltage supplies consisting of a series of Low Drop-Out (LDO) regulators and a dual-mode DC-to-DC buck converter (DC-DC) to generate 0.55 V, 0.8 V, and 1.8 V internal voltage rails that are automatically switched on and off as required for optimum performance and efficiency.

Multiple power modes—Below are top-level device modes listed from highest to lowest power consumption:

- GO—any or all processing cores operate up to their max frequency
- READY—all processing cores are clock gated off, but peripherals can run
- IDLE—all processing cores are powered off, but some peripherals can run
- STANDBY—all processing cores are powered off, but a few low-power peripherals can run
- STOP—entire device is powered off except the AON Region where rudimentary low-power peripherals and wake-up sources are active, as well as optional retained SRAM blocks

3.6.1 Power Domains

The device Power Domains (PD) are managed by a Power Sequence Controller (PSC) and several Power Policy Units (PPU). The PSC is a state machine that monitors a fixed set of inputs and automatically acts to turn power on or off in power domains at the lower levels. PPUs take inputs from the PSC, inputs from the device condition status, and inputs from configuration settings from the application code, then PPUs act autonomously to turn on or off power to the domains, and PPUs also control domain clock sources. Thus, the operational processes of the PSC and PPUs automatically and dynamically achieve the best power consumption based on instantaneous power demand.

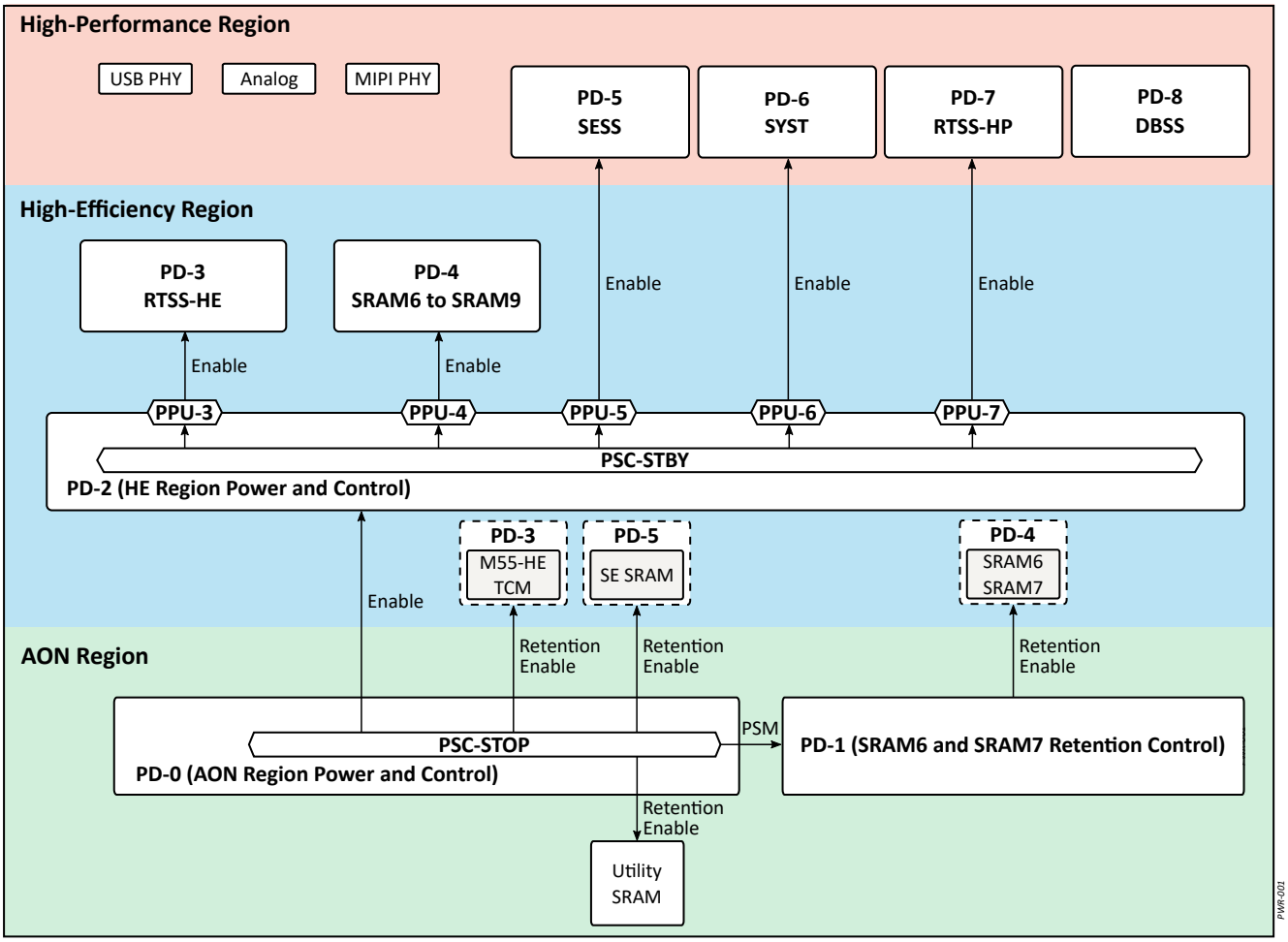
Figure 3-2 illustrates the power domains, control hierarchy, transition possibilities, and relevance to the three operating regions of the device. The power-up sequence of the shown regions and domains is:

1. If VDD_BATT is connected to a constant voltage source, the PD-0 domain and the AON Region are Always-On.
2. The PD-2 domain is first to power up.
3. The next order of powering up the domains depends on whether the device executes an initial boot (cold), or a wake up (warm).

PDs in each of the three device regions are defined as follows:

- AON Region
  - PD-0, AON power and control
  - PD-1, SRAM6 and SRAM7 retention control
- HE Region
  - PD-2, High Efficiency Region power and control
  - PD-3, Real Time Subsystem-High Efficiency (RTSS-HE)
  - PD-4, SRAM6 to SRAM9
- HP Region
  - PD-5, Secure Enclave Subsystem (SESS)
  - PD-6, Shared Peripherals / Shared System Resources (SYST)
  - PD-7, Real Time Subsystem-High Performance (RTSS-HP)
  - PD-8, Debug Subsystem (DBSS)

Figure 3-2 Device Power Domain Hierarchy and Transitions



For more details about PDs power-up and transitions, see the device series-specific Hardware Reference Manual.

Table 3-1 illustrates which specific resources are available within each of the power domains, and how the power domains are related to the three operational regions.

Table 3-1 Device Resources per Power Domain

AON Region	High-Efficiency Region			High-Performance Region			
PD-0	**PD-2**	**PD-3**	**PD-4**	**PD-5**	**PD-6**	**PD-7**	**PD-8**
PSC-STOP	PPU-3	M55-HE	SRAM6	SE CPU	GPIO	M55-HP	SWD
LPTIMER	PPU-4	M55-HE L1 Cache	SRAM7	SE SRAM (SERAM)	MRAM	M55-HP L1 Cache	
LPCMP	PPU-5	M55-HE TCM (SRAM4, SRAM5)	SRAM8	Security Unit	Bulk SRAM (SRAM0, SRAM1)	M55-HP TCM (SRAM2, SRAM3)	
LPGPIO	PPU-6	NPU-HE	SRAM9	System Controls	DMA0	NPU-HP	
LPRTC	PPU-7	LPCPI		SEUART	ETH	DMA1	
BOD	PINMUX	LPPDM			USB	MHU	
POR	LPUART	LPI2S			CANFD/CAN-CNT	WDT_HP	
VTOR	LPI2C	LPSPI			GPU2D	EVTRTR1	
LFRC	EWIC	DMA2			CSI		
LFXO	IRQRTR	MHU			DSI		
VBAT	JTAG	WDT_HE			DPI/CDC		
ANA	HFRC	EVTRTR2			CPI		
STOP_MODE	HFXO	M55HE_CFG			OSPI/AES		
LPGPIO_CTRL	PLL				SDMMC/SDIO		
	PPU-HP				UTIMER		
Optional SRAM Retention:	PPU-HE				QEC		
• Utility SRAM	CGU				I3C		
• M55-HE TCM (SRAM4, SRAM5)	AON				I2C		
• SE SRAM (SERAM)	CLKCTL_SYS				SPI		
PD-1	Host Debug				I2S		
					PDM		
Optional SRAM Retention:					UART		
• SRAM6					ADC12		
• SRAM7					ADC24		
					DAC12		
					CMP		
					TSENS		
					VREF		
					HWSEM		
					EVTRTR0		
					CLKCTL_PER_MST		
					CLKCTL_PER_SLV		
					CRC		
					AXI Bus		

3.6.2 Voltage Supplies

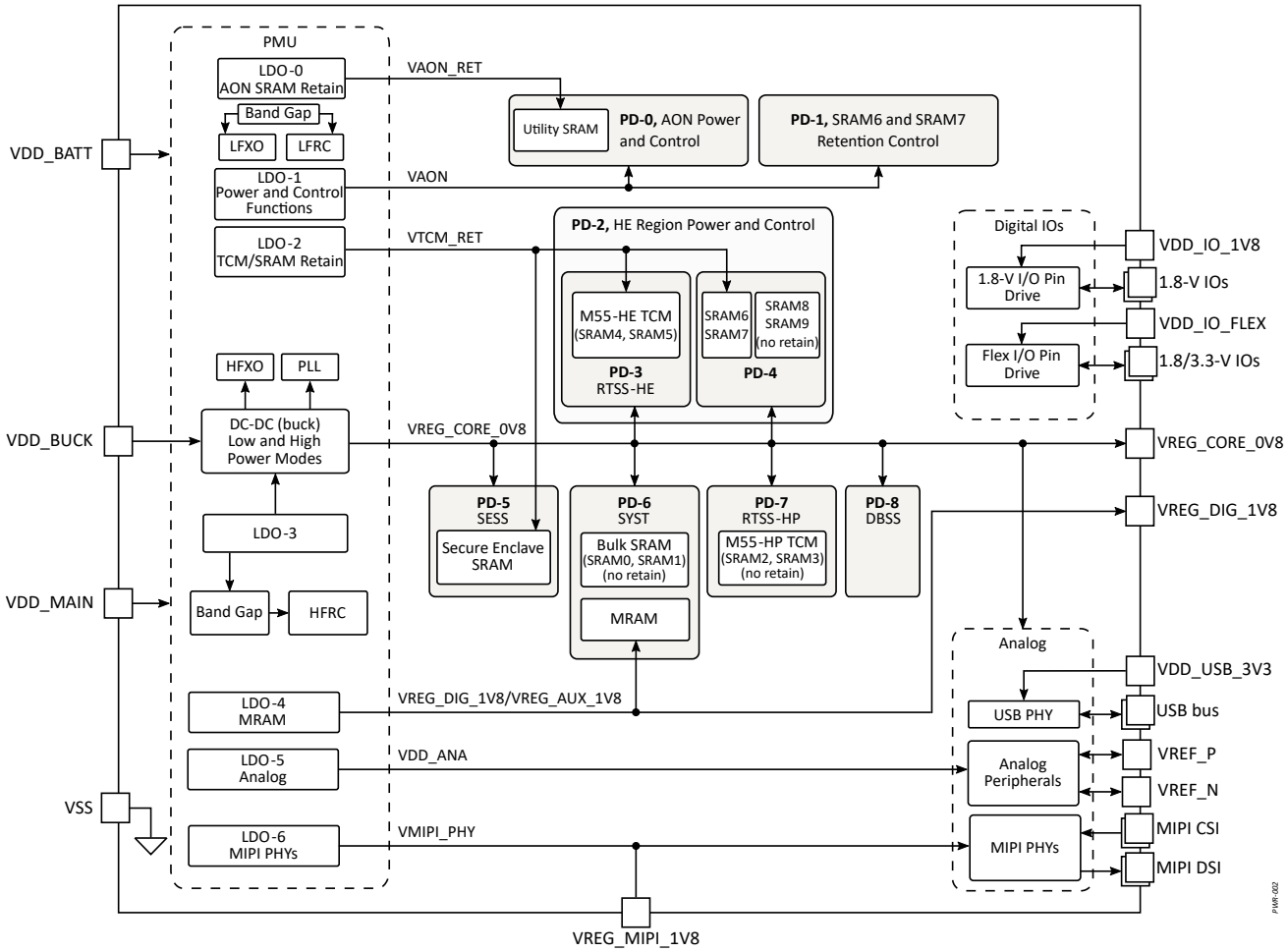
The device power domains are supplied with voltages from several internal supply sources. Power domains that feature SRAM retention have dual voltage supplies.

The device voltage supply and distribution system is architected to:

- Implement the *ai*PM strategy to dynamically power on only what is needed within the most optimum region of the device
- Minimize leakage current in STOP and STANDBY modes
- Rapidly exit low power modes upon a wake-up event
- Minimize dynamic current consumption in GO mode

Figure 3-3 illustrates the voltage distribution inside the device including highly efficient LDO regulators and a DC-DC buck converter. Very few external power sources are required because of the power management capability within the device to generate multiple voltage rails and to correctly sequence the supplies during power up and power down.

Figure 3-3 Device Voltage Distribution



For more information about power supply voltage ranges and general operating conditions, see Section 5.2.1 General Operating Conditions.

Table 3-2 presents power supply signals and provides descriptions to their functions.

Table 3-2 Power Supply Signal Descriptions

Signal Name	Pin Name	Type	Description
VDD_MAIN[5]	VDD_MAIN	PWR	Main power supply
VDD_BATT	VDD_BATT [1]	PWR	Always-On domain power input
VDD_BUCK	VDD_BUCK	PWR	Internal DC-DC converter power input
VDD_USB_3V3	VDD_USB_3V3	PWR	USB power input
VDD_IO_FLEX	VDD_IO_FLEX	PWR	GPIO flex pads (1.8 V [2] - 3.3 V) power input
VDD_IO_1V8	VDD_IO_1V8	PWR	GPIO standard pads (1.8 V) power input
VREG_DIG_1V8	VREG_DIG_1V8 [3]	PWR	Internal 1.8 V regulator output
VREG_AUX_1V8	VREG_AUX_1V8	PWR	Auxiliary 1.8 V regulator output
VDD_MIPI_1V8	VDD_MIPI_1V8	PWR	MIPI PHY power input (connect to VREG_MIPI_1V8)
VREG_MIPI_1V8	VREG_MIPI_1V8	PWR	Internal MIPI PHY 1.8 V power output
VDD_CORE_0V8	VDD_CORE_0V8	PWR	Main digital supply (connect to VREG_CORE_0V8)
VREG_MIPI_0V8	VREG_MIPI_0V8	PWR	MIPI PHY 0.8 V supply decoupling. Connect to decoupling capacitors only.
VREG_CORE_0V8	VREG_CORE_0V8	PWR	Internal DC-DC converter power output
VDD_SX_0V8	VDD_SX_0V8	PWR	Digital power supply to analog blocks (connect to VREG_CORE_0V8)
VDD_PLL_0V8	VDD_PLL_0V8	PWR	Digital power supply to PLL and Band Gaps (must be connected to VREG_CORE_0V8)
VREG_AON	VREG_AON [4]	PWR	Output of internal always-on LDO
VREG_LP_1V8	VREG_LP_1V8	PWR	Output of internal low-power LDO
VREF_P	VREF_P	A	Positive voltage reference for ADC
VREF_N	VREF_N	A	Negative voltage reference for ADC
VSW	VSW	PWR	DC-DC converter switching output (connect to inductor)
VSS_BUCK	VSS_BUCK	GND	DC-DC converter ground
VSS_ANA	VSS_ANA	GND	Analog ground
VSS	VSS	GND	Digital ground

1. VDD_BATT must be connected to VDD_MAIN on the printed circuit board.
2. VDD_IO_FLEX should be connected to VDD_IO_1V8 when 1.8-V mode is used.
3. VREG_DIG_1V8 must be bypassed to ground in one of two ways:
   - Through a 1-µF capacitor in series with a 10 Ω resistor if VDD_MAIN supply range is 1.90 V to 4.2 V.
   - Through a 100-nF capacitor if VDD_MAIN supply range is 1.75 V to 1.90 V.
4. VREG_AON must be bypassed to ground through a 1-µF capacitor in series with a 1.0 kΩ resistor.
5. BOR and BOD functions not supported below 1.9 V.

CAUTION

The decoupling for VREG_AON and VREG_DIG_1V8 pins must be present on the PCB or otherwise the device may be at risk for damage.

NOTE

Refer to Application Note AAPN0027, *PCB Layout Guidelines for Ensemble MCUs and Fusion Processors*, for detailed information about power decoupling for all power pins.

For more information about power supply voltage ranges and general operating conditions, see Section 5.2.1 General Operating Conditions.

3.6.3 Power Modes

Using *ai*PM, this device provides significant flexibility to balance power, performance, and wake-up time per application use case. The device-level power modes described in Table 3-4 make use of the power domains and the voltage supplies, described in Section 5.2.1 General Operating Conditions, to achieve this balance. Within each power mode the clock speed and clock gating can be fine-tuned for each core and peripheral to reduce power consumption.

Table 3-3 Individual CPU States Summary

CPU State	Description
RUN	When a CPU core is running and executing code.
SLEEP	When a CPU core is clock gated and can quickly resume.
OFF(1)	When a CPU core is powered down.

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.

Table 3-4 Device Power Mode Summary

Device Power Mode	Description	Wake-Up Peripherals
GO	One or more processing subsystems are in RUN state. See Table 3-3.	All
READY	All processing subsystems are in SLEEP state. See Table 3-3.	All
IDLE	All processing subsystems are in OFF state. See Table 3-3.	All(1)
STANDBY	All processing subsystems and shared resources in the HP Region are powered down.	LPUART, LPI2C, plus STOP mode peripherals
STOP	All processing subsystems and shared resources in the HP and HE Regions are powered down. Few peripherals remain on with extremely low leakage.	LPTIMER, LPCMP, LPRTC, and LPGPIO

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.

For more details about specific power consumption and wake-up times per power mode, see Section 5.2.2 Device Power Modes.

3.6.4 Power Supply Supervisors

The device has integrated supervisory circuits for Brown-Out Reset (BOR), Brown-Out Detect (BOD), and Power-On-Reset (POR).

There is one POR circuit, VBAT_POR, which monitors the VDD_BATT (AON Region) and keeps the entire device in reset during initial power ramp to the device.

The BOD circuit monitors the VDD_MAIN power supply and generates interrupts when the voltage falls below a programmable threshold. The BOD interrupt can be used as a wake-up source from STANDBY and

from STOP low-power modes. For applications utilizing the BOD, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

The BOR circuit monitors the VDD_MAIN power supply and causes an immediate reset to the main SoC when the voltage falls below a programmable threshold. For applications utilizing the BOR, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

The POR circuit is described further in Section 3.7 Reset Management Overview.

Table 3-5 summarizes the power supply supervisory functions.

Table 3-5 Power Supply Supervisory Functions

Power Supply	Supervisor Type	Supervisory Function
VDD_BATT	POR	Fixed threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains.
VDD_MAIN	BOR	Programmable threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains. For applications utilizing the BOR function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.
VDD_MAIN	BOD	Programmable threshold, triggers interrupts to the M55-HP, M55-HE and SE, and a request to DMA. For applications utilizing the BOD function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

3.7 Reset Management Overview

A reset brings the entire device (cold reset) or part of the device (warm reset) to a known good state.

The reset subsystem of the device is based on a Reset Controller (RSTC). The RSTC handles top-level reset conditions—VBAT_POR and software reset requests.

Figure 3-4 shows the main reset sources in the device.

Figure 3-4 Top-Level Reset Diagram

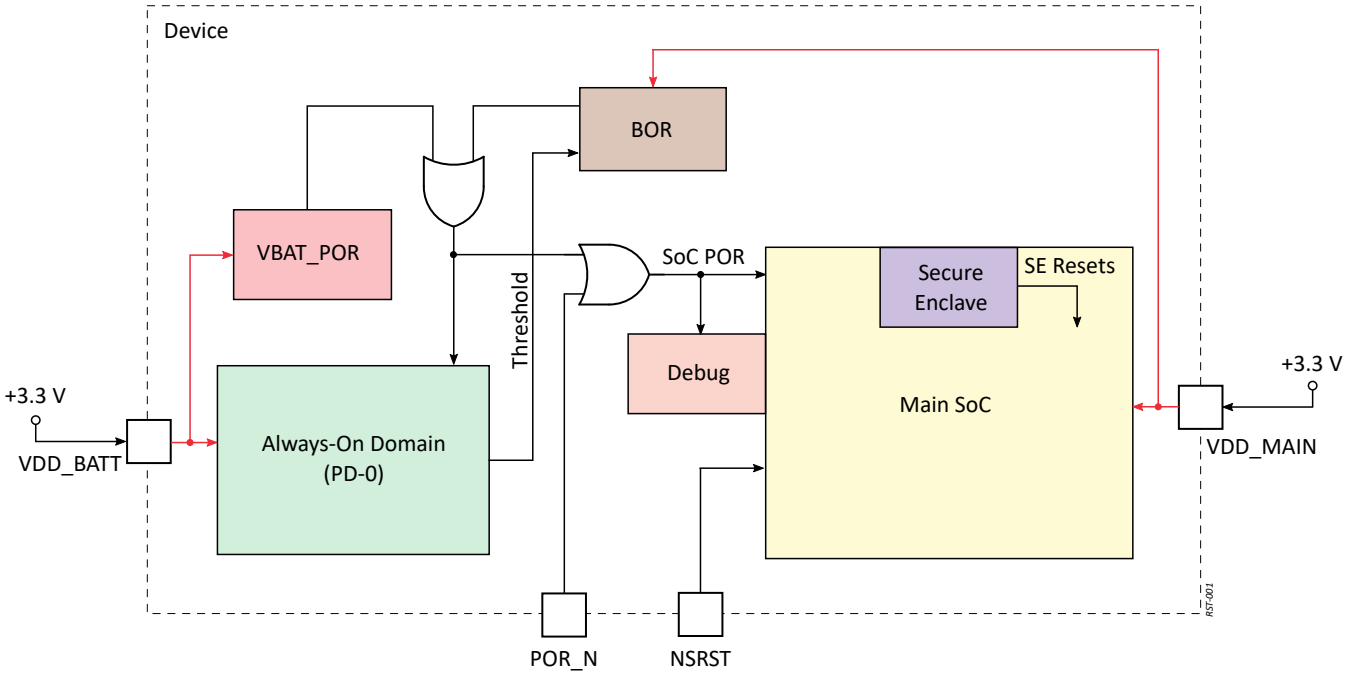


Table 3-6 lists the main reset sources along with their types and functions.

Table 3-6 Device Main Reset Sources

Reset Source	Hardware/Software	Description
POR_N pin (active-low)	HW	System cold Reset pin. Asserting this pin is equivalent to turning the device power off. After POR_N is deasserted, the device completes a full power on cycle, which is equivalent to a cold start. No logic or memory retains its state.
NSRST pin (active-low)	HW	System warm Reset pin. Typically, an external debugger asserts this reset pin. It resets all logic in the device except for PD-0 Always-On peripherals, debug logic, and the JTAG interface.
VBAT_POR monitor	HW	Fundamental POR. VBAT_POR keeps the entire device in reset during a power-on ramp-up until the device reaches the operational threshold.
BOR monitor	HW and SW	Brown-out reset. BOR assertion is equivalent to turning the device power off. After deasserting BOR, the device completes a full power on cycle, which is equivalent to a cold start. For applications utilizing the BOR function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.
Secure Enclave Reset	SW	Warm reset by Secure Enclave. Initializes all logic except for PD-0 Always-On, the debug logic, and the JTAG interface.

Reset Source	Hardware/Software	Description
SW_HP_RST	SW	High-performance subsystem (RTSS-HP) reset. Warm reset by Secure Enclave. RTSS-HP reset reasons logged to RTSS_HP_RESET register.
SW_HE_RST	SW	High-efficiency subsystem (RTSS-HE) reset. Warm reset by Secure Enclave. RTSS-HE reset reasons logged to RTSS_HE_RESET register.

Table 3-7 presents Reset signals and provides descriptions to their functions.

Table 3-7 Reset Signal Descriptions

Signal Name	Pin Name	Type	Description
NSRST	NSRST	I	JTAG reset (system reset) active low
POR_N	POR_N	I	Power-On-Reset (cold reset) active low

3.8 Clock Generation and Control

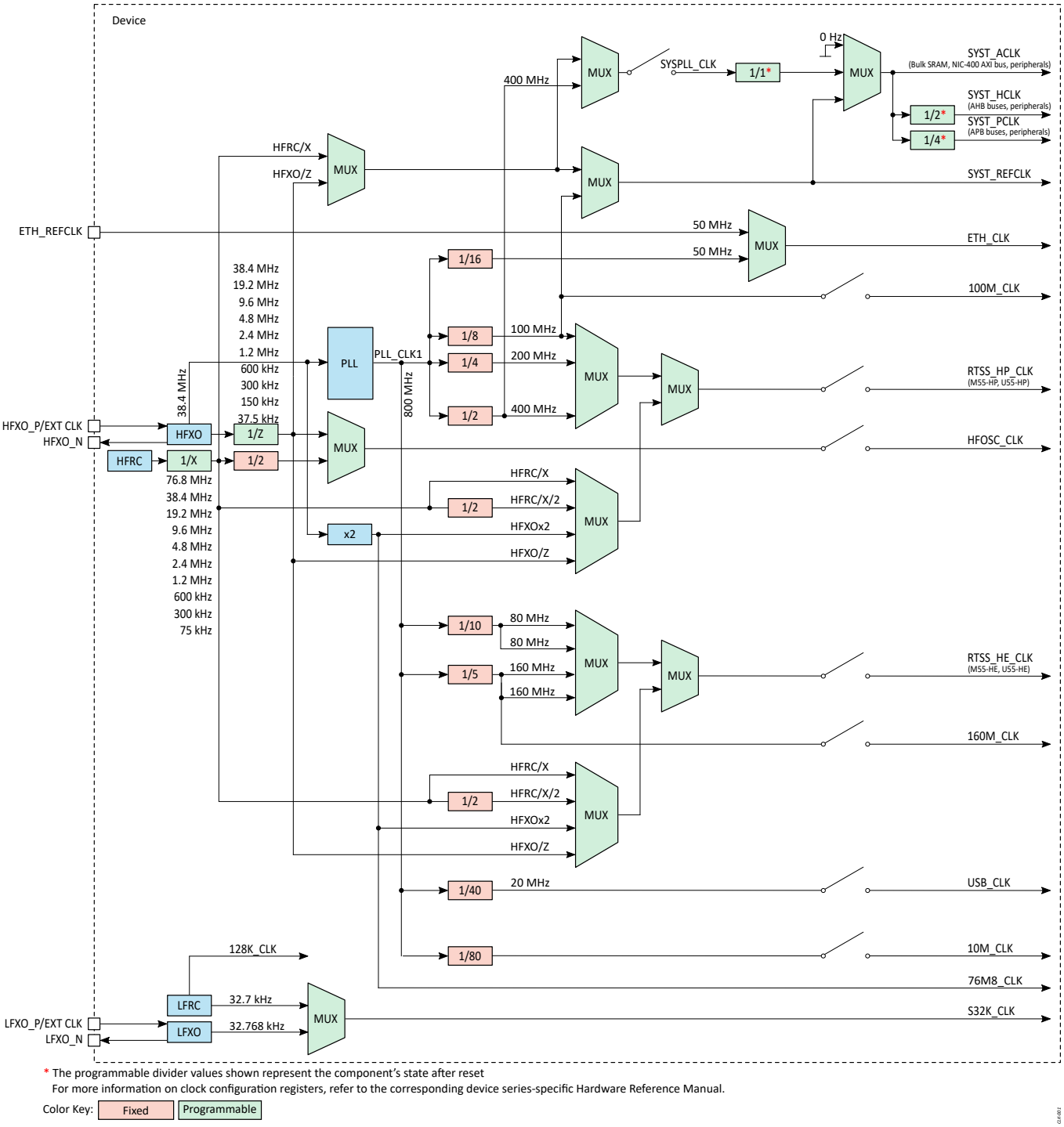
The device clocking scheme includes several clock domains, PLL, clock dividers, clock multiplexers, and four oscillators. The PLL has a single clock output.

The device clock sources are as follows:

- Low-Frequency Resistor-Capacitor (LFRC) oscillator—a low-power, internal RC oscillator powered by VDD_BATT. This oscillator is used during the power-up sequence, with a typical clock frequency accuracy of 32.7 kHz ±4%.
- Low-Frequency crystal Oscillator (LFXO)—a low-power oscillator that can be used with a high-accuracy 32.768 kHz external crystal. This oscillator is powered by VDD_BATT. It is enabled at power-up and is the typical clock source for LPRTC. The LFXO oscillator input may optionally be configured in bypass mode for connection to an external 32.768 kHz clock source.
- High-Frequency Resistor-Capacitor (HFRC) oscillator—a low-power internal RC oscillator that is able to generate frequencies of up to 76.8 MHz. When the LFXO clock source is available, the HFRC oscillator can be trimmed to reach an accuracy of ±2% or better over temperature. The HFRC oscillator is available in all power modes except for STOP mode. This oscillator can be used during a power-up sequence for rapid initialization and fast start-up.
- High-Frequency crystal Oscillator (HFXO)—a power-optimized oscillator that can be used with an external crystal with a frequency between 24 MHz and 38.4 MHz. This oscillator is enabled by software after initial device configuration and is the source clock for the PLL. The HFXO oscillator input may optionally be configured in bypass mode for connection to an external high-speed clock source/oscillator.
- Phase-Locked Loop (PLL)—a power-optimized, fast-locking clock multiplier with fractional mode. It has a single clock output used to supply most of the device subsystems, modules, and interconnects.

Figure 3-5 provides a high-level overview of the clocking scheme implementation in the device.

Figure 3-5 Device Clocking Scheme Overview



* The programmable divider values shown represent the component's state after reset
For more information on clock configuration registers, refer to the corresponding device series-specific Hardware Reference Manual.

Color Key: Fixed | Programmable

NOTE

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

Table 3-8 presents clock interface signals and provides descriptions to their functions.

Table 3-8 Clock Signal Descriptions

Signal Name	Pin Name	Type	Description
HFXO_P	HFXO_P	I	High-frequency oscillator input
HFXO_N	HFXO_N	O	High-frequency oscillator output
LFXO_P	LFXO_P	I	Low-frequency oscillator input
LFXO_N	LFXO_N	O	Low-frequency oscillator output

3.9 Signal Multiplexing and I/O Buffer Configuration

3.9.1 Signal Multiplexing

The device offers a sophisticated signal-to-pin multiplexing scheme. Each I/O pin may be assigned to one of up to eight peripheral signals, and vice versa, a peripheral signal may be routed to up to four I/O pins. This assignment is pseudo-static and must be performed once during boot time.

The multiplexed pins are divided into 8-pin groups, also referred to as 'ports'. A pin identifier 'Pn_i' may be used, where *n* is the port number and *i* is the pin number within that port. A pin may be referenced also with the GPIO peripheral's signal name 'GPIOn_i' because it shares the same numbering convention. For more information on the GPIO peripheral, see Section 3.15 General-Purpose Input/Output Module.

MIPI-CSI, MIPI-DSI, USB PHY pins, and power and ground pins have fixed functions and cannot be multiplexed.

Figure 3-6 shows the P0_0 multiplexing as an example. The Pn_i[PINMUX] register bitfield, where n = i = 0, selects a peripheral signal to be available on P0_0. The multiplexer switches three signals at a time: IN, OUT, and OEN (output enable). OEN could be dynamically driven by the peripheral, for example by the I2C which needs to change the Data pin direction very frequently. For many other peripherals OEN could be static, and for GPIO it is programmable via its Data Direction register. The analog peripherals are not multiplexed between themselves and all three can read P0_0 when [PINMUX] = 7. For more information on configuration registers, refer to the corresponding device series-specific Hardware Reference Manual.

Figure 3-6 I/O Signal Multiplexing (P0_0 Example)

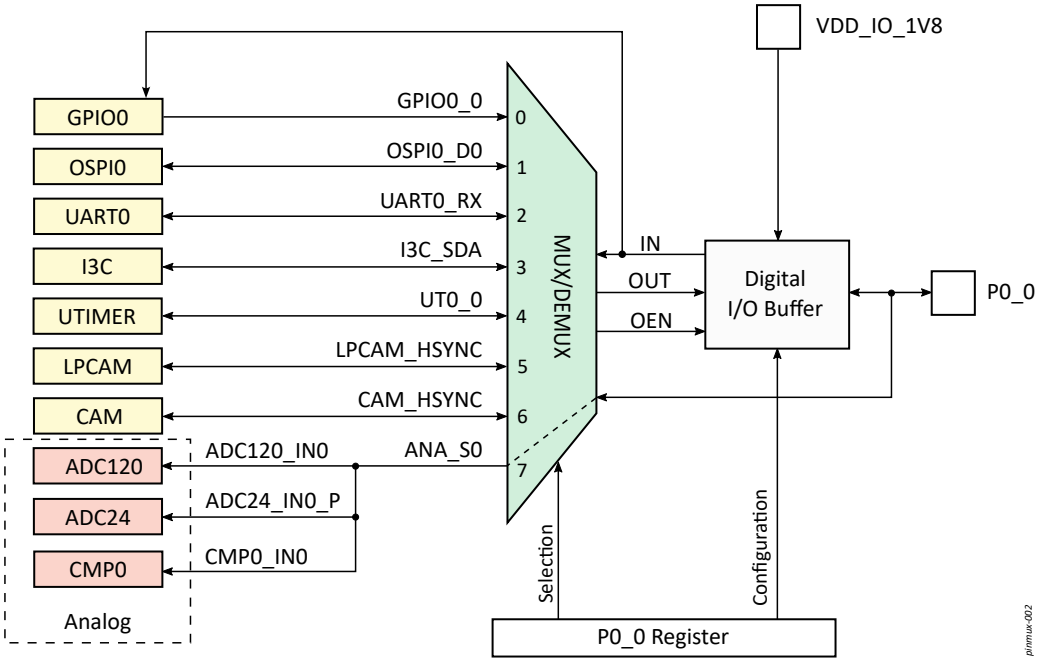
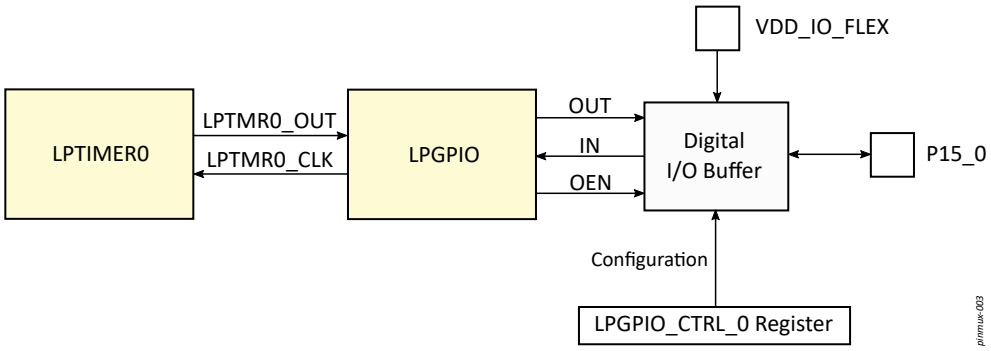


Figure 3-7 shows the LPGPIO pin sharing. Because Port 15 is located in the Always-On domain, here pin sharing is achieved differently. That is, there is no multiplexing as such. In this example, LPTIMER0 gets access to P15_0 via the LPGPIO module. LPGPIO controls the pin direction depending on the value written to its Data Direction register.

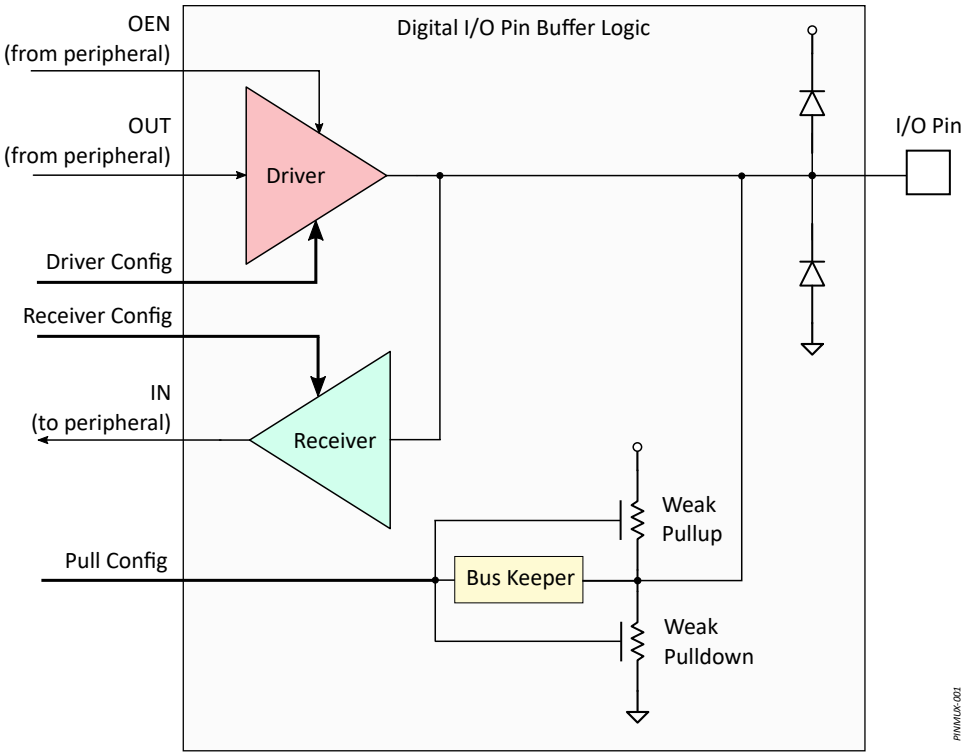
Figure 3-7 LPGPIO/LPTIMER Pin Sharing (P15_0 Example)



3.9.2 I/O Buffer Configuration

Figure 3-8 shows a top-level block diagram of a digital I/O buffer module. I/O buffer consists of configurable output buffer (driver), input buffer (receiver), pull-up/pull-down block, and protective diodes.

Figure 3-8 I/O Buffer Block Diagram



The I/O buffer has the following main features:

- Configurable direction (input, output or both)
- Selectable driver-disabled state:
  - No pull (Hi-Z, floating)
  - Weak pull-up
  - Weak pull-down
  - Bus keeper (keeps the last state seen on the pin)
- Configurable drive strength
- Configurable slew rate
- Output driver can be open drain or push-pull type
- Input may have a Schmitt trigger enabled which adds hysteresis to signal transitions
- Dedicated power rails:
  - VDD_IO_FLEX for the 1.8-V/3.3-V pins (GPIO7_[4-7] and GPIOV_[0-3])
  - VDD_IO_1V8 for the 1.8-V pins

The Pn_i registers contain bitfields controlling the following parameters:

- Driver type—[DRV] (open drain or push-pull)
- Output drive strength—[E] (2 mA, 4 mA, 8 mA, or 12 mA)
- Driver disabled state—[P] (Hi-Z, Pull-up, Pull-down, or Bus Keeper)
- Slew rate—[SR] (slow [half-speed] or fast)
- Schmitt trigger enable—[SMT]
- Receiver enable—[REN]

Similar I/O buffer controls exist also for Port 15 in the LPGPIO_CTRL_n[DRIVER] and LPGPIO_CTRL_n [RECEIVER] register bitfields.

NOTE

For more information on I/O buffer configuration registers, refer to sub-sections *PINMUX Registers Guide* and *LPGPIO_CTRL Registers Guide* in Section *Signal Multiplexing and I/O Buffer Configuration* of the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

3.10 Inter-Processor Communication

3.10.1 HWSEM Overview

The Hardware Semaphore (HWSEM) provides a mechanism for coordinating the concurrency between processor cores when they access shared resources—memory regions or peripherals.

The device includes 16 HWSEM modules with individual interrupt requests. Each of the semaphores can be assigned depending on the application needs.

Each HWSEM module supports the following main features:

- Acquire, Release, and Reset functions as atomic operation
- Single-processor access at a time
- An internal acquisition counter for enabling processor owning of a HWSEM to acquire it multiple times
- An interrupt assertion once the HWSEM becomes available

3.10.2 MHU Overview

The Message Handling Unit (MHU) provides point-to-point communication between the Secure Enclave processor and the two Real-Time processors (M55-HP and M55-HE). The MHU is an interrupt-based communication between two processing entities.

The device includes up to 12 unidirectional MHU modules.

Each of the MHU modules supports the following main features:

- Two memory mapped register frames—Sender and Receiver
- Unidirectional communication interface
- Read and write access—32-bit word aligned
- Dual transport channels
- Different transport protocols—Doorbell, Single-Word transfer, and Multi-Word
- Dedicated interrupt lines for the Sender and Receiver

The software responsibilities are:

- To request the Receiver to be powered
- To ensure that the Sender remains powered until the transfer has been finished
- To use Ready to Send protocol to send the transfer

Each processor entity includes only one of the Sender or Receiver frame. To ensure a bi-directional (full-duplex) communication between the entities, two MHUs with reversed Sender and Receiver parts are implemented.

3.11 Memories

3.11.1 MRAM Overview

The MRAM module is a type of non-volatile random-access memory which stores information in magnetic elements.

The MRAM operates at 33 MHz clock frequency over 128-bit data bus. The 128-bit (16-byte) word represents the minimum sector size for the MRAM. The smaller granularity offers much better efficiency compared to the legacy flash memory modules. It takes flash memories longer to be programmed/erased due to their much larger sector sizes.

The MRAM module implements a state machine controlling the erase and programming sequence of 16-byte memory blocks. This operation is transparent to the CPU core.

The MRAM controller implements read cache and write buffer mechanism that enables the concurrent read and write operations. This greatly benefits the implementation of multi-core applications that are not required to coordinate the access to the MRAM. Up to four bus masters can originate concurrent write operations, while the number of concurrent read operations is not limited.

The MRAM supports the following main features:

- Size up to 5.5MB
- High endurance (more than 100 000 erase cycles)
- More than 10 years data retention (at 125 °C junction temperature)
- 16 ECC bits for each 128-bit data word
- 2× 16 bytes read cache to accelerate access to frequently used data and non-16-byte aligned read requests
- Built-in state machine controlling 16-byte program/erase cycle (no need of driver)
- Concurrent write (up to four bus masters) and read operations (no need for synchronization between them)
- DMA write operation with up to 128 bytes in each DMA write cycle data payload

3.11.2 SRAM Overview

The device contains the following types of on-chip SRAM memories:

- User SRAM available for all bus masters:
  - Bulk SRAM: SRAM0 and SRAM1
  - M55-HP TCM: SRAM2 (M55-HP ITCM) and SRAM3 (M55-HP DTCM)
  - M55-HE TCM: SRAM4 (M55-HE ITCM) and SRAM5 (M55-HE DTCM), with optional retention
  - Other shared SRAM blocks: SRAM6_A/B, SRAM7, SRAM8, and SRAM9_A/B
- Processor cache memories:
  - M55-HP Level 1 cache
  - M55-HE Level 1 cache
- Utility SRAM
  - Located in Always-On domain

It is possible to configure address ranges within SRAM0 and SRAM1 to appear as contiguous address space to a given M55 core through configuration of the firewall controllers. For more information, refer to the corresponding device series-specific Hardware Reference Manual, Section Interconnect Firewall Functional Description.

The embedded bulk SRAM is a general-purpose memory to be shared among all applications. It is partitioned into two blocks, each having 64-bit wide data bus and providing read/write operation at 400 MHz. The bulk memory blocks can be accessed in parallel over the main 64-bit AXI bus running at 400 MHz.

The TCM is an SRAM block providing high-bandwidth and low latency access. The TCM is primarily used by the M55 core it is attached to. Alternatively, it can be shared with other bus masters in the device.

The cache memory is a high-performance SRAM accelerating the CPU access to frequently used instructions and data. The M55 processors have Level 1 cache memories dedicated to each M55 core.

The data retention of SRAM is used for context saving during low power modes.

The device includes the following quantities of SRAM with their performance characteristics:

- User SRAM available to all bus masters:
  - Up to 13.5MB:
    - 4MB bulk SRAM0 + up to 2.5MB bulk SRAM1
    - 0.25MB SRAM2 (M55-HP ITCM) + 1MB SRAM3 (M55-HP DTCM)
    - 0.25MB SRAM4 (M55-HE ITCM) + 0.25MB SRAM5 (M55-HE DTCM), with optional data retention
    - 1MB SRAM6_A + 1MB SRAM6_B + 0.5MB SRAM7 + 2MB SRAM8 + 0.25MB SRAM9_A + 0.5MB SRAM9_B
  - 400 MHz parallel read/write access
- Real-time processors (M55) cache memories:
  - Level 1 Cache: 32KB Instruction and 32KB Data cache per core
- Utility SRAM:
  - 4KB in Always-On power domain PD-0
  - 100 MHz read/write access (32-bit wide access only)

NOTE

User SRAM size and availability is device part number dependent. For more information on SRAM blocks enabled for each part number and their sizes, see Section 7 Ordering Information.

3.11.3 TCM Overview

The Tightly Coupled Memory (TCM) is a high-bandwidth and low latency memory. The TCM enables the Cortex-M55 cores to perform vector operations with high efficiency and process interrupts with minimum latency. The TCM access time is a single clock cycle with no wait states for reads. The TCM interface is based on Harvard architecture—it has one instruction memory (ITCM0) bus and four data memory (DTCM0/1/2/3) buses, all 32-bit wide.

Both M55-HP and M55-HE cores can use the ITCM for storing data and can fetch instructions out of the DTCM. In this scenario, the TCM access time is slower and vector operations are not supported.

The Cortex-M55 cores have the following TCM configurations:

- M55-HP:
  - 256KB of ITCM and 4 × 256KB of DTCM (total of 1.25MB)
  - 1 × 32-bit ITCM and 4 × 32-bit DTCM memory buses
  - Single-cycle read/write access at 400 MHz
  - Concurrent share of TCM with the other processing entities via AHB slave port
- M55-HE:
  - 256KB of ITCM and 4 × 64KB of DTCM (total of 512KB)
  - 1 × 32-bit ITCM and 4 × 32-bit DTCM memory buses

- Single-cycle read/write access at 160 MHz
- Concurrent share of TCM with the other processing entities via AHB slave port
- Optional content retention

3.11.4 External Memory Expansion Options

The device provides two options to expand the memory using external devices:

- 1× SDMMC interface
- 2× OSPI interface

The SDMMC interface can be used to access embedded or external memory cards with clock frequency up to 50 MHz. The data bus is up to 8 bits wide. This external memory interface is suitable for expanding the bulk data storage capacity in the form of an external flash-based file system. The SDMMC interface supports legacy 4-bit cards as well.

The OSPI interfaces can be used to access external flash memory devices. Each OSPI supports Double Data Rate (DDR) mode transferring 8-bit data on both edges of the clock signal. The maximum clock frequency is up to 100 MHz delivering raw DDR bandwidth of up to 200 MB/s.

The OSPI interface could access the memory in two modes—directly (through register read/write operations) or indirectly (through memory-mapped operations). The indirect access supports eXecute-in-Place (XIP) mode which translates the instruction fetch operations to proper address and data read transactions. This way, the external memory devices expand the available non-volatile memory.

The OSPI interfaces support legacy Single, Dual, Quad, or Octal SPI flash memory devices.

Each OSPI interface also supports the HyperBus protocol in direct and indirect modes. This enables the integration of external Static or Pseudo-Static RAM devices. See operation limitations in Section 3.17.1 Cryptographic OSPI Overview.

Each OSPI interface can be attached to a flash or SRAM devices based on the application needs.

The device includes two AES decoders—one for each OSPI interface. The decoders are implemented in hardware and enable on-the-fly decoding of the external memory content. This allows protecting the OSPI code or the confidentiality of the data stored in external devices. The decoders effectively add no latency while maintaining the overall external memory interface bandwidth.

3.11.5 Memory Mapping

Refer to the device series-specific Hardware Reference Manual for details on the memory mapping.

3.12 Interrupts and Events Management

3.12.1 NVIC Overview

The Nested Vectored Interrupt Controller (NVIC) resides in each of the M55-HP and M55-HE processors, and it is closely integrated with the Cortex-M55 core to achieve low-latency interrupt processing. Both NVIC modules have the same configuration in the device.

Each NVIC module supports the following main features:

- Maintaining the current execution priority of the Cortex-M55 processor
- Maintaining the pending and active status of all exceptions that are supported
- Invoking preemption when a pending exception has priority
- Providing wake-up signals to wake up the Cortex-M55 processor from deep sleep mode

- Providing support to the Internal Wakeup Interrupt Controller (IWIC) and External Wakeup Interrupt Controller (EWIC)
- Providing priority and exception information to other processor components
- 480 external interrupts, with 256 priority levels per interrupt

3.12.2 IRQRTR Overview

The shared Interrupt Router (IRQRTR) is intended to route interrupt signals from the device peripherals to all processing entities. It has an input port wired to the interrupt sources and three output ports connected to the Secure Enclave and the two Real-Time Processing interrupt controllers.

The router configuration registers define which interrupt sources are enabled and their destination output ports. Once configured, the router can be locked fully or partially so that further changes can be restricted.

The access to the IRQRTR configuration may be constrained based on the device security policy. In this case, the interrupt routing can be indirectly setup by service call to the Secure Enclave.

The IRQRTR supports the following main features:

- Manages up to 427 shared interrupts
- Configures routing of the interrupt signals to up to four processing entities
- Supports configuration access lockdown
- Reports tamper interrupts to the Secure Enclave

3.12.3 EVTRTR Overview

The device integrates a large number of peripherals that can generate events indicating changes in their state, receiving of data or completion of an operation. The Event Router (EVTRTR) is a module that can associate an event originated by one peripheral with an action executed by another.

The function of the EVTRTR is similar to the shared Interrupt Router (IRQRTR), which targets an interrupt controller and ultimately a CPU core. Unlike the IRQRTR, the EVTRTR is connecting the event signal to a peripheral that executes an action without involving any CPU core.

Modules generating such event signals include: GPIO, UTIMER, I2C, SPI, UART, and others. The EVTRTR passes the signals through edge-detection circuits and gating logic before routing them to specific targets.

The device includes three Event Routers, each dedicated to a specific target:

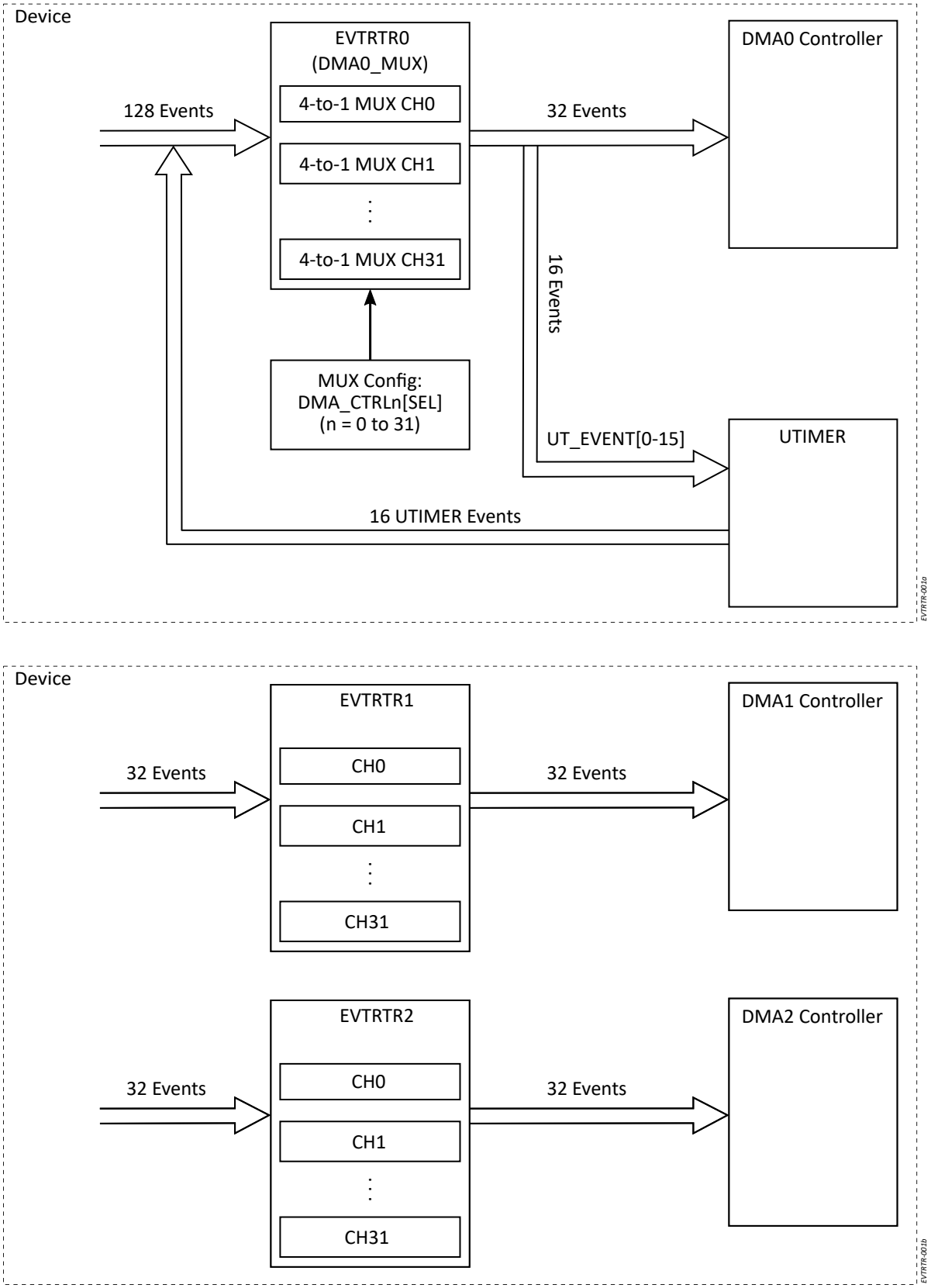
- EVTRTR0, dedicated to DMA0 controller and UTIMER
- EVTRTR1, dedicated to DMA1 controller
- EVTRTR2, dedicated to DMA2 controller

Each EVTRTR provides the following main features:

- Software generated events
- Zero wait state for event routing between peripherals in the same clock domain
- Automatic synchronization of events and triggers between peripherals in different clock domains
- DMA channel enable, handshake status and type selection

Figure 3-9 provides a high-level overview of the EVTRTR implementation in the device.

Figure 3-9 EVTRTR Overview



EVTRTR0 is also referred to as DMA0_MUX and expands the available 32 inputs of DMA0 by exposing the DMA channels to 128 different peripheral events via 32 × 4-to-1 multiplexers. The first 16 multiplexed DMA0 requests are also routed as input triggers to the Universal Timer (UTIMER). This mechanism enables the implementation of complex state machines involving the use of peripheral or time-based events that trigger data transfers and/or timer triggers.

EVTRTR1 and EVTRTR2 support 32 input events/output DMA channels each, without implementing events multiplexing.

3.13 DMA Management

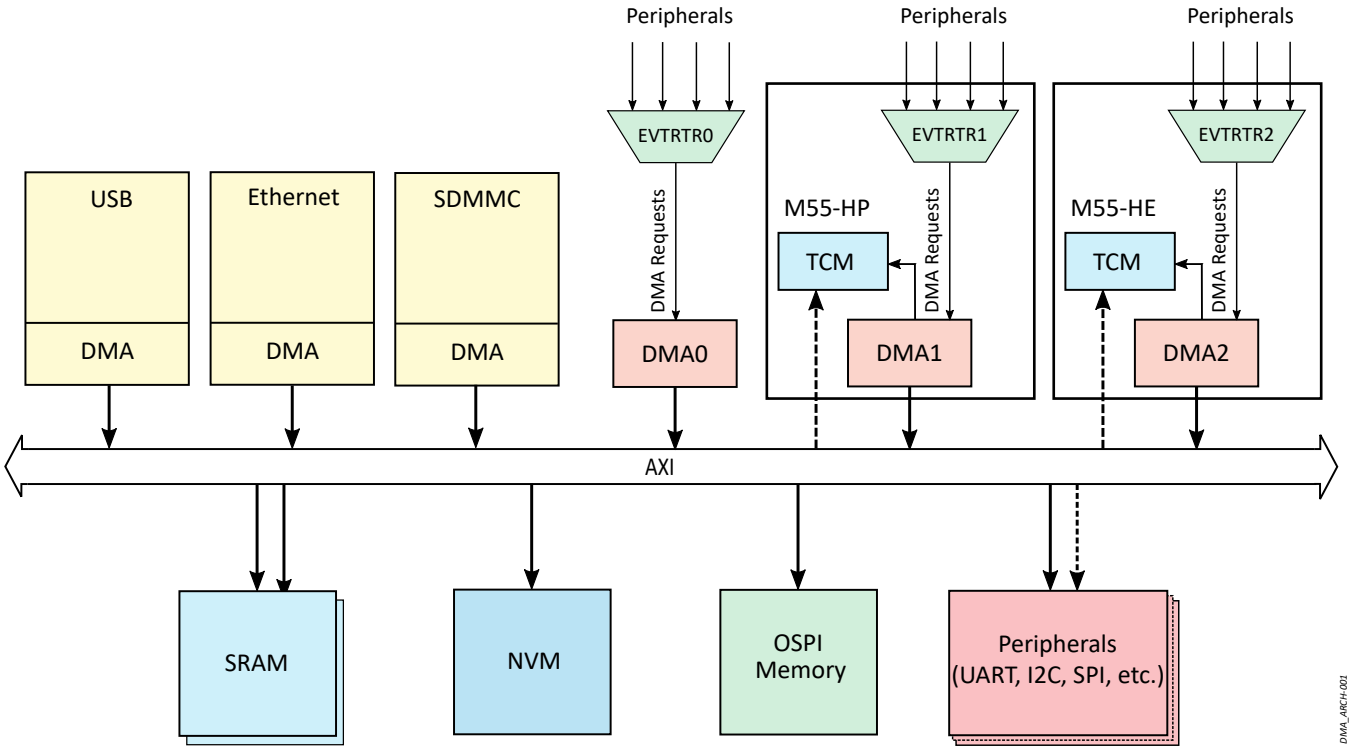
3.13.1 DMA Architecture Overview

The device features Direct Memory Access (DMA) controllers to offload the CPUs from repeated data transfer tasks. The device has the following DMA controllers:

- USB embedded DMA controller
- Ethernet embedded DMA controller
- SDMMC embedded DMA controller
- DMA0: Can be shared by all of the CPU cores and carries out data transfers from/to ADC, PDM, I2C, I3C, CANFD, SPI, OSPI, and UART. DMA0 also supports multiple DMA triggers like GPIO pins and timer events.
- DMA1: Dedicated to the RTSS-HP subsystem and serves DMA requests from CMP, QEC, UART, UTIMER, and via GPIO pins.
- DMA2: Dedicated to the RTSS-HE subsystem and can move data from/to the Low Power (LP) peripherals (such as LPUART), ADC, CANFD, and I3C. Additionally, BOD, LPTIMER, LPCAM_VSYNC, LPCAM_HSYNC, and LPGPIO transitions can trigger DMA requests.

Figure 3-10 gives a high-level overview of the DMA architecture in the device.

Figure 3-10 DMA Architecture



The high-speed interface peripherals (USB, ETH, and SDMMC) have their own, embedded DMA controllers. They are optimized for the specific needs of these interfaces.

DMA0, DMA1 and DMA2 are general-purpose, programmable, multi-channel, and TrustZone-aware DMA controllers (DMACs). Each of them has 32 inputs for accepting DMA requests from various device peripherals and triggers (for example, UART Tx and Rx, ADC conversion done, etc). The Event Routers positioned in front of the DMA controllers provide support for DMA handshaking between peripherals and DMACs. Additionally, EVTRTR0 provides 32 × 4-to-1 programmable multiplexers, which expose the 32 DMA0 inputs to 128 possible DMA requests from peripherals, thus providing an increased flexibility. Each DMA controller supports 8 internal data channels (FIFOs). All channels can perform independently programmed transactions including different data lengths, source and destination addresses, single or burst transfers.

DMA0 controller can be shared by all of the CPU cores. The security privilege of each channel is run-time programmable. DMA0 initiates transactions on the main AXI bus with its unique Stream ID. Each of the 32 request interfaces can generate an interrupt request signal. The interrupts are shared over the Interrupt Router (IRQRTR) with all of the CPU cores.

DMA1 and DMA2 controllers are assigned to the M55-HP and M55-HE CPU cores, respectively. They reside in their domains and share their AXI-bus Stream IDs (and security policy). The DMA1 and DMA2 request interfaces can generate individual interrupt requests, attached locally to their respective M55 cores.

3.13.2 DMA Controllers Overview

The device includes three copies of the general-purpose DMA Controller (DMAC):

- DMA0 can be shared among all CPU cores
- DMA1, dedicated to the RTSS-HP
- DMA2, dedicated to the RTSS-HE

Each DMAC supports the following main features:

- Flexible instruction set for programming DMA transfers
- Transfer types:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Scatter-gather
- 32 peripheral request interfaces (DMA_Req/DMA_Ack)
- 8 DMA channels (VFIFOs)
- Flagging of various DMA events using 33 interrupt signals
  - 32 interrupts, one per DMA request interface
  - One data abort interrupt
- Dual slave interfaces, secure and non-secure, for accessing registers
- Programmable security state for each DMA channel
- Arm TrustZone technology
- 4 active AXI read transactions
- 4 active AXI write transactions
- 32 deep internal data buffer (MFIFO)
- 4 lines in the instruction cache with 8 words in a line
- 8 deep read instruction queue
- 8 deep write instruction queue
- Request acceptance capability of a peripheral request interface—4 requests

3.14 Timers and Counters

3.14.1 LPTIMER Overview

The 32-bit Low-Power Timer (LPTIMER) module counts down from a programmed value and generates an interrupt when the count reaches zero. Two events can cause the timer to load the initial value from which it counts down. The first event is when the timer is enabled after being reset or disabled, and the second event is when the timer count reaches zero.

The device includes up to four independent LPTIMER modules (“channels”), accessible through a single bus.

Each LPTIMER module supports the following main features:

- 32-bit down counter
- Free-running and user-defined count modes
- Asynchronous event counting
- Individual toggle output
- Individual interrupt output
- Independent clock input that can be connected either to internal clocks or to an external clock source
- Each odd numbered LPTIMER module can be concatenated with the previous even numbered LPTIMER module to form up to a 64-bit timer
- The LPTIMER interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPTIMER. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-9 presents LPTIMER interface signals and provides descriptions to their functions.

Table 3-9 LPTIMER Signal Descriptions

Signal Name	Pin Name	Type	Description
LPTIMER0			
LPTMR0_CLK_IO	P15_0	IO	LPTIMER0_CLK: LPTIMR0 input clock from pin.
			LPTIMER0_OUT: LPTIMER0 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.
LPTIMER1			
LPTMR1_CLK_IO	P15_1	IO	LPTIMER1_CLK: LPTIMR1 input clock from pin.
			LPTIMER1_OUT: LPTIMER1 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.
LPTIMER2			
LPTMR2_CLK_IO	P15_2	IO	LPTIMER2_CLK: LPTIMR2 input clock from pin.
			LPTIMER2_OUT: LPTIMER2 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.

Signal Name	Pin Name	Type	Description
LPTIMER3			
LPTMR3_CLK_IO	P15_3	IO	LPTIMER3_CLK: LPTIMR3 input clock from pin.
			LPTIMER3_OUT: LPTIMER3 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.

3.14.2 UTIMER Overview

The 32-bit high-resolution Universal Timer (UTIMER) typically serves as a standard signal timing generator and a pulse counter. In addition, the UTIMER can also be used to implement a quadrature encoder interface and serve as a Quadrature Encoder Counter (QEC).

The device includes up to sixteen independent UTIMER modules (“channels”), which are allocated as follows:

- Up to twelve standard UTIMER modules: Channel 0 (UTIMER0) to Channel 11 (UTIMER11)
- Up to four UTIMER modules configured as QEC: Channel 12 (QEC0) to Channel 15 (QEC3)

In measurement mode, each UTIMER channel can capture the timing of internal events or external signal pulse edges. In counting mode, each channel can count external pulses, internal events, or decode quadrature pulse sequences.

As a signal generator, each UTIMER channel can be configured to produce PWM outputs with independent or complementary polarity and has the following main characteristics:

- Outputs configurable option to automatically insert dead-time suitable for power stages with asymmetric switching characteristics
- Multiple channels can be synchronized to drive three-phase inverters with variety of modulation schemes
- Driving up to 4 three-phase motors at once

Each QEC channel is a multifunctional counter with two inputs that can be configured to support different counting modes and an additional pin for zero signal used for reference run (zero-point calibration).

A QEC channel is intended to operate primarily as a decoder of a quadrature encoder pulse sequence. The input signals are passed through a digital filter to improve the noise immunity of the circuit. The count direction can be configured to depend on the phase difference between two signals (quadrature encoding) or on the level of one of them (pulse and direction encoding). Alternatively, one of the signals can be configured to increment and the other to decrement the timer counter values.

Each UTIMER channel supports the following main features:

- Clocked at high-resolution 400 MHz clock with 2.5 ns accuracy when generating a PWM output or when measuring input signal timing characteristics
- Dedicated digital inputs configurable as external synchronization sources or as fault signals that trigger automatic shut-off of the output drivers
- 32-bit wide counters and compare registers
- Double-buffered compare registers to support update of PWM duty cycle to occur upon several events, including at the middle or at the end of a PWM period. When buffer operation is enabled, it can be configured to use single or double stage.
- Up to 2 high-resolution PWM outputs with independent or complimentary polarity
- Support of capturing events placed closely together when the channel is configured as a pulse counter
- Capture and compare modes
- Compare registers dedicated to ADC synchronization—on a match they trigger ADC conversion, thus avoiding a power stage switching noise

- 8 interrupt events—some can be shared among channels to enable the implementation of complex state machines that can operate in a deterministic manner
- Configurable to use two I/O pins as inputs and to drive the two I/O pins

Each QEC channel has the following main features:

- 32-bit wide counters and compare registers
- Decoding quadrature encoder pulse sequence
- Counting in pulse/direction or increment/decrement modes
- Measurement of pulse width, period, or duty cycle
- Digital filter on the input signals for up to 32 peripheral clock cycles
- Generation of interrupts on two compare/match events
- Internal clock frequency up to 400 MHz
- External signals frequency up to 50 MHz

Table 3-10 presents UTIMER interface signals and provides descriptions to their functions.

Table 3-10 UTIMER Signal Descriptions

Signal Name	Pin Name	Type	Description
UTIMER0 A/B/C			
UT0_T0_A	P0_0	IO	UTIMER0 input event on channel A / output to driver A
UT0_T0_B	P5_0		
UT0_T0_C	P10_0		
UT0_T1_A	P0_1	IO	UTIMER0 input event on channel B / output to driver B
UT0_T1_B	P5_1		
UT0_T1_C	P10_1		
UTIMER1 A/B/C			
UT1_T0_A	P0_2	IO	UTIMER1 input event on channel A / output to driver A
UT1_T0_B	P5_2		
UT1_T0_C	P10_2		
UT1_T1_A	P0_3	IO	UTIMER1 input event on channel B / output to driver B
UT1_T1_B	P5_3		
UT1_T1_C	P10_3		
UTIMER2 A/B/C			
UT2_T0_A	P0_4	IO	UTIMER2 input event on channel A / output to driver A
UT2_T0_B	P5_4		
UT2_T0_C	P10_4		
UT2_T1_A	P0_5	IO	UTIMER2 input event on channel B / output to driver B
UT2_T1_B	P5_5		
UT2_T1_C	P10_5		
UTIMER3 A/B/C			
UT3_T0_A	P0_6	IO	UTIMER3 input event on channel A / output to driver A
UT3_T0_B	P5_6		
UT3_T0_C	P10_6		
UT3_T1_A	P0_7	IO	UTIMER3 input event on channel B / output to driver B
UT3_T1_B	P5_7		
UT3_T1_C	P10_7		
UTIMER4 A/B/C			
UT4_T0_A	P1_0	IO	UTIMER4 input event on channel A / output to driver A

Signal Name	Pin Name	Type	Description
UT4_T0_B	P6_0		
UT4_T0_C	P11_0		
UT4_T1_A	P1_1	IO	UTIMER4 input event on channel B / output to driver B
UT4_T1_B	P6_1		
UT4_T1_C	P11_1		
UTIMER5 A/B/C			
UT5_T0_A	P1_2	IO	UTIMER5 input event on channel A / output to driver A
UT5_T0_B	P6_2		
UT5_T0_C	P11_2		
UT5_T1_A	P1_3	IO	UTIMER5 input event on channel B / output to driver B
UT5_T1_B	P6_3		
UT5_T1_C	P11_3		
UTIMER6 A/B/C			
UT6_T0_A	P1_4	IO	UTIMER6 input event on channel A / output to driver A
UT6_T0_B	P6_4		
UT6_T0_C	P11_4		
UT6_T1_A	P1_5	IO	UTIMER6 input event on channel B / output to driver B
UT6_T1_B	P6_5		
UT6_T1_C	P11_5		
UTIMER7 A/B/C			
UT7_T0_A	P1_6	IO	UTIMER7 input event on channel A / output to driver A
UT7_T0_B	P6_6		
UT7_T0_C	P11_6		
UT7_T1_A	P1_7	IO	UTIMER7 input event on channel B / output to driver B
UT7_T1_B	P6_7		
UT7_T1_C	P11_7		
UTIMER8 A/B/C			
UT8_T0_A	P2_0	IO	UTIMER8 input event on channel A / output to driver A
UT8_T0_B	P7_0		
UT8_T0_C	P12_0		
UT8_T1_A	P2_1	IO	UTIMER8 input event on channel B / output to driver B
UT8_T1_B	P7_1		
UT8_T1_C	P12_1		
UTIMER9 A/B/C			
UT9_T0_A	P2_2	IO	UTIMER9 input event on channel A / output to driver A
UT9_T0_B	P7_2		
UT9_T0_C	P12_2		
UT9_T1_A	P2_3	IO	UTIMER9 input event on channel B / output to driver B
UT9_T1_B	P7_3		
UT9_T1_C	P12_3		
UTIMER10 A/B/C			
UT10_T0_A	P2_4	IO	UTIMER10 input event on channel A / output to driver A
UT10_T0_B	P7_4		
UT10_T0_C	P12_4		
UT10_T1_A	P2_5	IO	UTIMER10 input event on channel B / output to driver B

Signal Name	Pin Name	Type	Description
UT10_T1_B	P7_5		
UT10_T1_C	P12_5		
UTIMER11 A/B/C			
UT11_T0_A	P2_6	IO	UTIMER11 input event on channel A / output to driver A
UT11_T0_B	P7_6		
UT11_T0_C	P12_6		
UT11_T1_A	P2_7	IO	UTIMER11 input event on channel B / output to driver B
UT11_T1_B	P7_7		
UT11_T1_C	P12_7		

Table 3-11 presents UTIMER QEC interface signals and provides descriptions to their functions.

Table 3-11 UTIMER QEC Signal Descriptions

Signal Name	Pin Name	Type	Description
QEC0 A/B/C			
QEC0_X_A	P3_0	I	QEC0 input event on channel A
QEC0_X_B	P8_4		
QEC0_X_C	P13_0		
QEC0_Y_A	P3_1	I	QEC0 input event on channel B
QEC0_Y_B	P8_5		
QEC0_Y_C	P13_1		
QEC0_Z_A	P3_2	I	QEC0 input for zero signal
QEC0_Z_B	P8_6		
QEC0_Z_C	P13_2		
QEC1 A/B/C			
QEC1_X_A	P3_3	I	QEC1 input event on channel A
QEC1_X_B	P8_7		
QEC1_X_C	P13_3		
QEC1_Y_A	P3_4	I	QEC1 input event on channel B
QEC1_Y_B	P9_0		
QEC1_Y_C	P13_4		
QEC1_Z_A	P3_5	I	QEC1 input for zero signal
QEC1_Z_B	P9_1		
QEC1_Z_C	P13_5		
QEC2 A/B/C			
QEC2_X_A	P3_6	I	QEC2 input event on channel A
QEC2_X_B	P9_2		
QEC2_X_C	P13_6		
QEC2_Y_A	P3_7	I	QEC2 input event on channel B
QEC2_Y_B	P9_3		
QEC2_Y_C	P13_7		
QEC2_Z_A	P4_0	I	QEC2 input for zero signal
QEC2_Z_B	P9_4		
QEC2_Z_C	P14_0		
QEC3 A/B/C			

Signal Name	Pin Name	Type	Description
QEC3_X_A	P4_1	I	QEC3 input event on channel A
QEC3_X_B	P9_5		
QEC3_X_C	P14_1		
QEC3_Y_A	P4_2	I	QEC3 input event on channel B
QEC3_Y_B	P9_6		
QEC3_Y_C	P14_2		
QEC3_Z_A	P4_3	I	QEC3 input for zero signal
QEC3_Z_B	P9_7		
QEC3_Z_C	P14_3		

Table 3-12 presents UTIMER common interface signals and provides descriptions to their functions.

Table 3-12 UTIMER Common Signal Descriptions

Signal Name	Pin Name	Type	Description
Common A/B/C			
FAULT0_A	P4_4	I	Fault signal 0. Used to trigger automatic shut-off of the output drivers.
FAULT0_B	P8_0		
FAULT0_C	P14_4		
FAULT1_A	P4_5	I	Fault signal 1. Used to trigger automatic shut-off of the output drivers.
FAULT1_B	P8_1		
FAULT1_C	P14_5		
FAULT2_A	P4_6	I	Fault signal 2. Used to trigger automatic shut-off of the output drivers.
FAULT2_B	P8_2		
FAULT2_C	P14_6		
FAULT3_A	P4_7	I	Fault signal 3. Used to trigger automatic shut-off of the output drivers.
FAULT3_B	P8_3		
FAULT3_C	P14_7		

3.14.3 WDT_RTSS Overview

The Real-Time Subsystem Watchdog Timer module, hereinafter referred to as WDT_RTSS, is a timer based on a 32-bit down-counter. The basic function of the WDT_RTSS is to count for a fixed period, during which it expects to be serviced by the system, indicating normal operation. The WDT_RTSS provides a mechanism to detect errant system behavior and recover from an unknown state by causing Non-Maskable Interrupt (NMI) of the system if the count period elapses without intervention.

The device includes up to two WDT_RTSS modules:

- WDT_HP: Dedicated to the Arm Cortex-M55 High-Performance (M55-HP) processor
- WDT_HE: Dedicated to the Arm Cortex-M55 High-Efficiency (M55-HE) processor

The WDT_RTSS module supports the following main features:

- 32-bit down-counter
- Counter decrements by one on each positive watchdog clock edge
- Configurable NMI generation upon watch period expiration

3.14.4 LPRTC Overview

The Low-Power Real-Time Counter (LPRTC) module is a configurable high-range binary counter, which can generate an interrupt on a user-specified interval.

The device includes one LPRTC module located in the PD-0 power domain, allowing it to run even when the device is in the lowest power state and power is present on VDD_BATT.

The LPRTC module supports the following main features:

- 32.768 kHz typical reference clock
- 32-bit incrementing counter
- 16-bit programmable prescaler
- Interrupt generation upon programmed count match
- Counter wrap mode
- The LPRTC interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPRTC. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

The LPRTC module can be utilized for the following use cases:

- Real-time clock—to keep track of the current time
- Long-term exact chronometer—to keep track of time from now up to 136 years in the future (when clocked with a 1 Hz clock signal)
- Alarm function—to generate an interrupt after a programmed number of cycles
- Long time base counter—when clocked with a kHz range clock signal from either LFXO or LFRC

3.14.5 System Timers Overview

The system timer is composed of one counter and several timer modules. The counter provides count value to the timer modules, which generate interrupts when a certain timer condition is met.

The device includes two system timers – REFCLK_TMR and S32KCLK_TMR. The REFCLK_TMR system timer is clocked by SYST_REFCLK and has four timer modules – REFCLK_CNT_BASE[0-3]. The S32KCLK_TMR system timer is clocked by S32K_CLK and has two timer modules – S32KCLK_CNT_BASE[0-1].

Each system timer supports the following main features:

- Provides a uniform view of system time
- Provides 64-bit up counters and 32-bit down counters
- Has 64-bit wide counter and compare registers
- Supports virtual time by offsetting the real time via dedicated registers
- Can be incremented by larger amounts at a lower frequency (for example, increment by 4 at 4 times lower frequency)
- Has individual interrupt output for each timer module (CNT_BASEn)

3.15 General-Purpose Input/Output Module

The General-Purpose Input/Output (GPIO) module provides means for driving and reading from digital I/O pins when they are not used by other peripheral (like UART, I2C, etc.). GPIO module can be used for tasks like lighting LEDs or reading the state of push-buttons, switches, etc. The GPIO module also offers switch contact debounce and interrupt capabilities.

The device includes up to sixteen GPIO modules with support of up to 128 I/O pins in total. The I/O signals are distributed as follows:

- GPIO[0-14]: 8 I/O signals each
- LPGPIO: 8 I/O signals

The GPIO modules are integrated in two power domains:

- Power Domain PD-6: GPIO[0-14]
- Power Domain PD-0 (AON): LPGPIO

Each GPIO module supports the following main features:

- Data register allows driving and reading each GPIO pin individually
- Data Direction register selects pin direction – input or output
- Debounce function driven by the 32-k clock for switch/push-button contacts debouncing
- Individual interrupt generation for every pin of GPIO[0-14] and LPGPIO
- Common (combined) interrupt generation for the pin events of LPGPIO
- The LPGPIO interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPGPIO. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-13 presents GPIO interface signals and provides descriptions to their functions.

Table 3-13 GPIO Signal Descriptions

Signal Name	Pin Name	Type	Description
GPIO0			
GPIO0_0	P0_0	IO	General-purpose input/output(1)
GPIO0_1	P0_1	IO	General-purpose input/output(1)
GPIO0_2	P0_2	IO	General-purpose input/output(1)
GPIO0_3	P0_3	IO	General-purpose input/output(1)
GPIO0_4	P0_4	IO	General-purpose input/output(1)
GPIO0_5	P0_5	IO	General-purpose input/output(1)
GPIO0_6	P0_6	IO	General-purpose input/output(1)
GPIO0_7	P0_7	IO	General-purpose input/output(1)
GPIO1			
GPIO1_0	P1_0	IO	General-purpose input/output(1)
GPIO1_1	P1_1	IO	General-purpose input/output(1)
GPIO1_2	P1_2	IO	General-purpose input/output(1)
GPIO1_3	P1_3	IO	General-purpose input/output(1)

Signal Name	Pin Name	Type	Description
GPIO1_4	P1_4	IO	General-purpose input/output(1)
GPIO1_5	P1_5	IO	General-purpose input/output(1)
GPIO1_6	P1_6	IO	General-purpose input/output(1)
GPIO1_7	P1_7	IO	General-purpose input/output(1)
GPIO2			
GPIO2_0	P2_0	IO	General-purpose input/output(1)
GPIO2_1	P2_1	IO	General-purpose input/output(1)
GPIO2_2	P2_2	IO	General-purpose input/output(2)
GPIO2_3	P2_3	IO	General-purpose input/output(2)
GPIO2_4	P2_4	IO	General-purpose input/output(1)
GPIO2_5	P2_5	IO	General-purpose input/output(1)
GPIO2_6	P2_6	IO	General-purpose input/output(1)
GPIO2_7	P2_7	IO	General-purpose input/output(1)
GPIO3			
GPIO3_0	P3_0	IO	General-purpose input/output
GPIO3_1	P3_1	IO	General-purpose input/output
GPIO3_2	P3_2	IO	General-purpose input/output
GPIO3_3	P3_3	IO	General-purpose input/output
GPIO3_4	P3_4	IO	General-purpose input/output
GPIO3_5	P3_5	IO	General-purpose input/output
GPIO3_6	P3_6	IO	General-purpose input/output
GPIO3_7	P3_7	IO	General-purpose input/output
GPIO4			
GPIO4_0	P4_0	IO	General-purpose input/output
GPIO4_1	P4_1	IO	General-purpose input/output
GPIO4_2	P4_2	IO	General-purpose input/output
GPIO4_3	P4_3	IO	General-purpose input/output
GPIO4_4	P4_4	IO	General-purpose input/output
GPIO4_5	P4_5	IO	General-purpose input/output
GPIO4_6	P4_6	IO	General-purpose input/output
GPIO4_7	P4_7	IO	General-purpose input/output
GPIO5			
GPIO5_0	P5_0	IO	General-purpose input/output
GPIO5_1	P5_1	IO	General-purpose input/output
GPIO5_2	P5_2	IO	General-purpose input/output
GPIO5_3	P5_3	IO	General-purpose input/output
GPIO5_4	P5_4	IO	General-purpose input/output
GPIO5_5	P5_5	IO	General-purpose input/output
GPIO5_6	P5_6	IO	General-purpose input/output
GPIO5_7	P5_7	IO	General-purpose input/output
GPIO6			
GPIO6_0	P6_0	IO	General-purpose input/output
GPIO6_1	P6_1	IO	General-purpose input/output
GPIO6_2	P6_2	IO	General-purpose input/output
GPIO6_3	P6_3	IO	General-purpose input/output

Signal Name	Pin Name	Type	Description
GPIO6_4	P6_4	IO	General-purpose input/output
GPIO6_5	P6_5	IO	General-purpose input/output
GPIO6_6	P6_6	IO	General-purpose input/output
GPIO6_7	P6_7	IO	General-purpose input/output
GPIO7			
GPIO7_0	P7_0	IO	General-purpose input/output
GPIO7_1	P7_1	IO	General-purpose input/output
GPIO7_2	P7_2	IO	General-purpose input/output
GPIO7_3	P7_3	IO	General-purpose input/output
GPIO7_4	P7_4	IO	General-purpose input/output
GPIO7_5	P7_5	IO	General-purpose input/output
GPIO7_6	P7_6	IO	General-purpose input/output
GPIO7_7	P7_7	IO	General-purpose input/output
GPIO8			
GPIO8_0	P8_0	IO	General-purpose input/output
GPIO8_1	P8_1	IO	General-purpose input/output
GPIO8_2	P8_2	IO	General-purpose input/output
GPIO8_3	P8_3	IO	General-purpose input/output
GPIO8_4	P8_4	IO	General-purpose input/output
GPIO8_5	P8_5	IO	General-purpose input/output
GPIO8_6	P8_6	IO	General-purpose input/output
GPIO8_7	P8_7	IO	General-purpose input/output
GPIO9			
GPIO9_0	P9_0	IO	General-purpose input/output
GPIO9_1	P9_1	IO	General-purpose input/output
GPIO9_2	P9_2	IO	General-purpose input/output
GPIO9_3	P9_3	IO	General-purpose input/output
GPIO9_4	P9_4	IO	General-purpose input/output
GPIO9_5	P9_5	IO	General-purpose input/output
GPIO9_6	P9_6	IO	General-purpose input/output
GPIO9_7	P9_7	IO	General-purpose input/output
GPIO10			
GPIO10_0	P10_0	IO	General-purpose input/output
GPIO10_1	P10_1	IO	General-purpose input/output
GPIO10_2	P10_2	IO	General-purpose input/output
GPIO10_3	P10_3	IO	General-purpose input/output
GPIO10_4	P10_4	IO	General-purpose input/output
GPIO10_5	P10_5	IO	General-purpose input/output
GPIO10_6	P10_6	IO	General-purpose input/output
GPIO10_7	P10_7	IO	General-purpose input/output
GPIO11			
GPIO11_0	P11_0	IO	General-purpose input/output
GPIO11_1	P11_1	IO	General-purpose input/output
GPIO11_2	P11_2	IO	General-purpose input/output
GPIO11_3	P11_3	IO	General-purpose input/output

Signal Name	Pin Name	Type	Description
GPIO11_4	P11_4	IO	General-purpose input/output
GPIO11_5	P11_5	IO	General-purpose input/output
GPIO11_6	P11_6	IO	General-purpose input/output
GPIO11_7	P11_7	IO	General-purpose input/output
GPIO12			
GPIO12_0	P12_0	IO	General-purpose input/output
GPIO12_1	P12_1	IO	General-purpose input/output
GPIO12_2	P12_2	IO	General-purpose input/output
GPIO12_3	P12_3	IO	General-purpose input/output
GPIO12_4	P12_4	IO	General-purpose input/output
GPIO12_5	P12_5	IO	General-purpose input/output
GPIO12_6	P12_6	IO	General-purpose input/output
GPIO12_7	P12_7	IO	General-purpose input/output
GPIO13			
GPIO13_0	P13_0	IO	General-purpose input/output
GPIO13_1	P13_1	IO	General-purpose input/output
GPIO13_2	P13_2	IO	General-purpose input/output
GPIO13_3	P13_3	IO	General-purpose input/output
GPIO13_4	P13_4	IO	General-purpose input/output
GPIO13_5	P13_5	IO	General-purpose input/output
GPIO13_6	P13_6	IO	General-purpose input/output
GPIO13_7	P13_7	IO	General-purpose input/output
GPIO14			
GPIO14_0	P14_0	IO	General-purpose input/output
GPIO14_1	P14_1	IO	General-purpose input/output
GPIO14_2	P14_2	IO	General-purpose input/output
GPIO14_3	P14_3	IO	General-purpose input/output
GPIO14_4	P14_4	IO	General-purpose input/output
GPIO14_5	P14_5	IO	General-purpose input/output
GPIO14_6	P14_6	IO	General-purpose input/output
GPIO14_7	P14_7	IO	General-purpose input/output
LPGPIO			
GPIOV_0	P15_0	IO	Low-power general-purpose input/output
GPIOV_1	P15_1	IO	Low-power general-purpose input/output
GPIOV_2	P15_2	IO	Low-power general-purpose input/output
GPIOV_3	P15_3	IO	Low-power general-purpose input/output
GPIOV_4	P15_4	IO	Low-power general-purpose input/output
GPIOV_5	P15_5	IO	Low-power general-purpose input/output
GPIOV_6	P15_6	IO	Low-power general-purpose input/output
GPIOV_7	P15_7	IO	Low-power general-purpose input/output

1. Serves also as analog input. See Section 3.20.6 Analog Signals.
2. Serves also as analog input/output. See Section 3.20.6 Analog Signals.

3.16 Communication Peripherals

3.16.1 CANFD Overview

The Controller Area Network (CANFD) module performs serial communication according to the CAN protocol. The CAN bus interface uses the basic CAN principle and meets all constraints of the CAN Specification 2.0B active. The CANFD module supports both classic CAN and CAN with Flexible Data-rate (FD) specifications.

The device includes up to one CANFD module.

The CANFD module supports the following main features:

- CAN specifications:
  - CAN 2.0B (up to 8 bytes payload, verified by Bosch reference model)
  - CAN FD (up to 64 bytes payload, ISO 11898-1:2015 or non-ISO Bosch)
- Free programmable data rates:
  - Data rates up to 10 Mbps
  - CAN FD rates are limited by the transceiver and the clock frequency of the CAN controller
- Programmable baud rate prescaler (1 to 1/256)
- One receive buffer and two transmit buffers—primary transmit buffer (PTB) and secondary transmit buffer (STB):
  - Buffer size: 640 words
  - Number of buffer slots: 16
- 3× independent and programmable internal 29-bit acceptance filters
- Extended features:
  - Single Shot Transmission mode (for PTB and/or for STB)
  - Listen-Only mode
  - Loop Back mode (internal and external)
  - Transceiver Standby mode
- Extended status and error report:
  - Capturing of last occurred Kind Of Error (KOER) and arbitration lost position
  - Programmable Error Warning Limit
- 32-bit synchronous Host controller interfaces
- Configurable interrupt sources
- Dual port memory block for frame buffer
- CiA 603 32-bit timestamping
- Compatible with AUTOSAR
- Optimized for SAE J1939

Table 3-14 presents CANFD interface signals and provides descriptions to their functions.

Table 3-14 CANFD Signal Descriptions

Signal Name	Pin Name	Type	Description
CANFD A/B/C			
CAN_RXD_A	P7_0	I	CANFD serial data input (from external CAN transceiver)
CAN_RXD_B	P0_4		
CAN_RXD_C	P12_4		
CAN_TXD_A	P7_1	O	CANFD serial data output (to external CAN transceiver)
CAN_TXD_B	P0_5		
CAN_TXD_C	P12_5		
CAN_STBY_A	P7_3	O	CANFD transceiver standby mode signal
CAN_STBY_B	P0_6		

Signal Name	Pin Name	Type	Description
CAN_STBY_C	P12_6		

3.16.2 CRC Overview

The Cyclic Redundancy Check (CRC) calculation module can produce 8-, 16-, and 32-bit codes for variety of polynomials. This function is used to validate the integrity of a communication packet received or the integrity of a binary image that is an update candidate. This is achieved by computing and comparing the CRC code with the one received after the data packet transmission.

The device includes up to two CRC modules.

Each CRC module has the following main features:

- Built-in support for the following CRC algorithms:
  - CRC-8-CCITT
  - CRC-16
  - CRC-16-CCITT
  - CRC-32
  - CRC-32C
- Support of customized polynomials configured by register settings
- 8- or 32-bits of data processed at a time
- Configurable byte and bit swapping of data

3.16.3 ETH Overview

The Ethernet Controller (ETH) enables the device to transmit and receive data over Ethernet in compliance with IEEE 802.3-2008.

The device includes one ETH module.

The ETH module supports the following main features:

- Compliance with standards:
  - IEEE 1588-2008 standard for precision networked clock synchronization
  - RMII specification version 1.2 from RMII consortium
- MAC features:
  - 10 and 100 Mbps data transfer rates with RMII interface to communicate with an external fast Ethernet PHY
  - Full-duplex operation:
    - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion
    - Forwarding of received pause frames to the user application
  - Half-duplex operation:
    - CSMA/CD protocol support
    - Flow control using backpressure support
  - Preamble and Start of Frame Data (SFD) insertion in transmit path
  - Preamble and Start Frame Delimiter (SFD) deletion in the receive path
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Automatic pad and CRC stripping options for receive frames
  - Programmable frame length to support standard or jumbo Ethernet frames of up to 16KB
  - Programmable Interframe Gap (IFG) (40-bit to 96-bit times in steps of 8)
  - Transmit frames with reduced preamble size
  - Separate 32-bit status for transmit and receive packets

- IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces to the application
- Little-endian for transmit and receive paths
- 64-bit data transfer interface on system-side
- Detection of remote wake-up frames
- Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
- MDIO master interface for PHY device configuration and management
- Programmable watchdog timeout limit in the receive path

■ MAC Transaction Layer (MTL) features:
- 2KB transmit FIFO with programmable threshold
- 2KB receive FIFO with programmable threshold
- Single-channel transmit and receive engines
- Data transfers executed using simple FIFO protocol
- Optimization for packet-oriented transfers with frame delimiters
- Programmable burst length for starting a burst up to half the size of the MTL Rx and Tx FIFO
- Insertion of receive status vectors into the receive FIFO after the EOF transfer
- Store and forward mechanism for transmission to the MAC
- Automatic generation of pause frame control or backpressure signal to the MAC based on receive FIFO-fill (threshold configurable) level
- Automatic retransmission of collision frames for transmission
- Discard frames on late collision, excessive collisions, excessive deferral, and under-run conditions
- Software control to flush the transmit FIFO

■ DMA features:
- Exchanges data between the MTL block and system memory
- Single-channel transmit and receive engines
- Optimization for packet-oriented DMA transfers with frame delimiters
- Byte-aligned addressing for data buffer support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 8KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst size for transmit and receive DMA engines for optimal system bus utilization
- Programmable interrupt options for different operational conditions
- Per-frame transmit or receive complete interrupt control
- Round-robin or fixed-priority arbitration between receive and transmit engines

■ Monitoring and testing features:
- DMA states (Tx and Rx) as status bits
- Status registers that give status of FSMs in transmit and receive data-paths and FIFO fill levels
- Application abort status bits
- Current Tx/Rx buffer pointer as status registers
- Current Tx/Rx descriptor pointer as status registers

Table 3-15 presents Ethernet interface signals and provides descriptions to their functions.

Table 3-15 Ethernet Signal Descriptions

Signal Name	Pin Name	Type	Description
ETH A/B/C			

Signal Name	Pin Name	Type	Description
ETH_RXD0_A	P5_5	I	ETH PHY receive data bit 0
ETH_RXD0_B	P11_3		
ETH_RXD0_C	P1_0		
ETH_TXD0_A	P6_0	O	ETH PHY transmit data bit 0
ETH_TXD0_B	P10_4		
ETH_TXD0_C	P1_3		
ETH_RXD1_A	P5_6	I	ETH PHY receive data bit 1
ETH_RXD1_B	P11_4		
ETH_RXD1_C	P1_1		
ETH_TXD1_A	P6_1	O	ETH PHY transmit data bit 1
ETH_TXD1_B	P10_5		
ETH_TXD1_C	P1_4		
ETH_TXEN_A	P6_2	O	ETH PHY transmit data enable
ETH_TXEN_B	P10_6		
ETH_TXEN_C	P1_5		
ETH_CRS_DV_A	P6_7	I	ETH carrier sense/receive data valid
ETH_CRS_DV_B	P11_5		
ETH_CRS_DV_C	P2_2		
ETH_RST_A	P5_7	O	ETH reset to the external PHY module
ETH_RST_B	P11_6		
ETH_RST_C	P1_2		
ETH_IRQ_A	P6_3	I	ETH interrupt from the external PHY module
ETH_IRQ_B	P11_7		
ETH_IRQ_C	P1_6		
ETH_REFCLK_A	P6_4	IO	ETH 50-MHz reference clock
ETH_REFCLK_B	P11_0		
ETH_REFCLK_C	P1_7		
ETH_MDIO_A	P6_5	IO	ETH management data in/out
ETH_MDIO_B	P11_1		
ETH_MDIO_C	P2_0		
ETH_MDC_A	P6_6	O	ETH management data clock
ETH_MDC_B	P11_2		
ETH_MDC_C	P2_1		

3.16.4 I2C Overview

The Inter-Integrated Circuit (I2C) module is a synchronous, master/slave serial communication bus which is suitable for different system control applications.

The device includes:

- Up to four I2C modules in Shared Peripherals
- One Low-Power I2C (LPI2C) slave-only module in the RTSS-HE

The I2C modules support the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)

  - Fast Mode Plus (FM+) mode (up to 1 Mbps)
  - High Speed (HS) mode (up to 3.4 Mbps)
- Master or slave operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 32-byte deep receive and transmit FIFOs
- Bulk transmit mode
- Interrupt or polled-mode operation
- Bit and byte waiting at all bus speeds
- DMA handshaking interface
- Programmable SDA hold time
- Bus clear feature

The LPI2C module supports the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)
- Slave operation only
- 7-bit addressing only
- Hardcoded slave bus address (0x40)
- 8-byte deep inbound and outbound FIFOs
- Burst writes only (burst reads are not supported)
- Interrupt or polled-mode operation
- The LPI2C interrupt can be used as a wake-up source from STANDBY low-power mode

NOTE

All Low Power peripherals are single-master accessible, including LPI2C. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-16 presents I2C interface signals and provides descriptions to their functions.

Table 3-16 I2C Signal Descriptions

Signal Name	Pin Name	Type	Description
I2C0 A/B/C/D			
I2C0_SCL_A	P0_3	IO	I2C0 serial clock line. Open-drain output driver, requires external pull-up.
I2C0_SCL_B	P3_4		
I2C0_SCL_C	P7_1		
I2C0_SCL_D	P10_5		
I2C0_SDA_A	P0_2	IO	I2C0 serial data line. Open-drain output driver, requires external pull-up.
I2C0_SDA_B	P3_5		
I2C0_SDA_C	P7_0		
I2C0_SDA_D	P10_4		
I2C1 A/B/C/D			
I2C1_SCL_A	P0_5	IO	I2C1 serial clock line. Open-drain output driver, requires external pull-up.
I2C1_SCL_B	P3_7		

Signal Name	Pin Name	Type	Description
I2C1_SCL_C	P7_3		
I2C1_SCL_D	P10_7		
I2C1_SDA_A	P0_4	IO	I2C1 serial data line. Open-drain output driver, requires external pull-up.
I2C1_SDA_B	P3_6		
I2C1_SDA_C	P7_2		
I2C1_SDA_D	P10_6		
I2C2 A/B/C			
I2C2_SCL_A	P0_6	IO	I2C2 serial clock line. Open-drain output driver, requires external pull-up.
I2C2_SCL_B	P5_1		
I2C2_SCL_C	P5_6		
I2C2_SDA_A	P0_7	IO	I2C2 serial data line. Open-drain output driver, requires external pull-up.
I2C2_SDA_B	P5_0		
I2C2_SDA_C	P5_7		
I2C3 A/B/C			
I2C3_SCL_A	P1_1	IO	I2C3 serial clock line. Open-drain output driver, requires external pull-up.
I2C3_SCL_B	P9_7		
I2C3_SCL_C	P9_5		
I2C3_SDA_A	P1_0	IO	I2C3 serial data line. Open-drain output driver, requires external pull-up.
I2C3_SDA_B	P9_6		
I2C3_SDA_C	P9_4		
LPI2C A/B			
LPI2C_SCL_A	P7_4	I	LPI2C serial clock line. Slave-only, requires external pull-up.
LPI2C_SCL_B	P5_2		
LPI2C_SDA_A	P7_5	IO	LPI2C serial data line. Open-drain output driver, requires external pull-up.
LPI2C_SDA_B	P5_3		

3.16.5 I2S Overview

The Inter-IC Sound (I^2S™) is a low pin count, serial bus standard for a stereo audio data link between ADCs, DACs, CODECs, DSPs, and others. As the I^2S only handles the transfer of audio data, the control and sub-coding signals need to be transferred separately using a different bus interface (such as I^2C).

The device includes:

- Up to four I2S modules in Shared Peripherals
- One Low-Power I2S module (LPI2S) in the RTSS-HE

Each I2S module supports the following main features:

- I^2S transmitter and receiver based on the Philips I^2S serial protocol
- One stereo channel for transmitter and one for receiver
- Full duplex communication due to the independence of transmitter and receiver
- Master mode of operation
- Two input clock sources: 76.8 MHz or external audio clock
- 8, 16, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling frequencies
- 16, 24, or 32 clocks word-select cycles (left/right audio channel select)
- 12, 16, 20, 24, and 32 bits of audio data resolution
- FIFO depth of 16 words for each of receiver and transmitter
- Programmable FIFO thresholds

- DMA hardware handshaking interface
- 32-bit APB data bus

NOTE

All Low Power peripherals are single-master accessible, including LPI2S. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-17 presents I2S interface signals and provides descriptions to their functions.

Table 3-17 I2S Signal Descriptions

Signal Name	Pin Name	Type	Description
I2S0 A/B			
I2S0_SCLK_A	P3_0	O	I2S0 serial clock
I2S0_SCLK_B	P4_3		
I2S0_SDI_A	P1_6	I	I2S0 serial data input line
I2S0_SDI_B	P4_1		
I2S0_SDO_A	P1_7	O	I2S0 serial data output line
I2S0_SDO_B	P4_2		
I2S0_WS_A	P3_1	O	I2S0 word select line
I2S0_WS_B	P4_4		
I2S1 A/B			
I2S1_SCLK_A	P3_4	O	I2S1 serial clock
I2S1_SCLK_B	P12_2		
I2S1_SDI_A	P3_2	I	I2S1 serial data input line
I2S1_SDI_B	P12_0		
I2S1_SDO_A	P3_3	O	I2S1 serial data output line
I2S1_SDO_B	P12_1		
I2S1_WS_A	P4_0	O	I2S1 word select line
I2S1_WS_B	P12_3		
I2S2 A/B			
I2S2_SCLK_A	P8_3	O	I2S2 serial clock
I2S2_SCLK_B	P10_7		
I2S2_SDI_A	P8_1	I	I2S2 serial data input line
I2S2_SDI_B	P10_5		
I2S2_SDO_A	P8_2	O	I2S2 serial data output line
I2S2_SDO_B	P10_6		
I2S2_WS_A	P8_4	O	I2S2 word select line
I2S2_WS_B	P11_0		
I2S3 A/B			
I2S3_SCLK_A	P9_4	O	I2S3 serial clock
I2S3_SCLK_B	P8_6		
I2S3_SDI_A	P9_2	I	I2S3 serial data input line
I2S3_SDI_B	P9_0		

Signal Name	Pin Name	Type	Description
I2S3_SDO_A	P9_3	O	I2S3 serial data output line
I2S3_SDO_B	P9_1		
I2S3_WS_A	P9_5	O	I2S3 word select line
I2S3_WS_B	P8_7		
LPI2S A/B/C			
LPI2S_SCLK_A	P2_6	O	LPI2S serial clock
LPI2S_SCLK_B	P10_3		
LPI2S_SCLK_C	P13_6		
LPI2S_SDI_A	P2_4	I	LPI2S serial data input line
LPI2S_SDI_B	P10_1		
LPI2S_SDI_C	P13_4		
LPI2S_SDO_A	P2_5	O	LPI2S serial data output line
LPI2S_SDO_B	P10_2		
LPI2S_SDO_C	P13_5		
LPI2S_WS_A	P2_7	O	LPI2S word select line
LPI2S_WS_B	P10_4		
LPI2S_WS_C	P13_7		

3.16.6 I3C Overview

The MIPI Improved Inter-Integrated Circuit (I3C) provides an interface to external I3C devices.

The device includes one I3C module in Shared Peripherals.

The I3C module supports the following main features:

- Secondary Master function
- Data rates:
  - Fast Mode (FM) (up to 400 kbps)
  - Fast Mode Plus (FM+) (up to 1 Mbps)
  - Single Data Rate (SDR) (up to 10 Mbps)
  - High Data Rate—Double Data Rate (HDR-DDR) (up to 20 Mbps)
- Support for legacy I2C devices
- Separate command and data buffers for each of the transfers
- Buffer depths (each location can hold 4 bytes of data):
  - Commands buffer: 8 (16 locations)
  - Response buffer: 8 (8 locations)
  - Transmit and receive data buffers: 64 (64 locations) each
- Up to 2^{16} (65536) write/read bytes with a single command
- Hardware assisted Dynamic Address Assignment (DAA) support
- Hardware assisted device role switching between current master and slave
- Hot-Join support with user controllable filter
- CRC/parity generation and validation
- Broadcast and directed Common Command Code (CCC) transfers
- DMA support through hardware handshake interface
- Autonomous clock stalling
- Device address table for addressing multiple slaves
- Dedicated buffer for capturing information from ENTDAA CCC command

- Detects arbitration loss due to incoming In-Band Interrupt (IBI) and subsequently re-transmits the command
- Use of duty cycle to achieve lower effective speed for SDR transfers to work with slower I3C slaves
- Programmable Serial Data (SDA) transmit hold
- Programmable retry count for transfers that are addressed by slaves
- IBI with 16 locations of IBI status (no IBI payload)
- Defining Byte support for vendor specific broadcast and directed CCC transfers

Table 3-18 presents I3C interface signals and provides descriptions to their functions.

Table 3-18 I3C Signal Descriptions

Signal Name	Pin Name	Type	Description
I3C A/B/C/D			
I3C_SCL_A	P0_1	IO	I3C serial clock line
I3C_SCL_B	P1_3		
I3C_SCL_C	P3_3		
I3C_SCL_D	P7_7		
I3C_SDA_A	P0_0	IO	I3C serial data line
I3C_SDA_B	P1_2		
I3C_SDA_C	P3_2		
I3C_SDA_D	P7_6		

3.16.7 PDM Overview

The Pulse Density Modulation (PDM) module provides an interface to Digital Microphones (DMIC). The DMIC signal first gets amplified, and then sampled at a high rate and quantized by a DMIC's internal PDM modulator. The device PDM module provides clock and decodes the received 1-bit PDM stream into 16-bit values in Pulse Code Modulation (PCM) format.

The device includes:

- One PDM module in Shared Peripherals
- One Low-Power PDM module (LPPDM) in the RTSS-HE

Each PDM module supports the following main features:

- 4× 2-channel PDM microphone inputs for total support of up to 8 PDM channels (mono DMICs) for PDM module
- Audio signal bandwidth of up to 96 kHz
- DMA controller interface for storing audio samples
- 16-bit PCM output per channel
- Selection between 9 modes of PDM clock frequencies from 512 kHz to 4.8 MHz (oversampling). The mode applies to all channels.
- Microphone sleep mode when at 128 kHz PDM clock
- Independent phase adjustment per channel to allow beam forming
- Independent gain adjustment per channel
- Independent peak detector per channel with programmable thresholds
- Peak detection interrupt per channel producing wake-up event
- Independent programmable DC blocking Infinite Impulse Response (IIR) filter per channel
- Independent programmable Finite Impulse Response (FIR) filter per channel
- FIFO with a capability to store up to 8 PCM samples for each channel for CPU to read
- Programmable FIFO watermark level to generate *data available* interrupt
- FIFO overrun error interrupt

NOTE

All Low Power peripherals are single-master accessible, including LPPDM. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-19 presents PDM interface signals and provides descriptions to their functions.

Table 3-19 PDM Signal Descriptions

Signal Name	Pin Name	Type	Description
PDM A/B/C			
AUDIO_CLK_A	P8_0	I	PDM and I2S clock input
AUDIO_CLK_B	P9_6		
AUDIO_CLK_C	P12_0		
PDM_C0_A	P0_5	O	PDM clock output 0 to DMIC (shared between channels 0 and 1)
PDM_C0_B	P3_1		
PDM_C0_C	P6_1		
PDM_C1_A	P0_7	O	PDM clock output 1 to DMIC (shared between channels 2 and 3)
PDM_C1_B	P3_3		
PDM_C1_C	P6_3		
PDM_C2_A	P6_7	O	PDM clock output 2 to DMIC (shared between channels 4 and 5)
PDM_C2_B	P11_4		
PDM_C3_A	P5_2	O	PDM clock output 3 to DMIC (shared between channels 6 and 7)
PDM_C3_B	P11_5		
PDM_D0_A	P0_4	I	PDM data input 0 from DMIC (shared between channels 0 and 1)
PDM_D0_B	P3_0		
PDM_D0_C	P6_0		
PDM_D1_A	P0_6	I	PDM data input 1 from DMIC (shared between channels 2 and 3)
PDM_D1_B	P3_2		
PDM_D1_C	P6_2		
PDM_D2_A	P5_0	I	PDM data input 2 from DMIC (shared between channels 4 and 5)
PDM_D2_B	P5_4		
PDM_D3_A	P5_1	I	PDM data input 3 from DMIC (shared between channels 6 and 7)
PDM_D3_B	P5_5		
LPPDM A/B			
LPPDM_C0_A	P2_1	O	LPPDM clock output 0 to DMIC (shared between channels 0 and 1)
LPPDM_C0_B	P3_4		
LPPDM_C1_A	P2_3	O	LPPDM clock output 1 to DMIC (shared between channels 2 and 3)
LPPDM_C1_B	P3_6		
LPPDM_C2_A	P7_4	O	LPPDM clock output 2 to DMIC (shared between channels 4 and 5)
LPPDM_C2_B	P11_2		
LPPDM_C3_A	P7_6	O	LPPDM clock output 3 to DMIC (shared between channels 6 and 7)
LPPDM_C3_B	P11_3		
LPPDM_D0_A	P2_0	I	LPPDM data input 0 from DMIC (shared between channels 0 and 1)

Signal Name	Pin Name	Type	Description
LPPDM_D0_B	P3_5		
LPPDM_D1_A	P2_2	I	LPPDM data input 1 from DMIC (shared between channels 2 and 3)
LPPDM_D1_B	P3_7		
LPPDM_D2_A	P7_5	I	LPPDM data input 2 from DMIC (shared between channels 4 and 5)
LPPDM_D2_B	P11_6		
LPPDM_D3_A	P7_7	I	LPPDM data input 3 from DMIC (shared between channels 6 and 7)
LPPDM_D3_B	P11_7		

3.16.8 SPI Overview

The Serial Peripheral Interface (SPI) module is a programmable low pin count, full-duplex master or slave synchronous serial interface.

The device includes:

- Up to four high-speed SPI modules in Shared Peripherals
- One Low-Power SPI module (LPSPI) in the RTSS-HE

The SPI modules support the following main features:

- 32-bit data bus width for AHB interface (SPI modules) and APB interface (LPSPI module)
- Standard SPI mode
- Up to four slave select lines for the SPI modules, one slave select line for the LPSPI
- Multi-master contention detection
- Programmable delay on the sample time of received serial data bit for the high-speed SPI modules only (when programmed in Master mode)
- Separate Transmit and Receive FIFO buffers:
  - Buffer width of 32 bits
  - Buffer depth of 16 words
- DMA requests
- Combined interrupt lines and active high-level interrupts
- Operation modes:
  - Serial Master or Slave modes for the high-speed SPI modules
  - Master mode only for LPSPI
- Programmable frame formats:
  - Motorola Serial Peripheral Interface
  - Texas Instruments Synchronous Serial Protocol (SSP)
  - National Semiconductor Microwire
- Programmable data transfer clock bit rate for dynamic control of the serial bit rate
- Programmable data item size (4 to 32 bits) for each data transfer

NOTE

All Low Power peripherals are single-master accessible, including LPSPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-20 presents SPI interface signals and provides descriptions to their functions.

Table 3-20 SPI Signal Descriptions

Signal Name	Pin Name	Type	Description
SPI0 A/B/C			
SPI0_SCLK_A	P1_2	IO	SPI0 serial clock (driven by master)
SPI0_SCLK_B	P5_3		
SPI0_SCLK_C	P7_2		
SPI0_SS0_A	P1_3	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI0_SS0_B	P5_2		
SPI0_SS0_C	P7_3		
SPI0_SS1_A	P1_4	O	SPI0 slave select 1 (driven by master)
SPI0_SS1_B	P3_5		
SPI0_SS2_A	P1_5	O	SPI0 slave select 2 (driven by master)
SPI0_SS2_B	P3_6		
SPI0_SS3_A	P5_4	O	SPI0 slave select 3 (driven by master)
SPI0_SS3_B	P8_2		
SPI0_MISO_A	P1_0	IO	SPI0 master in slave out
SPI0_MISO_B	P5_0		
SPI0_MISO_C	P7_0		
SPI0_MOSI_A	P1_1	IO	SPI0 master out slave in
SPI0_MOSI_B	P5_1		
SPI0_MOSI_C	P7_1		
SPI1 A/B/C			
SPI1_SCLK_A	P2_6	IO	SPI1 serial clock (driven by master)
SPI1_SCLK_B	P8_5		
SPI1_SCLK_C	P14_6		
SPI1_SS0_A	P2_7	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI1_SS0_B	P6_4		
SPI1_SS0_C	P14_7		
SPI1_SS1_A	P3_7	O	SPI1 slave select 1 (driven by master)
SPI1_SS1_B	P6_5		
SPI1_SS2_A	P4_0	O	SPI1 slave select 2 (driven by master)
SPI1_SS2_B	P6_6		
SPI1_SS3_A	P4_1	O	SPI1 slave select 3 (driven by master)
SPI1_SS3_B	P6_7		
SPI1_MISO_A	P2_4	IO	SPI1 master in slave out
SPI1_MISO_B	P8_3		
SPI1_MISO_C	P14_4		
SPI1_MOSI_A	P2_5	IO	SPI1 master out slave in
SPI1_MOSI_B	P8_4		
SPI1_MOSI_C	P14_5		
SPI2 A/B			
SPI2_SCLK_A	P4_4	IO	SPI2 serial clock (driven by master)
SPI2_SCLK_B	P9_4		
SPI2_SS0_A	P4_5	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI2_SS0_B	P9_5		
SPI2_SS1_A	P4_6	O	SPI2 slave select 1 (driven by master)

Signal Name	Pin Name	Type	Description
SPI2_SS1_B	P9_6		
SPI2_SS2_A	P4_7	O	SPI2 slave select 2 (driven by master)
SPI2_SS2_B	P9_7		
SPI2_SS3_A	P13_3	O	SPI2 slave select 3 (driven by master)
SPI2_SS3_B	P10_0	O	SPI2 slave select 3 (driven by master)
SPI2_MISO_A	P4_2	IO	SPI2 master in slave out
SPI2_MISO_B	P9_2		
SPI2_MOSI_A	P4_3	IO	SPI2 master out slave in
SPI2_MOSI_B	P9_3		
SPI3 A/B			
SPI3_SCLK_A	P12_6	IO	SPI3 serial clock (driven by master)
SPI3_SCLK_B	P10_7	IO	SPI3 serial clock (driven by master)
SPI3_SS0_A	P12_7	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI3_SS0_B	P11_0		
SPI3_SS1_A	P13_0	O	SPI3 slave select 1 (driven by master)
SPI3_SS1_B	P11_1	O	SPI3 slave select 1 (driven by master)
SPI3_SS2_A	P13_1	O	SPI3 slave select 2 (driven by master)
SPI3_SS2_B	P11_2	O	SPI3 slave select 2 (driven by master)
SPI3_SS3_A	P13_2	O	SPI3 slave select 3 (driven by master)
SPI3_SS3_B	P11_3	O	SPI3 slave select 3 (driven by master)
SPI3_MISO_A	P12_4	IO	SPI3 master in slave out
SPI3_MISO_B	P10_5	IO	SPI3 master in slave out
SPI3_MOSI_A	P12_5	IO	SPI3 master out slave in
SPI3_MOSI_B	P10_6	IO	SPI3 master out slave in
LPSPI A/B			
LPSPI_SCLK_A	P7_6	IO	LPSPI serial clock (driven by master)
LPSPI_SCLK_B	P11_6		
LPSPI_MISO_A	P7_4	IO	LPSPI master in slave out
LPSPI_MISO_B	P11_4		
LPSPI_MOSI_A	P7_5	IO	LPSPI master out slave in
LPSPI_MOSI_B	P11_5		
LPSPI_SS_A	P7_7	IO	LPSPI slave select output
LPSPI_SS_B	P11_7		

3.16.9 UART Overview

The Universal Asynchronous Receiver/Transmitter (UART) module implements asynchronous serial communication interface based on standard Non-Return-to-Zero (NRZ) frame format.

The device includes:

- Up to eight UART modules in Shared Peripherals
- One Low-Power UART module (LPUART) in the RTSS-HE
- One UART module in the SESS (SEUART)—not accessible by user application

The UART modules are integrated in the following power domains:

- Power Domain PD-6: UART[0-7]
- Power Domain PD-2: LPUART

- Power Domain PD-5: SEUART

Each UART module supports the following main features:

- Full duplex operation
- Programmable baud rates up to 2.5 Mbps with a fractional baud rate divisor
- Interrupt driven or DMA controlled data transfer
- Auto flow control compatible with 16750 devices
- Configurable character length—5, 6, 7, 8 or 9 bits
- Optional parity bit—Even, Odd, Stick
- Number of stop bits—1, 1.5, 2 bits
- Line break generation and detection
- CTS/RTS signals for hardware flow control
- Drive enable output for RS485 interface support on UART[4-7] only
- Transmit (Tx) and Receive (Rx) FIFO depth of 32 characters
- Loopback mode for test and troubleshooting
- False start bit detection
- Compatible with the industry standard 16550 devices
- The LPUART interrupt can be used as a wake-up source from STANDBY low-power mode

NOTE

All Low Power peripherals are single-master accessible, including LPUART. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-21 presents UART interface signals and provides descriptions to their functions.

Table 3-21 UART Signal Descriptions

Signal Name	Pin Name	Type	Description
UART0 A/B			
UART0_RX_A	P0_0	I	UART0 serial data input
UART0_RX_B	P1_4		
UART0_TX_A	P0_1	O	UART0 serial data output
UART0_TX_B	P1_5		
UART0_CTS_A	P0_2	I	UART0 clear to send
UART0_CTS_B	P6_6		
UART0_RTS_A	P0_3	O	UART0 request to send
UART0_RTS_B	P6_7		
UART1 A/B			
UART1_RX_A	P0_4	I	UART1 serial data input
UART1_RX_B	P1_6		
UART1_TX_A	P0_5	O	UART1 serial data output
UART1_TX_B	P1_7		
UART1_CTS_A	P0_6	I	UART1 clear to send
UART1_CTS_B	P5_6		
UART1_RTS_A	P0_7	O	UART1 request to send
UART1_RTS_B	P5_7		

Signal Name	Pin Name	Type	Description
UART2 A/B			
UART2_RX_A	P1_0	I	UART2 serial data input
UART2_RX_B	P2_0		
UART2_TX_A	P1_1	O	UART2 serial data output
UART2_TX_B	P2_1		
UART2_CTS_A	P6_2	I	UART2 clear to send
UART2_CTS_B	P6_4		
UART2_RTS_A	P6_3	O	UART2 request to send
UART2_RTS_B	P6_5		
UART3 A/B			
UART3_RX_A	P1_2	I	UART3 serial data input
UART3_RX_B	P2_2		
UART3_TX_A	P1_3	O	UART3 serial data output
UART3_TX_B	P2_3		
UART3_CTS_A	P5_4	I	UART3 clear to send
UART3_CTS_B	P7_2		
UART3_RTS_A	P5_5	O	UART3 request to send
UART3_RTS_B	P7_3		
UART4 A/B/C			
UART4_RX_A	P3_0	I	UART4 serial data input
UART4_RX_B	P12_1		
UART4_RX_C	P5_0		
UART4_TX_A	P3_1	O	UART4 serial data output
UART4_TX_B	P12_2		
UART4_TX_C	P5_1		
UART4_DE_A	P6_0	O	UART4 RS485 driver enable
UART4_DE_B	P12_3		
UART5 A/B/C			
UART5_RX_A	P3_4	I	UART5 serial data input
UART5_RX_B	P11_3		
UART5_RX_C	P5_2		
UART5_TX_A	P3_5	O	UART5 serial data output
UART5_TX_B	P11_4		
UART5_TX_C	P5_3		
UART5_DE_A	P6_1	O	UART5 RS485 driver enable
UART5_DE_B	P11_7		
UART6 A/B/C			
UART6_RX_A	P10_5	I	UART6 serial data input
UART6_RX_B	P11_5		
UART6_RX_C	P14_0		
UART6_TX_A	P10_6	O	UART6 serial data output
UART6_TX_B	P11_6		
UART6_TX_C	P14_1		
UART6_DE_A	P11_2	O	UART6 RS485 driver enable
UART6_DE_B	P10_0		

Signal Name	Pin Name	Type	Description
UART7 A/B/C			
UART7_RX_A	P10_7	I	UART7 serial data input
UART7_RX_B	P9_3		
UART7_RX_C	P14_2		
UART7_TX_A	P11_0	O	UART7 serial data output
UART7_TX_B	P9_4		
UART7_TX_C	P14_3		
UART7_DE_A	P11_1	O	UART7 RS485 driver enable
UART7_DE_B	P9_7		
LPUART A/B			
LPUART_RX_A	P7_6	I	LPUART serial data input
LPUART_RX_B	P9_1		
LPUART_TX_A	P7_7	O	LPUART serial data output
LPUART_TX_B	P9_2		
LPUART_CTS_A	P7_4	I	LPUART clear to send
LPUART_CTS_B	P3_6		
LPUART_RTS_A	P7_5	O	LPUART request to send
LPUART_RTS_B	P3_7		
SEUART			
SEUART_RX	SEUART_RX	I	SEUART serial data input
SEUART_TX	SEUART_TX	O	SEUART serial data output

3.16.10 USB Overview

The Universal Serial Bus (USB) provides an expandable, bi-directional, hot-pluggable, serial interface that allows to plug different peripherals into a USB port and have them automatically configured and ready to use. USB host and devices use memory FIFO buffers to implement data endpoints used to accept or send data from and to its endpoint counterpart.

The device includes one USB module. The USB module consists of an xHCI USB2.0 Dual-Role Device (DRD) controller, a FIFO RAM, and an on-chip PHY.

The USB module supports the following main features:

- Compliant with USB Specification 2.0
- Four bi-directional endpoints including the bi-directional control endpoint 0
- Same programming model for Low-Speed (LS) (1.5 Mbit/s, host mode only), Full-Speed (FS) (12 Mbit/s), and High-Speed (HS) (480 Mbit/s) bit rates
- Internal DMA controller
- Power-saving features (clock gating)
- Link Power Management (LPM) protocol
- Hardware-controlled LPM support in Host mode
- Single 1865 × 64-bit RAM, accommodating registers, descriptor cache, Rx buffers and Tx prefetch
  - Dynamic FIFO memory allocation for endpoints
- Keep-alive feature in LS mode and (micro-)SOFs in FS and HS modes
- (micro-)SOFs (Start-of-Frame)
- Software-controlled standard USB commands (USB SETUP commands detected and forwarded to application for decoding)
- Hardware-controlled USB bus level and packet level error handling

- Low CPU utilization needs
  - Driver involved only in setting up transfers and high-level error recovery
  - Hardware handles data packing and routing to a specific pipe
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- On-chip PHY via an USB 2.0 Transceiver Macrocell Interface (UTMI+)

Table 3-22 presents USB interface signals and provides descriptions to their functions.

Table 3-22 USB Signal Descriptions

Signal Name	Pin Name	Type	Description
USB_DP	USB_DP	IO	USB 2.0 differential data (positive)
USB_DM	USB_DM	IO	USB 2.0 differential data (negative)
USB_VBUS	USB_VBUS	A	USB V_{BUS}-sense input
USB_IO_ID	USB_IO_ID	A	USB A/B-device detect—leave unconnected (Device) or tie to ground (Host)
USB_REXT	USB_REXT	P	External calibration resistor (200 Ω ±1%) to GND

3.17 External Memory Interfaces

3.17.1 Cryptographic OSPI Overview

The cryptographic OSPI implementation in the device consists of the Octal Serial Peripheral Interface (OSPI) module and the ancillary Advanced Encryption Standard (AES) engine.

The OSPI is an intelligent peripheral offering various memory expansion options. The OSPI can work either in a direct access mode to directly read and write data to the external SPI memory, or in a decryption mode where the incoming data is decrypted on-the-fly via the AES engine.

The device includes up to two OSPI modules, each assisted by a dedicated AES engine for the cryptographic operations.

Each OSPI module supports the following main features:

- Single, Dual, Quad, or Octal SPI Master mode operation
- Up to 100 MHz clock for up to 100 MB/s Single Data Rate (SDR) and 200 MB/s Dual Data Rate (DDR) support
- HyperBus protocol support for integration of HyperRAM™ modules
- Programmable instruction length, address length, wait cycles and data frame size
- Programmable option to skip address and instruction phase
- Read data strobe support in DDR mode for higher frequencies
- Support of Motorola Serial Peripheral Interface protocol
- DMA controller interface
- Programmable delay on the sample time of Received Serial Data (RXD) bit compensating routing delays
- Programmable frame size of each data transfer from 4 to 32 bits
- 256 words deep Rx and Tx FIFO buffers
- Execute-in-Place (XIP) support for read and write transfers—translates memory access requests to SPI transactions for code memory expansion. This mode supports the following main features:
  - Programmable instruction length and address length in XIP mode
  - Data frame size mapping directly from AHB transfers
  - Fixed data frame size for all the transfers
  - Continuous transfer mode for read transactions
  - Data mask support

  - Configurable data pre-fetch during XIP read transaction
  - Concurrent XIP and non-XIP transactions
- eXpanded SPI (xSPI) with all the command formats as described in JEDEC xSPI version 1.0
- Two xSPI command modes:
  - 1S-1S-1S—one IO signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
  - 8D-8D-8D—eight IO signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.

Each AES engine supports the following main features:

- On-the-fly decryption, transparent for the OSPI read transactions from external memory
- Electronic Codebook (ECB) mode of operation

  In general, a given OSPI instance (OSPI0 or OSPI1) should only be configured and used by either the RTSS-HP (Cortex-M55 HP core) or the RTSS-HE (Cortex-M55 HE core).
- 128-bit long AES keys
- Secure setup and lockup of the decryption keys by the Secure Enclave at boot time

Table 3-23 presents OSPI interface signals and provides descriptions to their functions.

CAUTION

The following pin multiplexing options are recommended:

- For OSPI0, the OSPI0_D[0-7]_B data bus signals are recommended to be used for 100 MHz operation. OSPI0_D[0-7]_A and OSPI0_D[0-7]_C data bus signals are recommended to be used for 50 MHz operation.

- For OSPI1, the OSPI1_D[0-7]_C data bus signals are recommended to be used for 100 MHz operation. OSPI1_D[0-7]_A and OSPI1_D[0-7]_B data bus signals are recommended to be used for 50 MHz operation.

Table 3-23 OSPI Signal Descriptions

Signal Name	Pin Name	Type	Description
OSPI0 Data Bus A/B/C			
OSPI0_D0_A	P0_0	IO	OSPI0 data input/output 0 in enhanced SPI modes. Data output (MOSI) in standard SPI mode.
OSPI0_D0_B	P2_0		
OSPI0_D0_C	P6_0		
OSPI0_D1_A	P0_1	IO	OSPI0 data input/output 1 in enhanced SPI modes. Data input (MISO) in standard SPI mode.
OSPI0_D1_B	P2_1		
OSPI0_D1_C	P6_1		
OSPI0_D2_A	P0_2	IO	OSPI0 data 2
OSPI0_D2_B	P2_2		
OSPI0_D2_C	P6_2		
OSPI0_D3_A	P0_3	IO	OSPI0 data 3
OSPI0_D3_B	P2_3		
OSPI0_D3_C	P6_3		
OSPI0_D4_A	P0_4	IO	OSPI0 data 4
OSPI0_D4_B	P2_4		
OSPI0_D4_C	P6_4		

Signal Name	Pin Name	Type	Description
OSPI0_D5_A	P0_5	IO	OSPI0 data 5
OSPI0_D5_B	P2_5		
OSPI0_D5_C	P6_5		
OSPI0_D6_A	P0_6	IO	OSPI0 data 6
OSPI0_D6_B	P2_6		
OSPI0_D6_C	P6_6		
OSPI0_D7_A	P0_7	IO	OSPI0 data 7
OSPI0_D7_B	P2_7		
OSPI0_D7_C	P6_7		
OSPI0 Clock, Slave Select, Data Strobe A/B/C			
OSPI0_SCLKN_A	P3_5	O	OSPI0 serial clock (negative)
OSPI0_SCLKN_B	P3_1		
OSPI0_SCLKN_C	P12_1		
OSPI0_SCLK_A	P1_7	O	OSPI0 serial clock
OSPI0_SCLK_B	P3_0		
OSPI0_SCLK_C	P12_0		
OSPI0_RXDS_A	P3_4	IO	OSPI0 read data strobe (RXDS) when input. Data mask (TXD_DM) when output.
OSPI0_RXDS_B	P1_6		
OSPI0_RXDS_C	P12_2		
OSPI0_SS0_A	P1_4	O	OSPI0 slave select 0
OSPI0_SS0_B	P3_2		
OSPI0_SS0_C	P12_3		
OSPI0_SS1_A	P1_5	O	OSPI0 slave select 1
OSPI0_SS1_B	P3_3		
OSPI0_SS1_C	P12_4		
OSPI1 Data Bus A/B/C			
OSPI1_D0_A	P11_0	IO	OSPI1 data input/output 0 in enhanced SPI modes. Data output (MOSI) in standard SPI mode.
OSPI1_D0_B	P13_0		
OSPI1_D0_C	P9_5		
OSPI1_D1_A	P11_1	IO	OSPI1 data input/output 1 in enhanced SPI modes. Data input (MISO) in standard SPI mode.
OSPI1_D1_B	P13_1		
OSPI1_D1_C	P9_6		
OSPI1_D2_A	P11_2	IO	OSPI1 data 2
OSPI1_D2_B	P13_2		
OSPI1_D2_C	P9_7		
OSPI1_D3_A	P11_3	IO	OSPI1 data 3
OSPI1_D3_B	P13_3		
OSPI1_D3_C	P10_0		
OSPI1_D4_A	P11_4	IO	OSPI1 data 4
OSPI1_D4_B	P13_4		
OSPI1_D4_C	P10_1		
OSPI1_D5_A	P11_5	IO	OSPI1 data 5
OSPI1_D5_B	P13_5		
OSPI1_D5_C	P10_2		
OSPI1_D6_A	P11_6	IO	OSPI1 data 6

Signal Name	Pin Name	Type	Description
OSPI1_D6_B	P13_6		
OSPI1_D6_C	P10_3		
OSPI1_D7_A	P11_7	IO	OSPI1 data 7
OSPI1_D7_B	P13_7		
OSPI1_D7_C	P10_4		
OSPI1 Clock, Slave Select, Data Strobe A/B/C			
OSPI1_SCLKN_A	P5_2	O	OSPI1 serial clock (negative)
OSPI1_SCLKN_B	P14_1		
OSPI1_SCLKN_C	P8_0		
OSPI1_SCLK_A	P5_3	O	OSPI1 serial clock
OSPI1_SCLK_B	P14_0		
OSPI1_SCLK_C	P5_5		
OSPI1_RXDS_A	P5_0	IO	OSPI1 read data strobe (RXDS) when input. Data mask (TXD_DM) when output.
OSPI1_RXDS_B	P12_7		
OSPI1_RXDS_C	P10_7		
OSPI1_SS0_A	P5_1	O	OSPI1 slave select 0
OSPI1_SS0_B	P14_2		
OSPI1_SS0_C	P5_7		
OSPI1_SS1_A	P5_4	O	OSPI1 slave select 1
OSPI1_SS1_B	P14_3		

3.17.2 SDMMC Overview

The Secure Digital / MultiMediaCard (SDMMC) module provides an interface to embedded MultiMediaCard (eMMC™), Secure Digital® (SD®) card, and SD Input/Output (SDIO). The communication between the SDMMC module and eMMC/SD/SDIO device is performed according to the eMMC/SD/SDIO protocol.

The device includes one SDMMC module.

The SDMMC module supports the following main features:

- SD card interface:
  - 4-bit data bus
  - Complaint with SD Host Controller Standard Specification v4.20
  - Complaint with SD Physical Layer Specification v6.00
  - Backward compatible with earlier SD card specifications
  - UHS-I mode
  - Speed modes:
    - Default-Speed (DS)
    - High-Speed (HS)
    - SDR12
    - SDR25
    - SDR50
- SDIO interface:
  - 4-bit data bus
  - Complaint with SD Specifications Part E1 SDIO Specification Version 4.10
  - SDIO read wait
  - SDIO card interrupts in both 1-bit and 4-bit modes
  - Wake-up on card interrupt

- eMMC interface:
  - 4-bit/8-bit data bus
  - Complaint with JEDEC eMMC 5.1 Specification (JESD84-B51)
  - Backward compatible with earlier eMMC specifications
  - Speed legacy modes:
    - High Speed SDR
  - Boot operation and alternative boot operation
- 32-bit slave AHB and master AXI interface
- Data transfer types for SD and eMMC:
  - CPU
  - SDMA
  - ADMA2
  - ADMA3
- Clocking:
  - Supports independent clocks for the host controller, slave interface, and master interface
  - Supports gating of host controller base clock, if host controller is inactive
  - Supports context aware functional clock gates
- Interrupt outputs:
  - Combined and separate interrupt outputs
  - Interrupt enabling and masking
- Data buffering:
  - Automatic packing/unpacking of data to fit buffer width

Table 3-24 presents SDMMC interface signals and provides descriptions to their functions.

CAUTION

The following pin multiplexing options are recommended:

For SDMMC, the SD_*_C signals are recommended to be used for 50 MHz operation. SD_*_A, SD_*_B, and SD_*_D signals are recommended to be used for 25 MHz operation.

Table 3-24 SDMMC Signal Descriptions

Signal Name	Pin Name	Type	Description
SDMMC Data Bus A/B/C/D			
SD_D0_A	P5_0	IO	SDMMC data line 0
SD_D0_B	P13_0		
SD_D0_C	P8_0		
SD_D0_D	P6_0		
SD_D1_A	P5_1	IO	SDMMC data line 1
SD_D1_B	P13_1		
SD_D1_C	P8_1		
SD_D1_D	P6_1		
SD_D2_A	P5_2	IO	SDMMC data line 2
SD_D2_B	P13_2		
SD_D2_C	P8_2		
SD_D2_D	P6_2		
SD_D3_A	P5_3	IO	SDMMC data line 3

Signal Name	Pin Name	Type	Description
SD_D3_B	P13_3		
SD_D3_C	P8_3		
SD_D3_D	P6_3		
SD_D4_A	P5_4	IO	SDMMC data line 4
SD_D4_B	P13_4		
SD_D4_C	P8_4		
SD_D4_D	P6_4		
SD_D5_A	P5_5	IO	SDMMC data line 5
SD_D5_B	P13_5		
SD_D5_C	P8_5		
SD_D5_D	P6_5		
SD_D6_A	P5_6	IO	SDMMC data line 6
SD_D6_B	P13_6		
SD_D6_C	P8_6		
SD_D6_D	P6_6		
SD_D7_A	P5_7	IO	SDMMC data line 7
SD_D7_B	P13_7		
SD_D7_C	P8_7		
SD_D7_D	P6_7		
SDIO Command, Clock, Reset A/B/C/D			
SD_CMD_A	P7_0	IO	SDMMC command/response line
SD_CMD_B	P14_0	IO	SDMMC command/response line
SD_CMD_C	P9_0	IO	SDMMC command/response line
SD_CMD_D	P4_2	IO	SDMMC command/response line
SD_CLK_A	P7_1	O	SDMMC host to card clock line
SD_CLK_B	P14_1	O	SDMMC host to card clock line
SD_CLK_C	P9_1	O	SDMMC host to card clock line
SD_CLK_D	P4_1	O	SDMMC host to card clock line
SD_RST_A	P7_2	O	SDMMC reset line (for eMMC devices)
SD_RST_B	P14_2	O	SDMMC reset line (for eMMC devices)
SD_RST_C	P9_2	O	SDMMC reset line (for eMMC devices)
SD_RST_D	P4_3	O	SDMMC reset line (for eMMC devices)

3.18 Camera Interfaces

3.18.1 CPI Overview

The digital Camera Parallel Interface (CPI) enables pixel data reception from external CMOS sensors and camera modules, or from the internal MIPI CSI controller. The data transfer rate is limited by the maximum supported pixel clock and data bus width.

The device includes:

- One CPI controller in Shared Peripherals. The CPI receives parallel data from either of the following sources:
  - External camera sensor (up to 16-bit data bus)
  - Internal MIPI CSI controller (16-bit or 48-bit IPI data bus)

- One Low-Power CPI (LPCPI) controller in the RTSS-HE. The LPCPI receives parallel data from an external camera sensor (up to 8-bit data bus).

Each CPI controller supports the following main features:

- Up to 60 MHz pixel clock
- Programmable polarity for the pixel clock, horizontal and vertical synchronization signals
- Single frame capture snapshot mode only (automated streaming mode is not supported)
- Pixel clock output to external camera sensor

Each CPI controller supports the following specific features depending on the pixel data source and bus width:

- External camera sensor source:
  - Data modes: 1-, 2-, 4-, 8-bit (CPI and LPCPI), and 16-bit (CPI only)
  - Data mask for 16-bit data mode (CPI only)
  - Programmable MSB/LSB selection
  - Transfer 10-bit pixel encoding over 8-bit wide data bus
- MIPI CSI controller source:
  - Data modes: 8-, 16-, 32-, 64-bit
  - Halt function to prevent FIFO overflow

NOTE

All Low Power peripherals are single-master accessible, including LPCPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-25 presents CPI interface signals and provides descriptions to their functions.

CAUTION

- For CAM_PCLK and CAM_XVCLK signals, recommended to be used are CAM_PCLK_B and CAM_ XVCLK_B pin multiplexing options.

Table 3-25 CPI Signal Descriptions

Signal Name	Pin Name	Type	Description
CPI Data Bus A/B			
CAM_D0_A	P2_4	I	CPI pixel data from external camera sensor bit [0]
CAM_D0_B	P8_0		
CAM_D1_A	P2_5	I	CPI pixel data from external camera sensor bit [1]
CAM_D1_B	P8_1		
CAM_D2_A	P2_6	I	CPI pixel data from external camera sensor bit [2]
CAM_D2_B	P8_2		
CAM_D3_A	P2_7	I	CPI pixel data from external camera sensor bit [3]
CAM_D3_B	P8_3		
CAM_D4_A	P3_0	I	CPI pixel data from external camera sensor bit [4]
CAM_D4_B	P8_4		

Signal Name	Pin Name	Type	Description
CAM_D5_A	P3_1	I	CPI pixel data from external camera sensor bit [5]
CAM_D5_B	P8_5		
CAM_D6_A	P3_2	I	CPI pixel data from external camera sensor bit [6]
CAM_D6_B	P8_6		
CAM_D7_A	P3_3	I	CPI pixel data from external camera sensor bit [7]
CAM_D7_B	P8_7		
CAM_D8_A	P3_4	I	CPI pixel data from external camera sensor bit [8]
CAM_D8_B	P9_0		
CAM_D9_A	P3_5	I	CPI pixel data from external camera sensor bit [9]
CAM_D9_B	P9_1		
CAM_D10_A	P3_6	I	CPI pixel data from external camera sensor bit [10]
CAM_D10_B	P9_2		
CAM_D11_A	P3_7	I	CPI pixel data from external camera sensor bit [11]
CAM_D11_B	P9_3		
CAM_D12_A	P4_0	I	CPI pixel data from external camera sensor bit [12]
CAM_D12_B	P9_4		
CAM_D13_A	P4_1	I	CPI pixel data from external camera sensor bit [13]
CAM_D13_B	P9_5		
CAM_D14_A	P4_2	I	CPI pixel data from external camera sensor bit [14]
CAM_D14_B	P9_6		
CAM_D15_A	P4_3	I	CPI pixel data from external camera sensor bit [15]
CAM_D15_B	P9_7		
CPI Clock and Sync A/B			
CAM_HSYNC_A	P0_0	I	CPI line valid from external camera sensor
CAM_HSYNC_B	P10_0		
CAM_VSYNC_A	P0_1	I	CPI vertical synchronization from external camera sensor
CAM_VSYNC_B	P10_1		
CAM_PCLK_A	P0_2	I	CPI pixel clock from external camera sensor
CAM_PCLK_B	P10_2		
CAM_XVCLK_A	P0_3	O	CPI pixel clock to external camera sensor
CAM_XVCLK_B	P10_3		

Table 3-26 presents LPCPI interface signals and provides descriptions to their functions.

CAUTION

- For LPCAM_PCLK and LPCAM_XVCLK signals, recommended to be used are LPCAM_PCLK_A and LPCAM_XVCLK_A pin multiplexing options.

Table 3-26 LPCPI Signal Descriptions

Signal Name	Pin Name	Type	Description
LPCPI Data Bus A/B/C			
LPCAM_D0_A	P8_0	I	LPCPI pixel data from external camera sensor bit [0]
LPCAM_D0_B	P2_4		

Signal Name	Pin Name	Type	Description
LPCAM_D0_C	P1_4		
LPCAM_D1_A	P8_1	I	LPCPI pixel data from external camera sensor bit [1]
LPCAM_D1_B	P2_5		
LPCAM_D1_C	P1_5		
LPCAM_D2_A	P8_2	I	LPCPI pixel data from external camera sensor bit [2]
LPCAM_D2_B	P2_6		
LPCAM_D2_C	P1_6		
LPCAM_D3_A	P8_3	I	LPCPI pixel data from external camera sensor bit [3]
LPCAM_D3_B	P2_7		
LPCAM_D3_C	P1_7		
LPCAM_D4_A	P8_4	I	LPCPI pixel data from external camera sensor bit [4]
LPCAM_D4_B	P3_0		
LPCAM_D4_C	P2_0		
LPCAM_D5_A	P8_5	I	LPCPI pixel data from external camera sensor bit [5]
LPCAM_D5_B	P3_1		
LPCAM_D5_C	P2_1		
LPCAM_D6_A	P8_6	I	LPCPI pixel data from external camera sensor bit [6]
LPCAM_D6_B	P3_2		
LPCAM_D6_C	P2_2		
LPCAM_D7_A	P8_7	I	LPCPI pixel data from external camera sensor bit [7]
LPCAM_D7_B	P3_3		
LPCAM_D7_C	P2_3		
LPCPI Clock and Sync A/B/C			
LPCAM_HSYNC_A	P10_0	I	LPCPI line valid from external camera sensor
LPCAM_HSYNC_B	P0_0		
LPCAM_HSYNC_C	P1_0		
LPCAM_VSYNC_A	P10_1	I	LPCPI vertical synchronization from external camera sensor
LPCAM_VSYNC_B	P0_1		
LPCAM_VSYNC_C	P1_1		
LPCAM_PCLK_A	P10_2	I	LPCPI pixel clock from external camera sensor
LPCAM_PCLK_B	P0_2		
LPCAM_PCLK_C	P1_2		
LPCAM_XVCLK_A	P10_3	O	LPCPI pixel clock to external camera sensor
LPCAM_XVCLK_B	P0_3		
LPCAM_XVCLK_C	P1_3		

3.18.2 CSI Overview

The MIPI Camera Serial Interface (CSI) facilitates the data reception from a MIPI CSI-2 compliant camera sensor. The interface is realized through a MIPI CSI-2 host controller that implements the protocol functions defined in the MIPI CSI-2 Specification, and a MIPI D-PHY module acting as the physical layer.

The device includes a single CSI implementation.

The CSI supports the following main features:

- Conformity to MIPI standards:
  - MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.2, January 2014
  - MIPI Alliance Specification for D-PHY, Version 1.2, September 2014
- PHY Protocol Interface (PPI) between the CSI-2 host controller and the D-PHY receiver
- Up to two D-PHY RX data lanes
- Up to 2.5 Gbps throughput per lane
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Virtual channel extension—up to 16 interleaved virtual channels
- Timing accurate signaling of frame and line synchronization packets
- Several frame formats:
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type (packet or frame level) and virtual channel interleaving
- Primary and secondary data formats:
  - YUV420: 8-bit (legacy)/8-bit/10-bit/8-bit (CSPS)/10-bit (CSPS)
  - YUV422: 8-bit/10-bit
  - RGB: RGB888/RGB666/RGB565/RGB555/RGB444
  - RAW: RAW6/RAW7/RAW8/RAW10/RAW12/RAW14/RAW16
  - Generic 8-bit long packet data types
  - User-defined byte-based data
  - Embedded data (RAW16)
- Error detection and correction at PHY, packet, line and frame level
- Up to four Data IDs (VC/DT pairs) for simultaneous error monitoring
- Data scrambling for Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) mitigation
- Configurable Image Pixel Interface (IPI) to system level that provides:
  - Conversion of CSI-2 packets data from byte to pixel format
  - 16- or 48-bit output parallel data bus, operating at pixel clock rate and delivering either one color component at a time or one pixel (or pair of pixels) per pixel clock cycle, respectively
  - Vertical and horizontal timing accurate video synchronization signals
  - 1024-entry FIFO for data storage and synchronization
- APB slave configuration interface

The CSI does not provide support for RAW data type decompression.

Table 3-27 presents MIPI CSI interface signals and provides descriptions to their functions.

Table 3-27 MIPI CSI Signal Descriptions

Signal Name	Pin Name	Type	Description
MIPICSI_0_P	MIPICSI_0_P	I	CSI D-PHY Rx differential data lane 0 (positive)
MIPICSI_0_N	MIPICSI_0_N	I	CSI D-PHY Rx differential data lane 0 (negative)
MIPICSI_1_P	MIPICSI_1_P	I	CSI D-PHY Rx differential data lane 1 (positive)
MIPICSI_1_N	MIPICSI_1_N	I	CSI D-PHY Rx differential data lane 1 (negative)
MIPICSI_C_P	MIPICSI_C_P	I	CSI D-PHY Rx differential clock lane (positive)
MIPICSI_C_N	MIPICSI_C_N	I	CSI D-PHY Rx differential clock lane (negative)

NOTE

The CSI D-PHY Rx module shares the MIPI_REXT signal connection to a reference resistor (200 Ω, ±1%) with DSI D-PHY Tx module. For more details, see Table 3-29 MIPI DSI Signal Descriptions.

3.19 Display Interfaces

3.19.1 DPI Controller Overview

The Display Parallel Interface (DPI) provides a 24-bit RGB data bus either directly to LCD and TFT panels with a resolution of up to WXGA (1280 × 800) or to the MIPI DSI Controller. In addition to the 24 data lines, the interface includes pixel clock up to 50 MHz, horizontal and vertical synchronization pulses, and data enable signals with configurable polarity.

The device includes a single Configurable DPI Controller (CDC).

The CDC supports the following main features:

- Configurable resolution and refresh rate
- Two display layers
- Programmable background color
- Color Look-Up Table (CLUT) with 256 × 24-bit entries per layer for indexed pixel formats
- Flexible blending between the layers using alpha value (pixel alpha or constant alpha)
- Color keying: defining transparent color for pixel formats without alpha channel
- Windowing: blending a programmable rectangular area of one layer into the other
- Gamma correction
- Dithering (2 bits per color component): providing softer color transitions for displays with less color depth
- Multiple input pixel formats selectable per layer:
  - ARGB8888, RGBA8888, RGB888, RGB565, ARGB1555, ARGB4444
  - AL44 (4-bit alpha + 4-bit luminance) and L8 (8-bit luminance)
- RGB888 output pixel format
- Master Bus Interface (MBI): 64-bit AXI interface used for pixel data transfer
- Slave Bus Interface (SBI): 32-bit APB interface used for configuration

Table 3-28 presents DPI interface signals and provides descriptions to their functions.

Table 3-28 DPI Signal Descriptions

Signal Name	Pin Name	Type	Description
DPI Data Bus A/B			
CDC_D0_A	P8_0	O	DPI RGB pixel data output bit B[0]
CDC_D0_B	P11_0		
CDC_D1_A	P8_1	O	DPI RGB pixel data output bit B[1]
CDC_D1_B	P11_1		
CDC_D2_A	P8_2	O	DPI RGB pixel data output bit B[2]
CDC_D2_B	P11_2		
CDC_D3_A	P8_3	O	DPI RGB pixel data output bit B[3]
CDC_D3_B	P11_3		
CDC_D4_A	P8_4	O	DPI RGB pixel data output bit B[4]
CDC_D4_B	P11_4		

Signal Name	Pin Name	Type	Description
CDC_D5_A	P8_5	O	DPI RGB pixel data output bit B[5]
CDC_D5_B	P11_5		
CDC_D6_A	P8_6	O	DPI RGB pixel data output bit B[6]
CDC_D6_B	P11_6		
CDC_D7_A	P8_7	O	DPI RGB pixel data output bit B[7]
CDC_D7_B	P11_7		
CDC_D8_A	P9_0	O	DPI RGB pixel data output bit G[0]
CDC_D8_B	P12_0		
CDC_D9_A	P9_1	O	DPI RGB pixel data output bit G[1]
CDC_D9_B	P12_1		
CDC_D10_A	P9_2	O	DPI RGB pixel data output bit G[2]
CDC_D10_B	P12_2		
CDC_D11_A	P9_3	O	DPI RGB pixel data output bit G[3]
CDC_D11_B	P12_3		
CDC_D12_A	P9_4	O	DPI RGB pixel data output bit G[4]
CDC_D12_B	P12_4		
CDC_D13_A	P9_5	O	DPI RGB pixel data output bit G[5]
CDC_D13_B	P12_5		
CDC_D14_A	P9_6	O	DPI RGB pixel data output bit G[6]
CDC_D14_B	P12_6		
CDC_D15_A	P9_7	O	DPI RGB pixel data output bit G[7]
CDC_D15_B	P12_7		
CDC_D16_A	P10_0	O	DPI RGB pixel data output bit R[0]
CDC_D16_B	P13_0		
CDC_D17_A	P10_1	O	DPI RGB pixel data output bit R[1]
CDC_D17_B	P13_1		
CDC_D18_A	P10_2	O	DPI RGB pixel data output bit R[2]
CDC_D18_B	P13_2		
CDC_D19_A	P10_3	O	DPI RGB pixel data output bit R[3]
CDC_D19_B	P13_3		
CDC_D20_A	P10_4	O	DPI RGB pixel data output bit R[4]
CDC_D20_B	P13_4		
CDC_D21_A	P10_5	O	DPI RGB pixel data output bit R[5]
CDC_D21_B	P13_5		
CDC_D22_A	P10_6	O	DPI RGB pixel data output bit R[6]
CDC_D22_B	P13_6		
CDC_D23_A	P10_7	O	DPI RGB pixel data output bit R[7]
CDC_D23_B	P13_7		
DPI Clock and Sync A/B			
CDC_DE_A	P5_4	O	DPI pixel data enable
CDC_DE_B	P0_7		
CDC_PCLK_A	P5_3	O	DPI pixel clock
CDC_PCLK_B	P2_3		
CDC_HSYNC_A	P5_5	O	DPI horizontal synchronization
CDC_HSYNC_B	P4_1		

Signal Name	Pin Name	Type	Description
CDC_VSYNC_A	P5_6	O	DPI vertical synchronization
CDC_VSYNC_B	P4_0		

3.19.2 DSI Overview

The MIPI Display Serial Interface (DSI) facilitates the communication and data transfer to a MIPI DSI compliant display panel. The interface is realized through a MIPI DSI host controller that implements the protocol functions defined in the MIPI DSI Specification, and a MIPI D-PHY module acting as the physical layer.

The device includes a single DSI implementation.

The DSI supports the following main features:

- Conformity to MIPI standards:
  - MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.2—16 June 2014
  - MIPI Alliance Standard for Display Pixel Interface v2.00 (DPI-2)—15 September 2005
  - MIPI Alliance Specification for Stereoscopic Display Formats (SDF) v1.0—22 November 2011
  - MIPI Alliance Specification for D-PHY v1.2, 01 August 2014
- PPI between the DSI host controller and the D-PHY transmitter
- Up to two D-PHY TX data lanes
- Up to 2.5 Gbps throughput per lane
- Bidirectional communication and escape mode support through data lane 0
- End of Transmission Packet (EoTp)
- ECC and checksum capabilities
- Fault recovery schemes
- Stereoscopic (3D) image data transmission
- Video mode only
- Configurable MIPI Display Pixel Interface (DPI) to system level that provides:
  - Data transfer in Video mode:
    - Real-time pixel stream
    - Shut Down Peripheral and Color Mode commands
  - DPI interface color coding mappings into a 30-bit interface:
    - 16-bit RGB
    - 18-bit RGB
    - 24-bit RGB
  - Programmable polarity of all DPI interface signals
  - The maximum resolution and frame rate are limited by the pixel clock and the available DSI physical link bandwidth (defined by the number of lanes and the maximum speed per lane)
- Slave interface used for the transmission of generic commands
- Independently programmable virtual channel ID for the DPI and slave interfaces
- DPI payload FIFO with 1024 × 32-bit slots depth
- Generic command FIFO with 16 × 32-bit slots depth
- Generic payload FIFO with 128 × 32-bit slots depth
- Generic read FIFO with 32 × 32-bit slots depth
- Video mode pattern generator with the following capabilities:
  - Vertical and horizontal color bar generation without DPI stimuli
  - PHY Bit-Error Ratio (BER) pattern without DPI stimuli

The DSI does not support the following features:

- Command mode
- VESA® Display Stream Compression (DSC) standard

Table 3-29 presents MIPI DSI interface signals and provides descriptions to their functions.

Table 3-29 MIPI DSI Signal Descriptions

Signal Name	Pin Name	Type	Description
MIPIDSI_0_P	MIPIDSI_0_P	IO	DSI D-PHY Tx differential data lane 0 (positive)
MIPIDSI_0_N	MIPIDSI_0_N	IO	DSI D-PHY Tx differential data lane 0 (negative)
MIPIDSI_1_P	MIPIDSI_1_P	O	DSI D-PHY Tx differential data lane 1 (positive)
MIPIDSI_1_N	MIPIDSI_1_N	O	DSI D-PHY Tx differential data lane 1 (negative)
MIPIDSI_C_P	MIPIDSI_C_P	O	DSI D-PHY Tx differential clock lane (positive)
MIPIDSI_C_N	MIPIDSI_C_N	O	DSI D-PHY Tx differential clock lane (negative)
MIPI_REXT	MIPI_REXT	P	DSI D-PHY Tx and CSI D-PHY Rx external reference resistor (200 Ω, ±1%) connection(1)

1. Shared with CSI D-PHY Rx module.

3.20 Analog Peripherals

3.20.1 ADC Overview

The Analog-to-Digital Converter (ADC) modules are 12-bit/24-bit, multi-input units used for analog signals conversion into digital values.

The device includes three ADC12 modules and one ADC24 module.

ADC12 modules support the following main features:

- 12-bit Successive Approximation Register (SAR) ADC
- Conversion rate of up to 1.25 MSPS
- 6 external inputs and two internal inputs:
  - 6 external pins may be configured to 6 single-ended or 3 differential inputs
  - One input from the on-chip temperature sensor (TSENS)
  - One input from internal voltage reference

ADC24 supports the following main features:

- 24-bit Sigma-Delta ADC
- Conversion rate of up to 16 kSPS
- 4 external differential inputs

ADC12 and ADC24 common features:

- Programmable gain instrumentation amplifier (up to 38 dB gain)
- On-chip offset calibration and factory calibrated gain error
- Widely programmable sample time
- Hardware averaging option (up to 256 samples) for enhanced Signal-to-Noise Ratio (SNR)
  - ADC12 must use hardware averaging at all times, with a minimum of two samples per average
- Flexible digital user interface:
  - Programmable input scan modes:
    - Single-shot or continuous conversions
    - A sequencer can be programmed to loop over a selection of inputs
  - Conversions can be triggered also externally by UTIMER events or QEC pins
  - Conversion results can be stored into sample registers and to SRAM via DMA

    - Hardware data shift:
        - 1 to 12 bits left shift
        - 1 to 12 bits right shift (up to 8 bits for the averaging function plus 4 bits more)
    - Threshold and window detection options. A comparator logic can generate interrupts when an input signal passes programmable thresholds
- Designed for low power operation:
    - ADC sample rate is selectable via a clock divider
    - ADC power consumption decreases as sample rate decreases
- The ADC12, ADC24, as well as other analog peripherals, are powered from a dedicated internal 1.8-V LDO

For information on ADC interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.2 DAC12 Overview

The Digital-to-Analog Converter (DAC12) module converts 12-bit digital values into analog voltage signals. The analog output range is between 0 V and 1.8 V in LP mode.

The device includes two DAC12 modules.

Each DAC12 module supports the following main features:

- Up to 1 kHz conversion rate at 12-bit resolution
- Accepts unsigned binary or two's complement signed digital data
- Programmable output current up to 1.5 mA
- Programmable load capacitance compensation
- Internal 1.8-V voltage reference
- Excellent high-frequency Power Supply Rejection Ratio (PSRR)
- Maximum current output up to 1.5 mA
- Software-selectable low-power (LP) or high-performance (HP) modes
    - HP mode handles larger resistive load at the expense of higher power consumption
    - LP mode handles slow sample rate and light resistive load for power savings

For information on DAC interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.3 CMP Overview

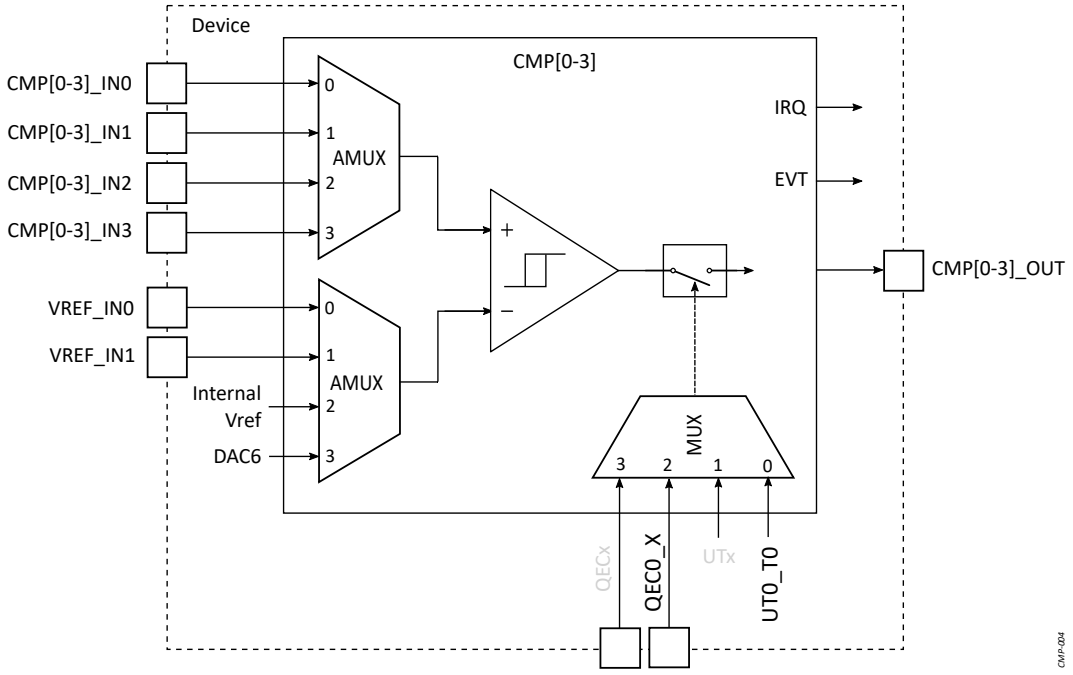
The High-Speed Comparator (CMP) module is a rail-to-rail, multi-input, analog comparator with programmable reference voltage and hysteresis.

The device includes up to four CMP modules.

Each CMP module supports the following main features:

- Reference voltage from DAC6, internal Vref, or external pins
- Programmable hysteresis
- Windowing (gating) driven by one of four events from UTIMER and QEC
- Comparator result inverter
- Configurable number of taps for filtering
- Interrupt generation after filtering
- Response time: < 5 ns
- Power supply from internal 1.8-V LDO (LDO-5)

Figure 3-11 CMP Overview



For information on CMP interface signals and their descriptions, see Section 3.20.6 Analog Signals.

Table 3-30 presents the CMP digital outputs.

Table 3-30 CMP Signal Descriptions

Signal Name	Pin Name	Type	Description
CMP Outputs A/B			
CMP0_OUT_A	P7_3	O	CMP0 comparison result output
CMP0_OUT_B	P14_7		
CMP1_OUT_A	P7_2	O	CMP1 comparison result output
CMP1_OUT_B	P14_6		
CMP2_OUT_A	P7_1	O	CMP2 comparison result output
CMP2_OUT_B	P14_5		
CMP3_OUT_A	P7_0	O	CMP3 comparison result output
CMP3_OUT_B	P14_4		

3.20.4 LPCMP Overview

The Low-Power Comparator (LPCMP) module is a low power, rail-to-rail, analog comparator with selectable reference voltage and hysteresis.

The device includes a single LPCMP module located in the PD0 domain.

The LPCMP supports the following main features:

- Up to four external pins for voltage monitoring
- Voltage reference from:
  - Internal AON 0.8-V voltage reference or
  - External VREF pins
- Programmable hysteresis
- Power supply from VDD_IO_1V8 pin

- Response time: < 10 µs
- The LPCMP interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPCMP. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

For information on LPCMP interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.5 TSENS Overview

The Temperature Sensor (TSENS) generates a voltage V_{TEMP} that varies incrementally with silicon die's temperature.

The TSENS is connected internally to input channel 6 of each ADC12 module. ADC12 can convert the sensor output voltage into a digital value. The real temperature can be translated using *temperature.h* C header file available in the Alif Ensemble CMSIS pack.

The sensor provides good linearity and accuracy of better than 2.4 °C. Additional calibration can be applied to improve accuracy.

3.20.6 Analog Signals

Table 3-31 shows how the analog signals are mapped simultaneously to functions of the analog modules. Each signal can be used by more than one module at a time.

Table 3-31 Analog Signal Functions Mapping

Signal Name	Function by Module				
	ADC12	ADC24	DAC	CMP	LPCMP
ANA_S0	ADC120_IN0	ADC24_IN0_P		CMP0_IN0	
ANA_S1	ADC120_IN1	ADC24_IN1_P		CMP1_IN0	
ANA_S2	ADC120_IN2	ADC24_IN2_P		CMP2_IN0	
ANA_S3	ADC120_IN3	ADC24_IN3_P		CMP3_IN0	
ANA_S4	ADC120_IN4	ADC24_IN0_N		CMP0_IN3	
ANA_S5	ADC120_IN5	ADC24_IN1_N		CMP1_IN3	
ANA_S6	ADC121_IN0	ADC24_IN2_N		CMP0_IN1	
ANA_S7	ADC121_IN1	ADC24_IN3_N		CMP1_IN1	
ANA_S8	ADC121_IN2			CMP2_IN1	
ANA_S9	ADC121_IN3			CMP3_IN1	
ANA_S10	ADC121_IN4			CMP2_IN3	
ANA_S11	ADC121_IN5			CMP3_IN3	
ANA_S12	ADC122_IN0			CMP0_IN2	
ANA_S13	ADC122_IN1			CMP1_IN2	
ANA_S14	ADC122_IN2			CMP2_IN2	
ANA_S15	ADC122_IN3			CMP3_IN2	
ANA_S16	ADC122_IN4			VREF_IN0	

Signal Name	Function by Module				
	ADC12	ADC24	DAC	CMP	LPCMP
ANA_S17	ADC122_IN5			VREF_IN1	
ANA_S18			DAC12_0_OUT		VREF_IN2
ANA_S19			DAC12_1_OUT		
ANA_S20					LPCMP_IN0
ANA_S21					LPCMP_IN1
ANA_S22					LPCMP_IN2
ANA_S23					LPCMP_IN3

Table 3-32 presents the analog signals with the respective mapping to the analog modules and provides descriptions to their functions.

Table 3-32 Analog Signal Descriptions

Signal Name	Pin Name	Type	Description
ANA_S0	P0_0	A	ADC120_IN0 (ADC120 input 0) ADC24_IN0_P (ADC24 differential input 0 positive) CMP0_IN0 (CMP0 input 0)
ANA_S1	P0_1	A	ADC120_IN1 (ADC120 input 1) ADC24_IN1_P (ADC24 differential input 1 positive) CMP1_IN0 (CMP1 input 0)
ANA_S2	P0_2	A	ADC120_IN2 (ADC120 input 2) ADC24_IN2_P (ADC24 differential input 2 positive) CMP2_IN0 (CMP2 input 0)
ANA_S3	P0_3	A	ADC120_IN3 (ADC120 input 3) ADC24_IN3_P (ADC24 differential input 3 positive) CMP3_IN0 (CMP3 input 0)
ANA_S4	P0_4	A	ADC120_IN4 (ADC120 input 4) ADC24_IN0_N (ADC24 differential input 0 negative) CMP0_IN3 (CMP0 input 3)
ANA_S5	P0_5	A	ADC120_IN5 (ADC120 input 5) ADC24_IN1_N (ADC24 differential input 1 negative) CMP1_IN3 (CMP1 input 3)
ANA_S6	P0_6	A	ADC121_IN0 (ADC121 input 0) ADC24_IN2_N (ADC24 differential input 2 negative) CMP0_IN1 (CMP0 input 1)
ANA_S7	P0_7	A	ADC121_IN1 (ADC121 input 1) ADC24_IN3_N (ADC24 differential input 3 negative) CMP1_IN1 (CMP1 input 1)
ANA_S8	P1_0	A	ADC121_IN2 (ADC121 input 2) CMP2_IN1 (CMP2 input 1)
ANA_S9	P1_1	A	ADC121_IN3 (ADC121 input 3) CMP3_IN1 (CMP3 input 1)
ANA_S10	P1_2	A	ADC121_IN4 (ADC121 input 4) CMP2_IN3 (CMP2 input 3)
ANA_S11	P1_3	A	ADC121_IN5 (ADC121 input 5) CMP3_IN3 (CMP3 input 3)
ANA_S12	P1_4	A	ADC122_IN0 (ADC122 input 0) CMP0_IN2 (CMP0 input 2)

Signal Name	Pin Name	Type	Description
ANA_S13	P1_5	A	ADC122_IN1 (ADC122 input 1) CMP1_IN2 (CMP1 input 2)
ANA_S14	P1_6	A	ADC122_IN2 (ADC122 input 2) CMP2_IN2 (CMP2 input 2)
ANA_S15	P1_7	A	ADC122_IN3 (ADC122 input 3) CMP3_IN2 (CMP3 input 2)
ANA_S16	P2_0	A	ADC122_IN4 (ADC122 input 4) VREF_IN0 (CMP0-CMP3 and LPCMP reference voltage input 0)
ANA_S17	P2_1	A	ADC122_IN5 (ADC122 input 5) VREF_IN1 (CMP0-CMP3 and LPCMP reference voltage input 1)
ANA_S18	P2_2	A	DAC12_0_OUT (DAC120 output) VREF_IN2 (LPCMP reference voltage input 2)
ANA_S19	P2_3	A	DAC12_1_OUT (DAC121 output)
ANA_S20	P2_4	A	LPCMP_IN0 (LPCMP input 0)
ANA_S21	P2_5	A	LPCMP_IN1 (LPCMP input 1)
ANA_S22	P2_6	A	LPCMP_IN2 (LPCMP input 2)
ANA_S23	P2_7	A	LPCMP_IN3 (LPCMP input 3)

3.21 Debug Infrastructure

To support the debug of multiple cores running simultaneously, the device provides an extensive debug infrastructure, compliant with the Arm® Debug Interface Architecture Specification ADIv6.0. The debug features include:

- JTAG debug support
- Serial Wire Debug (SWD) support
- External debug of SE, RTSS-HP or RTSS-HE by an off-chip debugger
- Debug through power down for RTSS-HP and RTSS-HE
- Debug from reset for all systems
- Support for single or multi-system debug
- Trace and cross trigger capabilities

Table 3-33 presents JTAG interface signals and provides descriptions to their functions.

Table 3-33 JTAG Signal Descriptions

Signal Name	Pin Name	Type	Description
JTAG			
JTAG_TCK	P4_4	I	JTAG test clock input
JTAG_TMS	P4_5	I	JTAG test mode select input
JTAG_TDI	P4_6	I	JTAG test data input
JTAG_TDO	P4_7	O	JTAG test data output

NOTE

Code execution tracing during debug stores the resulting trace data in on-chip SRAM that can be read out of the device for formatting and post-analysis.

4 Pin Assignments

4.1 Pin Location per Package Type

4.1.1 WLCSP208 Package Pin Location Assignment

Figure 4-1 presents a simplified diagram of the WLCSP208 package pin locations.

Figure 4-1 WLCSP208 Pin Location Assignment Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
A	GPIO4_1		GPIO4_5		GPIO13_5		GPIO5_3		GPIO5_7		GPIO6_3		VDD_CORE_0V8		GPIO12_4		GPIO14_0		GPIO7_3		GPIO8_3		HFXO_P		HFXO_N		N/A	
B		SEUART_RX		GPIO4_4		GPIO5_0		GPIO5_2		GPIO5_6		VSS		GPIO6_4		GPIO12_5		GPIO7_0		GPIO8_2		VSS		VSS		N.C.		N.C.
C	GPIO12_2		RESERVED		SEUART_TX		GPIO4_6		GPIO13_7		GPIO5_5		VDD_IO_1V8		N.C.		GPIO6_7		GPIO8_0		VDD_SX_0V8		N.C.		VDD_PLL_0V8		N.C.	
D		GPIO12_0		GPIO12_1		NSRST		GPIO4_3		GPIO13_6		GPIO5_4		GPIO6_2		GPIO6_6		GPIO7_1		GPIO8_4		VSS		N/A		N.C.		N.C.
E	GPIO13_3		GPIO13_4		GPIO4_0		GPIO12_3		GPIO4_2		GPIO4_7		GPIO5_1		GPIO6_1		GPIO12_7		GPIO8_1		N.C.		N.C.		VSS		VSS	
F		GPIO13_0		VDD_IO_1V8		GPIO13_1		GPIO13_2		GPIO2_7		GPIO2_5		GPIO6_0		GPIO12_6		GPIO7_2		GPIO3_3		GPIO3_2		N.C.		VSS		N.C.
G	VSS		VDD_CORE_0V8		GPIO2_4		GPIO2_0		GPIO1_6		N.C.		VREG_MIPI_1V8		GPIO6_5		GPIO3_0		GPIO3_1		GPIO3_4		GPIO3_5		GPIO14_2		GPIO14_1	
H		GPIO2_6		GPIO2_3		GPIO1_7		GPIO1_2		GPIO0_6		GPIO0_1		USB_VBUS		GPIO9_1		GPIO9_0		GPIO8_7		GPIO8_6		VDD_CORE_0V8		VSS		GPIO8_5
J	GPIO2_2		GPIO2_1		GPIO1_4		GPIO0_7		GPIO0_2		VREG_DIG_1V8		MIPI_REXT		GPIOV_5		GPIO11_1		GPIO9_7		GPIO9_5		GPIO9_4		GPIO9_3		GPIO9_2	
K		GPIO1_5		GPIO1_3		GPIO0_5		GPIO0_4		POR_N		VDD_BATT		USB_REXT		GPIO11_6		GPIOV_0		GPIO10_3		GPIO10_2		GPIO10_1		GPIO10_0		GPIO9_6
L	GPIO1_0		GPIO1_1		VDD_MAIN		GPIO0_0		VSS		VREG_AON		VREG_MIPI_0V8		GPIO14_6		GPIOV_6		GPIO7_5		GPIO10_7		GPIO10_6		GPIO10_5		GPIO10_4	
M		VREF_N		VREF_P		VREG_CORE_0V8		MIPICSI_C_P		MIPICSI_1_P		VDD_MIPI_1V8		MIPIDSI_1_N		GPIO14_5		GPIOV_7		VSS		GPIO7_4		GPIO11_3		GPIO11_2		GPIO11_0
N	VSS_ANA		GPIO0_3		VREG_LP_1V8		MIPICSI_C_N		MIPICSI_1_N		MIPIDSI_0_N		MIPIDSI_1_P		USB_DM		VDD_CORE_0V8		GPIO11_4		GPIOV_2		GPIOV_1		GPIO7_7		GPIO7_6	
P		VDD_BUCK		VSW		LFXO_N		MIPICSI_0_P		MIPIDSI_0_P		MIPIDSI_C_N		VDD_USB_3V3		USB_IO_ID		GPIO14_3		GPIO11_5		GPIO3_6		VDD_IO_1V8		GPIOV_3		VDD_IO_FLEX
R	VSW		VSS_BUCK		LFXO_P		MIPICSI_0_N		VSS		MIPIDSI_C_P		VSS		USB_DP		GPIO14_7		GPIO14_4		GPIO11_7		GPIO3_7		VSS		GPIOV_4	

For detailed information about package outlines, thermal characteristics, and markings, see Section 6.2.1 WLCSP208 Package Information.

4.1.2 FBGA194 Package Pin Location Assignment

Figure 4-2 presents a simplified diagram of the FBGA194 package pin locations.

Figure 4-2 FBGA194 Pin Location Assignment Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VDD_PLL_0V8	VDD_SX_0V8	HFXO_N	HFXO_P	VDD_IO_1V8	GPIO3_1	GPIO8_3	GPIO7_3	GPIO6_7	GPIO12_5	GPIO6_2	GPIO6_0	SEUART_TX	SEUART_RX	GPIO13_7	GPIO5_0	GPIO13_5	GPIO4_6	GPIO4_5
B	N.C.	VSS	GPIO7_1	GPIO8_4	VDD_CORE_0V8	GPIO3_0	GPIO8_0	GPIO7_0	GPIO14_0	GPIO6_3	GPIO5_7	GPIO5_6	GPIO5_3	GPIO5_1	GPIO13_6	GPIO4_7	GPIO4_4	GPIO4_3	GPIO4_1
C	N.C.	GPIO8_1	GPIO8_2															VSS	GPIO4_2
D	GPIO7_2	GPIO12_7																GPIO12_3	VDD_IO_1V8
E	VDD_CORE_0V8	GPIO3_2			GPIO12_6	GPIO6_6	GPIO6_5	GPIO6_4	GPIO6_1	GPIO5_5	GPIO5_4	GPIO5_2	GPIO13_3	GPIO13_4	GPIO12_2			GPIO12_1	VDD_CORE_0V8
F	GPIO3_5	GPIO3_4			GPIO12_4										GPIO13_2			GPIO4_0	GPIO12_0
G	GPIO14_2	GPIO3_3			GPIO9_2										GPIO13_1			GPIO13_0	GPIO2_4
H	GPIO8_5	GPIO14_1			GPIO9_3										GPIO2_3			GPIO2_6	GPIO2_5
J	GPIO8_7	GPIO8_6			GPIO9_4			N.C.	GPIO11_5	VSS	RESERVED	NSRST			GPIO2_2			GPIO1_7	GPIO2_7
K	GPIO9_1	GPIO9_0			GPIO9_6			GPIO11_4	VSS	VSS	VSS	GPIO14_6			GPIO1_3			GPIO2_1	GPIO2_0
L	GPIO9_5	VSS			GPIO9_7			GPIO3_7	GPIO11_7	VSS	GPIO14_5	GPIO14_7			GPIO1_2			GPIO1_5	GPIO1_6
M	GPIO10_1	GPIO10_0			GPIO10_4										GPIO1_1			N.C.	GPIO1_4
N	GPIO10_2	GPIO10_3			GPIO10_5										GPIO0_5			VREF_P	VREG_MIPI_1V8
P	GPIO10_7	GPIO11_0			GPIO10_6										GPIO0_6			VSS_ANA	VDD_MAIN
R	GPIO11_1	GPIO11_2			GPIO11_3	GPIO11_6	GPIO14_3	GPIO14_4	USB_IO_ID	GPIO0_4	GPIO0_3	GPIO0_2	GPIO0_1	GPIO1_0	GPIO0_7			VDD_BUCK	GPIO0_0
T	GPIO7_4	GPIO7_5																VDD_BATT	VSW
U	GPIO7_7	GPIOV_2	GPIO7_6														VREG_AON	POR_N	VREG_DIG_1V8
V	GPIOV_3	GPIOV_0	GPIOV_4	GPIOV_6	GPIO3_6	VDD_CORE_0V8	USB_DM	USB_REXT	MIPIDSI_1_N	MIPIDSI_C_N	MIPIDSI_0_N	VSS	MIPI_REXT	MIPICSI_0_N	MIPICSI_1_N	MIPICSI_C_N	LFXO_N	VREG_AUX_1V8	VSS_BUCK
W	VDD_IO_FLEX	GPIOV_1	VDD_IO_1V8	GPIOV_5	GPIOV_7	USB_VBUS	USB_DP	VDD_USB_3V3	MIPIDSI_1_P	MIPIDSI_C_P	MIPIDSI_0_P	VDD_MIPI_1V8	VREG_MIPI_0V8	MIPICSI_0_P	MIPICSI_1_P	MIPICSI_C_P	LFXO_P	VREG_CORE_0V8	VREG_LP_1V8

For detailed information about package outlines, thermal characteristics, and markings, see Section 6.2.2 FBGA194 Package Information.

4.2 Pin Function Options by Location

Table 4-1 describes the pin functions available as multiplexed on each pin.

CAUTION

A peripheral I/O signal can be routed to up to four different pins. In such cases, a suffix _A, _B, _C, or _D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set or Pin Group.

There are no restrictions on the combination of signals from different pin groups (A, B, C, or D). However, it is user's responsibility to make sure that each peripheral I/O signal is routed to only one pin at a time through the pin multiplexing options.

Additionally, for some peripherals there are recommendations on the pin multiplexing options to use, which are described below.

The following pin multiplexing options are recommended:

- For OSPI0, the OSPI0_D[0-7]_B data bus signals are recommended to be used for 100 MHz operation. OSPI0_D[0-7]_A and OSPI0_D[0-7]_C data bus signals are recommended to be used for 50 MHz operation.

- For OSPI1, the OSPI1_D[0-7]_C data bus signals are recommended to be used for 100 MHz operation. OSPI1_D[0-7]_A and OSPI1_D[0-7]_B data bus signals are recommended to be used for 50 MHz operation.

- For SDMMC, the SD_*_C signals are recommended to be used for 50 MHz operation. SD_*_A, SD_*_B, and SD_*_D signals are recommended to be used for 25 MHz operation.

- For CAM_PCLK and CAM_XVCLK signals, recommended to be used are CAM_PCLK_B and CAM_XVCLK_B pin multiplexing options.

- For LPCAM_PCLK and LPCAM_XVCLK signals, recommended to be used are LPCAM_PCLK_A and LPCAM_XVCLK_A pin multiplexing options.

Table 4-1 Pin Function Options by Location

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_0	L7	R19	GPIO0_0	IO	0	P0_0	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D0_A	IO	1			
			UART0_RX_A	I	2			
			I3C_SDA_A	IO	3			
			UT0_T0_A	IO	4			
			LPCAM_HSYNC_B	I	5			
			CAM_HSYNC_A	I	6			
			ANA_S0	A	7			
P0_1	H12	R13	GPIO0_1	IO	0	P0_1	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D1_A	IO	1			
			UART0_TX_A	O	2			
			I3C_SCL_A	IO	3			
			UT0_T1_A	IO	4			
			LPCAM_VSYNC_B	I	5			
			CAM_VSYNC_A	I	6			
			ANA_S1	A	7			
P0_2	J9	R12	GPIO0_2	IO	0	P0_2	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D2_A	IO	1			
			UART0_CTS_A	I	2			
			I2C0_SDA_A	IO	3			
			UT1_T0_A	IO	4			
			LPCAM_PCLK_B	I	5			
			CAM_PCLK_A	I	6			
			ANA_S2	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_3	N3	R11	GPIO0_3	IO	0	P0_3	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D3_A	IO	1			
			UART0_RTS_A	O	2			
			I2C0_SCL_A	IO	3			
			UT1_T1_A	IO	4			
			LPCAM_XVCLK_B	O	5			
			CAM_XVCLK_A	O	6			
			ANA_S3	A	7			
P0_4	K8	R10	GPIO0_4	IO	0	P0_4	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D4_A	IO	1			
			UART1_RX_A	I	2			
			PDM_D0_A	I	3			
			I2C1_SDA_A	IO	4			
			UT2_T0_A	IO	5			
			CAN_RXD_B	I	6			
			ANA_S4	A	7			
P0_5	K6	N15	GPIO0_5	IO	0	P0_5	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D5_A	IO	1			
			UART1_TX_A	O	2			
			PDM_C0_A	O	3			
			I2C1_SCL_A	IO	4			
			UT2_T1_A	IO	5			
			CAN_TXD_B	O	6			
			ANA_S5	A	7			
P0_6	H10	P15	GPIO0_6	IO	0	P0_6	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D6_A	IO	1			
			UART1_CTS_A	I	2			
			PDM_D1_A	I	3			
			I2C2_SCL_A	IO	4			
			UT3_T0_A	IO	5			
			CAN_STBY_B	O	6			
			ANA_S6	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_7	J7	R15	GPIO0_7	IO	0	P0_7	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D7_A	IO	1			
			UART1_RTS_A	O	2			
			PDM_C1_A	O	3			
			I2C2_SDA_A	IO	4			
			UT3_T1_A	IO	5			
			CDC_DE_B	O	6			
			ANA_S7	A	7			
P1_0	L1	R14	GPIO1_0	IO	0	P1_0	LVCMOS ANALOG	VDD_IO_1V8
			UART2_RX_A	I	1			
			SPI0_MISO_A	IO	2			
			I2C3_SDA_A	IO	3			
			UT4_T0_A	IO	4			
			LPCAM_HSYNC_C	I	5			
			ETH_RXD0_C	I	6			
			ANA_S8	A	7			
P1_1	L3	M15	GPIO1_1	IO	0	P1_1	LVCMOS ANALOG	VDD_IO_1V8
			UART2_TX_A	O	1			
			SPI0_MOSI_A	IO	2			
			I2C3_SCL_A	IO	3			
			UT4_T1_A	IO	4			
			LPCAM_VSYNC_C	I	5			
			ETH_RXD1_C	I	6			
			ANA_S9	A	7			
P1_2	H8	L15	GPIO1_2	IO	0	P1_2	LVCMOS ANALOG	VDD_IO_1V8
			UART3_RX_A	I	1			
			SPI0_SCLK_A	IO	2			
			I3C_SDA_B	IO	3			
			UT5_T0_A	IO	4			
			LPCAM_PCLK_C	I	5			
			ETH_RST_C	O	6			
			ANA_S10	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P1_3	K4	K15	GPIO1_3	IO	0	P1_3	LVCMOS ANALOG	VDD_IO_1V8
			UART3_TX_A	O	1			
			SPI0_SS0_A	IO	2			
			I3C_SCL_B	IO	3			
			UT5_T1_A	IO	4			
			LPCAM_XVCLK_C	O	5			
			ETH_TXD0_C	O	6			
			ANA_S11	A	7			
P1_4	J5	M19	GPIO1_4	IO	0	P1_4	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS0_A	O	1			
			UART0_RX_B	I	2			
			SPI0_SS1_A	O	3			
			UT6_T0_A	IO	4			
			LPCAM_D0_C	I	5			
			ETH_TXD1_C	O	6			
			ANA_S12	A	7			
P1_5	K2	L18	GPIO1_5	IO	0	P1_5	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS1_A	O	1			
			UART0_TX_B	O	2			
			SPI0_SS2_A	O	3			
			UT6_T1_A	IO	4			
			LPCAM_D1_C	I	5			
			ETH_TXEN_C	O	6			
			ANA_S13	A	7			
P1_6	G9	L19	GPIO1_6	IO	0	P1_6	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_RXDS_B	IO	1			
			UART1_RX_B	I	2			
			I2S0_SDI_A	I	3			
			UT7_T0_A	IO	4			
			LPCAM_D2_C	I	5			
			ETH_IRQ_C	I	6			
			ANA_S14	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P1_7	H6	J18	GPIO1_7	IO	0	P1_7	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SCLK_A	O	1			
			UART1_TX_B	O	2			
			I2S0_SDO_A	O	3			
			UT7_T1_A	IO	4			
			LPCAM_D3_C	I	5			
			ETH_REFCLK_C	IO	6			
			ANA_S15	A	7			
P2_0	G7	K19	GPIO2_0	IO	0	P2_0	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D0_B	IO	1			
			UART2_RX_B	I	2			
			LPPDM_D0_A	I	3			
			UT8_T0_A	IO	4			
			LPCAM_D4_C	I	5			
			ETH_MDIO_C	IO	6			
			ANA_S16	A	7			
P2_1	J3	K18	GPIO2_1	IO	0	P2_1	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D1_B	IO	1			
			UART2_TX_B	O	2			
			LPPDM_C0_A	O	3			
			UT8_T1_A	IO	4			
			LPCAM_D5_C	I	5			
			ETH_MDC_C	O	6			
			ANA_S17	A	7			
P2_2	J1	J15	GPIO2_2	IO	0	P2_2	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D2_B	IO	1			
			UART3_RX_B	I	2			
			LPPDM_D1_A	I	3			
			UT9_T0_A	IO	4			
			LPCAM_D6_C	I	5			
			ETH_CRS_DV_C	I	6			
			ANA_S18	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P2_3	H4	H15	GPIO2_3	IO	0	P2_3	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D3_B	IO	1			
			UART3_TX_B	O	2			
			LPPDM_C1_A	O	3			
			UT9_T1_A	IO	4			
			LPCAM_D7_C	I	5			
			CDC_PCLK_B	O	6			
			ANA_S19	A	7			
P2_4	G5	G19	GPIO2_4	IO	0	P2_4	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D4_B	IO	1			
			LPI2S_SDI_A	I	2			
			SPI1_MISO_A	IO	3			
			UT10_T0_A	IO	4			
			LPCAM_D0_B	I	5			
			CAM_D0_A	I	6			
			ANA_S20	A	7			
P2_5	F12	H19	GPIO2_5	IO	0	P2_5	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D5_B	IO	1			
			LPI2S_SDO_A	O	2			
			SPI1_MOSI_A	IO	3			
			UT10_T1_A	IO	4			
			LPCAM_D1_B	I	5			
			CAM_D1_A	I	6			
			ANA_S21	A	7			
P2_6	H2	H18	GPIO2_6	IO	0	P2_6	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D6_B	IO	1			
			LPI2S_SCLK_A	O	2			
			SPI1_SCLK_A	IO	3			
			UT11_T0_A	IO	4			
			LPCAM_D2_B	I	5			
			CAM_D2_A	I	6			
			ANA_S22	A	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P2_7	F10	J19	GPIO2_7	IO	0	P2_7	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_D7_B	IO	1			
			LPI2S_WS_A	O	2			
			SPI1_SS0_A	IO	3			
			UT11_T1_A	IO	4			
			LPCAM_D3_B	I	5			
			CAM_D3_A	I	6			
			ANA_S23	A	7			
P3_0	G17	B6	GPIO3_0	IO	0	P3_0	LVCMOS	VDD_IO_1V8
			OSPI0_SCLK_B	O	1			
			UART4_RX_A	I	2			
			PDM_D0_B	I	3			
			I2S0_SCLK_A	O	4			
			QEC0_X_A	I	5			
			LPCAM_D4_B	I	6			
			CAM_D4_A	I	7			
P3_1	G19	A6	GPIO3_1	IO	0	P3_1	LVCMOS	VDD_IO_1V8
			OSPI0_SCLKN_B	O	1			
			UART4_TX_A	O	2			
			PDM_C0_B	O	3			
			I2S0_WS_A	O	4			
			QEC0_Y_A	I	5			
			LPCAM_D5_B	I	6			
			CAM_D5_A	I	7			
P3_2	F22	E2	GPIO3_2	IO	0	P3_2	LVCMOS	VDD_IO_1V8
			OSPI0_SS0_B	O	1			
			PDM_D1_B	I	2			
			I2S1_SDI_A	I	3			
			I3C_SDA_C	IO	4			
			QEC0_Z_A	I	5			
			LPCAM_D6_B	I	6			
			CAM_D6_A	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P3_3	F20	G2	GPIO3_3	IO	0	P3_3	LVCMOS	VDD_IO_1V8
			OSPI0_SS1_B	O	1			
			PDM_C1_B	O	2			
			I2S1_SDO_A	O	3			
			I3C_SCL_C	IO	4			
			QEC1_X_A	I	5			
			LPCAM_D7_B	I	6			
			CAM_D7_A	I	7			
P3_4	G21	F2	GPIO3_4	IO	0	P3_4	LVCMOS	VDD_IO_1V8
			OSPI0_RXDS_A	IO	1			
			UART5_RX_A	I	2			
			LPPDM_C0_B	O	3			
			I2S1_SCLK_A	O	4			
			I2C0_SCL_B	IO	5			
			QEC1_Y_A	I	6			
			CAM_D8_A	I	7			
P3_5	G23	F1	GPIO3_5	IO	0	P3_5	LVCMOS	VDD_IO_1V8
			OSPI0_SCLKN_A	O	1			
			UART5_TX_A	O	2			
			LPPDM_D0_B	I	3			
			SPI0_SS1_B	O	4			
			I2C0_SDA_B	IO	5			
			QEC1_Z_A	I	6			
			CAM_D9_A	I	7			
P3_6	P22	V5	GPIO3_6	IO	0	P3_6	LVCMOS	VDD_IO_1V8
			LPUART_CTS_B	I	2			
			LPPDM_C1_B	O	3			
			SPI0_SS2_B	O	4			
			I2C1_SDA_B	IO	5			
			QEC2_X_A	I	6			
			CAM_D10_A	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P3_7	R23	L8	GPIO3_7	IO	0	P3_7	LVCMOS	VDD_IO_1V8
			LPUART_RTS_B	O	2			
			LPPDM_D1_B	I	3			
			SPI1_SS1_A	O	4			
			I2C1_SCL_B	IO	5			
			QEC2_Y_A	I	6			
			CAM_D11_A	I	7			
P4_0	E5	F18	GPIO4_0	IO	0	P4_0	LVCMOS	VDD_IO_1V8
			I2S1_WS_A	O	3			
			SPI1_SS2_A	O	4			
			QEC2_Z_A	I	5			
			CDC_VSYNC_B	O	6			
			CAM_D12_A	I	7			
P4_1	A1	B19	GPIO4_1	IO	0	P4_1	LVCMOS	VDD_IO_1V8
			I2S0_SDI_B	I	2			
			SPI1_SS3_A	O	3			
			QEC3_X_A	I	4			
			SD_CLK_D	O	5			
			CDC_HSYNC_B	O	6			
			CAM_D13_A	I	7			
P4_2	E9	C19	GPIO4_2	IO	0	P4_2	LVCMOS	VDD_IO_1V8
			I2S0_SDO_B	O	3			
			SPI2_MISO_A	IO	4			
			QEC3_Y_A	I	5			
			SD_CMD_D	IO	6			
			CAM_D14_A	I	7			
P4_3	D8	B18	GPIO4_3	IO	0	P4_3	LVCMOS	VDD_IO_1V8
			I2S0_SCLK_B	O	3			
			SPI2_MOSI_A	IO	4			
			QEC3_Z_A	I	5			
			SD_RST_D	O	6			
			CAM_D15_A	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P4_4	B4	B17	GPIO4_4	IO	0	P4_4	LVCMOS	VDD_IO_1V8
			JTAG_TCK[a]	I	1			
			I2S0_WS_B	O	2			
			SPI2_SCLK_A	IO	3			
			FAULT0_A	I	4			
P4_5	A3	A19	GPIO4_5	IO	0	P4_5	LVCMOS	VDD_IO_1V8
			JTAG_TMS[a]	I	1			
			SPI2_SS0_A	IO	2			
			FAULT1_A	I	3			
P4_6	C7	A18	GPIO4_6	IO	0	P4_6	LVCMOS	VDD_IO_1V8
			JTAG_TDI[a]	I	1			
			SPI2_SS1_A	O	2			
			FAULT2_A	I	3			
P4_7	E11	B16	GPIO4_7	IO	0	P4_7	LVCMOS	VDD_IO_1V8
			JTAG_TDO[a]	O	1			
			SPI2_SS2_A	O	2			
			FAULT3_A	I	3			
P5_0	B6	A16	GPIO5_0	IO	0	P5_0	LVCMOS	VDD_IO_1V8
			OSPI1_RXDS_A	IO	1			
			UART4_RX_C	I	2			
			PDM_D2_A	I	3			
			SPI0_MISO_B	IO	4			
			I2C2_SDA_B	IO	5			
			UT0_T0_B	IO	6			
			SD_D0_A	IO	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P5_1	E13	B14	GPIO5_1	IO	0	P5_1	LVCMOS	VDD_IO_1V8
			OSPI1_SS0_A	O	1			
			UART4_TX_C	O	2			
			PDM_D3_A	I	3			
			SPI0_MOSI_B	IO	4			
			I2C2_SCL_B	IO	5			
			UT0_T1_B	IO	6			
			SD_D1_A	IO	7			
P5_2	B8	E12	GPIO5_2	IO	0	P5_2	LVCMOS	VDD_IO_1V8
			OSPI1_SCLKN_A	O	1			
			UART5_RX_C	I	2			
			PDM_C3_A	O	3			
			SPI0_SS0_B	IO	4			
			LPI2C_SCL_B	I	5			
			UT1_T0_B	IO	6			
			SD_D2_A	IO	7			
P5_3	A7	B13	GPIO5_3	IO	0	P5_3	LVCMOS	VDD_IO_1V8
			OSPI1_SCLK_A	O	1			
			UART5_TX_C	O	2			
			SPI0_SCLK_B	IO	3			
			LPI2C_SDA_B	IO	4			
			UT1_T1_B	IO	5			
			SD_D3_A	IO	6			
			CDC_PCLK_A	O	7			
P5_4	D12	E11	GPIO5_4	IO	0	P5_4	LVCMOS	VDD_IO_1V8
			OSPI1_SS1_A	O	1			
			UART3_CTS_A	I	2			
			PDM_D2_B	I	3			
			SPI0_SS3_A	O	4			
			UT2_T0_B	IO	5			
			SD_D4_A	IO	6			
			CDC_DE_A	O	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P5_5	C11	E10	GPIO5_5	IO	0	P5_5	LVCMOS	VDD_IO_1V8
			OSPI1_SCLK_C	O	1			
			UART3_RTS_A	O	2			
			PDM_D3_B	I	3			
			UT2_T1_B	IO	4			
			SD_D5_A	IO	5			
			ETH_RXD0_A	I	6			
			CDC_HSYNC_A	O	7			
P5_6	B10	B12	GPIO5_6	IO	0	P5_6	LVCMOS	VDD_IO_1V8
			UART1_CTS_B	I	2			
			I2C2_SCL_C	IO	3			
			UT3_T0_B	IO	4			
			SD_D6_A	IO	5			
			ETH_RXD1_A	I	6			
			CDC_VSYNC_A	O	7			
P5_7	A9	B11	GPIO5_7	IO	0	P5_7	LVCMOS	VDD_IO_1V8
			OSPI1_SS0_C	O	1			
			UART1_RTS_B	O	2			
			I2C2_SDA_C	IO	3			
			UT3_T1_B	IO	4			
			SD_D7_A	IO	5			
			ETH_RST_A	O	6			
P6_0	F14	A12	GPIO6_0	IO	0	P6_0	LVCMOS	VDD_IO_1V8
			OSPI0_D0_C	IO	1			
			UART4_DE_A	O	2			
			PDM_D0_C	I	3			
			UT4_T0_B	IO	4			
			SD_D0_D	IO	5			
			ETH_TXD0_A	O	6			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P6_1	E15	E9	GPIO6_1	IO	0	P6_1	LVCMOS	VDD_IO_1V8
			OSPI0_D1_C	IO	1			
			UART5_DE_A	O	2			
			PDM_C0_C	O	3			
			UT4_T1_B	IO	4			
			SD_D1_D	IO	5			
			ETH_TXD1_A	O	6			
P6_2	D14	A11	GPIO6_2	IO	0	P6_2	LVCMOS	VDD_IO_1V8
			OSPI0_D2_C	IO	1			
			UART2_CTS_A	I	2			
			PDM_D1_C	I	4			
			UT5_T0_B	IO	5			
			SD_D2_D	IO	6			
			ETH_TXEN_A	O	7			
P6_3	A11	B10	GPIO6_3	IO	0	P6_3	LVCMOS	VDD_IO_1V8
			OSPI0_D3_C	IO	1			
			UART2_RTS_A	O	2			
			PDM_C1_C	O	4			
			UT5_T1_B	IO	5			
			SD_D3_D	IO	6			
			ETH_IRQ_A	I	7			
P6_4	B14	E8	GPIO6_4	IO	0	P6_4	LVCMOS	VDD_IO_1V8
			OSPI0_D4_C	IO	1			
			UART2_CTS_B	I	2			
			SPI1_SS0_B	IO	4			
			UT6_T0_B	IO	5			
			SD_D4_D	IO	6			
			ETH_REFCLK_A	IO	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P6_5	G15	E7	GPIO6_5	IO	0	P6_5	LVCMOS	VDD_IO_1V8
			OSPI0_D5_C	IO	1			
			UART2_RTS_B	O	2			
			SPI1_SS1_B	O	4			
			UT6_T1_B	IO	5			
			SD_D5_D	IO	6			
			ETH_MDIO_A	IO	7			
P6_6	D16	E6	GPIO6_6	IO	0	P6_6	LVCMOS	VDD_IO_1V8
			OSPI0_D6_C	IO	1			
			UART0_CTS_B	I	2			
			SPI1_SS2_B	O	4			
			UT7_T0_B	IO	5			
			SD_D6_D	IO	6			
			ETH_MDC_A	O	7			
P6_7	C17	A9	GPIO6_7	IO	0	P6_7	LVCMOS	VDD_IO_1V8
			OSPI0_D7_C	IO	1			
			UART0_RTS_B	O	2			
			PDM_C2_A	O	3			
			SPI1_SS3_B	O	4			
			UT7_T1_B	IO	5			
			SD_D7_D	IO	6			
			ETH_CRS_DV_A	I	7			
P7_0	B18	B8	GPIO7_0	IO	0	P7_0	LVCMOS	VDD_IO_1V8
			CMP3_OUT_A	O	2			
			SPI0_MISO_C	IO	3			
			I2C0_SDA_C	IO	4			
			UT8_T0_B	IO	5			
			SD_CMD_A	IO	6			
			CAN_RXD_A	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P7_1	D18	B3	GPIO7_1	IO	0	P7_1	LVCMOS	VDD_IO_1V8
			CMP2_OUT_A	O	2			
			SPI0_MOSI_C	IO	3			
			I2C0_SCL_C	IO	4			
			UT8_T1_B	IO	5			
			SD_CLK_A	O	6			
			CAN_TXD_A	O	7			
P7_2	F18	D1	GPIO7_2	IO	0	P7_2	LVCMOS	VDD_IO_1V8
			UART3_CTS_B	I	2			
			CMP1_OUT_A	O	3			
			SPI0_SCLK_C	IO	4			
			I2C1_SDA_C	IO	5			
			UT9_T0_B	IO	6			
			SD_RST_A	O	7			
P7_3	A19	A8	GPIO7_3	IO	0	P7_3	LVCMOS	VDD_IO_1V8
			UART3_RTS_B	O	2			
			CMP0_OUT_A	O	3			
			SPI0_SS0_C	IO	4			
			I2C1_SCL_C	IO	5			
			UT9_T1_B	IO	6			
			CAN_STBY_A	O	7			
P7_4	M22	T1	GPIO7_4	IO	0	P7_4	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPUART_CTS_A	I	2			
			LPPDM_C2_A	O	3			
			LPSPI_MISO_A	IO	4			
			LPI2C_SCL_A	I	5			
			UT10_T0_B	IO	6			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P7_5	L19	T2	GPIO7_5	IO	0	P7_5	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPUART_RTS_A	O	2			
			LPPDM_D2_A	I	4			
			LPSPI_MOSI_A	IO	5			
			LPI2C_SDA_A	IO	6			
			UT10_T1_B	IO	7			
P7_6	N27	U3	GPIO7_6	IO	0	P7_6	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPUART_RX_A	I	2			
			LPPDM_C3_A	O	4			
			LPSPI_SCLK_A	IO	5			
			I3C_SDA_D	IO	6			
			UT11_T0_B	IO	7			
P7_7	N25	U1	GPIO7_7	IO	0	P7_7	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPUART_TX_A	O	2			
			LPPDM_D3_A	I	4			
			LPSPI_SS_A	IO	5			
			I3C_SCL_D	IO	6			
			UT11_T1_B	IO	7			
P8_0	C19	B7	GPIO8_0	IO	0	P8_0	LVCMOS	VDD_IO_1V8
			OSPI1_SCLKN_C	O	1			
			AUDIO_CLK_A	I	2			
			FAULT0_B	I	3			
			LPCAM_D0_A	I	4			
			SD_D0_C	IO	5			
			CDC_D0_A	O	6			
			CAM_D0_B	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P8_1	E19	C2	GPIO8_1	IO	0	P8_1	LVCMOS	VDD_IO_1V8
			I2S2_SDI_A	I	1			
			FAULT1_B	I	2			
			LPCAM_D1_A	I	3			
			SD_D1_C	IO	4			
			CDC_D1_A	O	5			
			CAM_D1_B	I	6			
P8_2	B20	C3	GPIO8_2	IO	0	P8_2	LVCMOS	VDD_IO_1V8
			I2S2_SDO_A	O	1			
			SPI0_SS3_B	O	2			
			FAULT2_B	I	3			
			LPCAM_D2_A	I	4			
			SD_D2_C	IO	5			
			CDC_D2_A	O	6			
			CAM_D2_B	I	7			
P8_3	A21	A7	GPIO8_3	IO	0	P8_3	LVCMOS	VDD_IO_1V8
			I2S2_SCLK_A	O	1			
			SPI1_MISO_B	IO	2			
			FAULT3_B	I	3			
			LPCAM_D3_A	I	4			
			SD_D3_C	IO	5			
			CDC_D3_A	O	6			
			CAM_D3_B	I	7			
P8_4	D20	B4	GPIO8_4	IO	0	P8_4	LVCMOS	VDD_IO_1V8
			I2S2_WS_A	O	1			
			SPI1_MOSI_B	IO	2			
			QEC0_X_B	I	3			
			LPCAM_D4_A	I	4			
			SD_D4_C	IO	5			
			CDC_D4_A	O	6			
			CAM_D4_B	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P8_5	H28	H1	GPIO8_5	IO	0	P8_5	LVCMOS	VDD_IO_1V8
			SPI1_SCLK_B	IO	2			
			QEC0_Y_B	I	3			
			LPCAM_D5_A	I	4			
			SD_D5_C	IO	5			
			CDC_D5_A	O	6			
			CAM_D5_B	I	7			
P8_6	H22	J2	GPIO8_6	IO	0	P8_6	LVCMOS	VDD_IO_1V8
			I2S3_SCLK_B	O	2			
			QEC0_Z_B	I	3			
			LPCAM_D6_A	I	4			
			SD_D6_C	IO	5			
			CDC_D6_A	O	6			
			CAM_D6_B	I	7			
P8_7	H20	J1	GPIO8_7	IO	0	P8_7	LVCMOS	VDD_IO_1V8
			I2S3_WS_B	O	2			
			QEC1_X_B	I	3			
			LPCAM_D7_A	I	4			
			SD_D7_C	IO	5			
			CDC_D7_A	O	6			
			CAM_D7_B	I	7			
P9_0	H18	K2	GPIO9_0	IO	0	P9_0	LVCMOS	VDD_IO_1V8
			I2S3_SDI_B	I	2			
			QEC1_Y_B	I	3			
			SD_CMD_C	IO	4			
			CDC_D8_A	O	5			
			CAM_D8_B	I	6			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P9_1	H16	K1	GPIO9_1	IO	0	P9_1	LVCMOS	VDD_IO_1V8
			LPUART_RX_B	I	1			
			I2S3_SDO_B	O	2			
			QEC1_Z_B	I	3			
			SD_CLK_C	O	4			
			CDC_D9_A	O	5			
			CAM_D9_B	I	6			
P9_2	J27	G5	GPIO9_2	IO	0	P9_2	LVCMOS	VDD_IO_1V8
			LPUART_TX_B	O	1			
			I2S3_SDI_A	I	2			
			SPI2_MISO_B	IO	3			
			QEC2_X_B	I	4			
			SD_RST_C	O	5			
			CDC_D10_A	O	6			
			CAM_D10_B	I	7			
P9_3	J25	H5	GPIO9_3	IO	0	P9_3	LVCMOS	VDD_IO_1V8
			UART7_RX_B	I	2			
			I2S3_SDO_A	O	3			
			SPI2_MOSI_B	IO	4			
			QEC2_Y_B	I	5			
			CDC_D11_A	O	6			
			CAM_D11_B	I	7			
P9_4	J23	J5	GPIO9_4	IO	0	P9_4	LVCMOS	VDD_IO_1V8
			UART7_TX_B	O	1			
			I2S3_SCLK_A	O	2			
			SPI2_SCLK_B	IO	3			
			I2C3_SDA_C	IO	4			
			QEC2_Z_B	I	5			
			CDC_D12_A	O	6			
			CAM_D12_B	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P9_5	J21	L1	GPIO9_5	IO	0	P9_5	LVCMOS	VDD_IO_1V8
			OSPI1_D0_C	IO	1			
			I2S3_WS_A	O	2			
			SPI2_SS0_B	IO	3			
			I2C3_SCL_C	IO	4			
			QEC3_X_B	I	5			
			CDC_D13_A	O	6			
			CAM_D13_B	I	7			
P9_6	K28	K5	GPIO9_6	IO	0	P9_6	LVCMOS	VDD_IO_1V8
			OSPI1_D1_C	IO	1			
			AUDIO_CLK_B	I	2			
			SPI2_SS1_B	O	3			
			I2C3_SDA_B	IO	4			
			QEC3_Y_B	I	5			
			CDC_D14_A	O	6			
			CAM_D14_B	I	7			
P9_7	J19	L5	GPIO9_7	IO	0	P9_7	LVCMOS	VDD_IO_1V8
			OSPI1_D2_C	IO	1			
			UART7_DE_B	O	2			
			SPI2_SS2_B	O	3			
			I2C3_SCL_B	IO	4			
			QEC3_Z_B	I	5			
			CDC_D15_A	O	6			
			CAM_D15_B	I	7			
P10_0	K26	M2	GPIO10_0	IO	0	P10_0	LVCMOS	VDD_IO_1V8
			OSPI1_D3_C	IO	1			
			UART6_DE_B	O	2			
			SPI2_SS3_B	O	3			
			UT0_T0_C	IO	4			
			LPCAM_HSYNC_A	I	5			
			CDC_D16_A	O	6			
			CAM_HSYNC_B	I	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P10_1	K24	M1	GPIO10_1	IO	0	P10_1	LVCMOS	VDD_IO_1V8
			OSPI1_D4_C	IO	1			
			LPI2S_SDI_B	I	3			
			UT0_T1_C	IO	4			
			LPCAM_VSYNC_A	I	5			
			CDC_D17_A	O	6			
			CAM_VSYNC_B	I	7			
P10_2	K22	N1	GPIO10_2	IO	0	P10_2	LVCMOS	VDD_IO_1V8
			OSPI1_D5_C	IO	1			
			LPI2S_SDO_B	O	3			
			UT1_T0_C	IO	4			
			LPCAM_PCLK_A	I	5			
			CDC_D18_A	O	6			
			CAM_PCLK_B	I	7			
P10_3	K20	N2	GPIO10_3	IO	0	P10_3	LVCMOS	VDD_IO_1V8
			OSPI1_D6_C	IO	1			
			LPI2S_SCLK_B	O	3			
			UT1_T1_C	IO	4			
			LPCAM_XVCLK_A	O	5			
			CDC_D19_A	O	6			
			CAM_XVCLK_B	O	7			
P10_4	L27	M5	GPIO10_4	IO	0	P10_4	LVCMOS	VDD_IO_1V8
			OSPI1_D7_C	IO	1			
			LPI2S_WS_B	O	3			
			I2C0_SDA_D	IO	4			
			UT2_T0_C	IO	5			
			ETH_TXD0_B	O	6			
			CDC_D20_A	O	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P10_5	L25	N5	GPIO10_5	IO	0	P10_5	LVCMOS	VDD_IO_1V8
			UART6_RX_A	I	1			
			I2S2_SDI_B	I	2			
			SPI3_MISO_B	IO	3			
			I2C0_SCL_D	IO	4			
			UT2_T1_C	IO	5			
			ETH_TXD1_B	O	6			
			CDC_D21_A	O	7			
P10_6	L23	P5	GPIO10_6	IO	0	P10_6	LVCMOS	VDD_IO_1V8
			UART6_TX_A	O	1			
			I2S2_SDO_B	O	2			
			SPI3_MOSI_B	IO	3			
			I2C1_SDA_D	IO	4			
			UT3_T0_C	IO	5			
			ETH_TXEN_B	O	6			
			CDC_D22_A	O	7			
P10_7	L21	P1	GPIO10_7	IO	0	P10_7	LVCMOS	VDD_IO_1V8
			UART7_RX_A	I	1			
			I2S2_SCLK_B	O	2			
			SPI3_SCLK_B	IO	3			
			I2C1_SCL_D	IO	4			
			UT3_T1_C	IO	5			
			CDC_D23_A	O	6			
			OSPI1_RXDS_C	IO	7			
P11_0	M28	P2	GPIO11_0	IO	0	P11_0	LVCMOS	VDD_IO_1V8
			OSPI1_D0_A	IO	1			
			UART7_TX_A	O	2			
			I2S2_WS_B	O	3			
			SPI3_SS0_B	IO	4			
			UT4_T0_C	IO	5			
			ETH_REFCLK_B	IO	6			
			CDC_D0_B	O	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P11_1	J17	R1	GPIO11_1	IO	0	P11_1	LVCMOS	VDD_IO_1V8
			OSPI1_D1_A	IO	1			
			UART7_DE_A	O	2			
			SPI3_SS1_B	O	3			
			UT4_T1_C	IO	4			
			ETH_MDIO_B	IO	5			
			CDC_D1_B	O	6			
P11_2	M26	R2	GPIO11_2	IO	0	P11_2	LVCMOS	VDD_IO_1V8
			OSPI1_D2_A	IO	1			
			UART6_DE_A	O	2			
			LPPDM_C2_B	O	3			
			SPI3_SS2_B	O	4			
			UT5_T0_C	IO	5			
			ETH_MDC_B	O	6			
			CDC_D2_B	O	7			
P11_3	M24	R5	GPIO11_3	IO	0	P11_3	LVCMOS	VDD_IO_1V8
			OSPI1_D3_A	IO	1			
			UART5_RX_B	I	2			
			LPPDM_C3_B	O	3			
			SPI3_SS3_B	O	4			
			UT5_T1_C	IO	5			
			ETH_RXD0_B	I	6			
			CDC_D3_B	O	7			
P11_4	N19	K8	GPIO11_4	IO	0	P11_4	LVCMOS	VDD_IO_1V8
			OSPI1_D4_A	IO	1			
			UART5_TX_B	O	2			
			PDM_C2_B	O	3			
			LPSPI_MISO_B	IO	4			
			UT6_T0_C	IO	5			
			ETH_RXD1_B	I	6			
			CDC_D4_B	O	7			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P11_5	P20	J9	GPIO11_5	IO	0	P11_5	LVCMOS	VDD_IO_1V8
			OSPI1_D5_A	IO	1			
			UART6_RX_B	I	2			
			PDM_C3_B	O	3			
			LPSPI_MOSI_B	IO	4			
			UT6_T1_C	IO	5			
			ETH_CRS_DV_B	I	6			
			CDC_D5_B	O	7			
P11_6	K16	R6	GPIO11_6	IO	0	P11_6	LVCMOS	VDD_IO_1V8
			OSPI1_D6_A	IO	1			
			UART6_TX_B	O	2			
			LPPDM_D2_B	I	3			
			LPSPI_SCLK_B	IO	4			
			UT7_T0_C	IO	5			
			ETH_RST_B	O	6			
			CDC_D6_B	O	7			
P11_7	R21	L9	GPIO11_7	IO	0	P11_7	LVCMOS	VDD_IO_1V8
			OSPI1_D7_A	IO	1			
			UART5_DE_B	O	2			
			LPPDM_D3_B	I	3			
			LPSPI_SS_B	IO	4			
			UT7_T1_C	IO	5			
			ETH_IRQ_B	I	6			
			CDC_D7_B	O	7			
P12_0	D2	F19	GPIO12_0	IO	0	P12_0	LVCMOS	VDD_IO_1V8
			OSPI0_SCLK_C	O	1			
			AUDIO_CLK_C	I	2			
			I2S1_SDI_B	I	3			
			UT8_T0_C	IO	4			
			CDC_D8_B	O	5			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P12_1	D4	E18	GPIO12_1	IO	0	P12_1	LVCMOS	VDD_IO_1V8
			OSPI0_SCLKN_C	O	1			
			UART4_RX_B	I	2			
			I2S1_SDO_B	O	3			
			UT8_T1_C	IO	4			
			CDC_D9_B	O	5			
P12_2	C1	E15	GPIO12_2	IO	0	P12_2	LVCMOS	VDD_IO_1V8
			OSPI0_RXDS_C	IO	1			
			UART4_TX_B	O	2			
			I2S1_SCLK_B	O	3			
			UT9_T0_C	IO	4			
			CDC_D10_B	O	5			
P12_3	E7	D18	GPIO12_3	IO	0	P12_3	LVCMOS	VDD_IO_1V8
			OSPI0_SS0_C	O	1			
			UART4_DE_B	O	2			
			I2S1_WS_B	O	3			
			UT9_T1_C	IO	4			
			CDC_D11_B	O	5			
P12_4	A15	F5	GPIO12_4	IO	0	P12_4	LVCMOS	VDD_IO_1V8
			OSPI0_SS1_C	O	1			
			SPI3_MISO_A	IO	2			
			UT10_T0_C	IO	3			
			CAN_RXD_C	I	4			
			CDC_D12_B	O	5			
P12_5	B16	A10	GPIO12_5	IO	0	P12_5	LVCMOS	VDD_IO_1V8
			SPI3_MOSI_A	IO	2			
			UT10_T1_C	IO	3			
			CAN_TXD_C	O	4			
			CDC_D13_B	O	5			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P12_6	F16	E5	GPIO12_6	IO	0	P12_6	LVCMOS	VDD_IO_1V8
			SPI3_SCLK_A	IO	2			
			UT11_T0_C	IO	3			
			CAN_STBY_C	O	4			
			CDC_D14_B	O	5			
P12_7	E17	D2	GPIO12_7	IO	0	P12_7	LVCMOS	VDD_IO_1V8
			OSPI1_RXDS_B	IO	1			
			SPI3_SS0_A	IO	3			
			UT11_T1_C	IO	4			
			CDC_D15_B	O	5			
P13_0	F2	G18	GPIO13_0	IO	0	P13_0	LVCMOS	VDD_IO_1V8
			OSPI1_D0_B	IO	1			
			SPI3_SS1_A	O	3			
			QEC0_X_C	I	4			
			SD_D0_B	IO	5			
			CDC_D16_B	O	6			
P13_1	F6	G15	GPIO13_1	IO	0	P13_1	LVCMOS	VDD_IO_1V8
			OSPI1_D1_B	IO	1			
			SPI3_SS2_A	O	2			
			QEC0_Y_C	I	3			
			SD_D1_B	IO	4			
			CDC_D17_B	O	5			
P13_2	F8	F15	GPIO13_2	IO	0	P13_2	LVCMOS	VDD_IO_1V8
			OSPI1_D2_B	IO	1			
			SPI3_SS3_A	O	2			
			QEC0_Z_C	I	3			
			SD_D2_B	IO	4			
			CDC_D18_B	O	5			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P13_3	E1	E13	GPIO13_3	IO	0	P13_3	LVCMOS	VDD_IO_1V8
			OSPI1_D3_B	IO	1			
			SPI2_SS3_A	O	2			
			QEC1_X_C	I	3			
			SD_D3_B	IO	4			
			CDC_D19_B	O	5			
P13_4	E3	E14	GPIO13_4	IO	0	P13_4	LVCMOS	VDD_IO_1V8
			OSPI1_D4_B	IO	1			
			LPI2S_SDI_C	I	2			
			QEC1_Y_C	I	3			
			SD_D4_B	IO	4			
			CDC_D20_B	O	5			
P13_5	A5	A17	GPIO13_5	IO	0	P13_5	LVCMOS	VDD_IO_1V8
			OSPI1_D5_B	IO	1			
			LPI2S_SDO_C	O	2			
			QEC1_Z_C	I	3			
			SD_D5_B	IO	4			
			CDC_D21_B	O	5			
P13_6	D10	B15	GPIO13_6	IO	0	P13_6	LVCMOS	VDD_IO_1V8
			OSPI1_D6_B	IO	1			
			LPI2S_SCLK_C	O	2			
			QEC2_X_C	I	3			
			SD_D6_B	IO	4			
			CDC_D22_B	O	5			
P13_7	C9	A15	GPIO13_7	IO	0	P13_7	LVCMOS	VDD_IO_1V8
			OSPI1_D7_B	IO	1			
			LPI2S_WS_C	O	2			
			QEC2_Y_C	I	3			
			SD_D7_B	IO	4			
			CDC_D23_B	O	5			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P14_0	A17	B9	GPIO14_0	IO	0	P14_0	LVCMOS	VDD_IO_1V8
			OSPI1_SCLK_B	O	1			
			UART6_RX_C	I	2			
			QEC2_Z_C	I	3			
			SD_CMD_B	IO	4			
P14_1	G27	H2	GPIO14_1	IO	0	P14_1	LVCMOS	VDD_IO_1V8
			OSPI1_SCLKN_B	O	1			
			UART6_TX_C	O	2			
			QEC3_X_C	I	4			
			SD_CLK_B	O	5			
P14_2	G25	G1	GPIO14_2	IO	0	P14_2	LVCMOS	VDD_IO_1V8
			OSPI1_SS0_B	O	1			
			UART7_RX_C	I	2			
			QEC3_Y_C	I	4			
			SD_RST_B	O	5			
P14_3	P18	R7	GPIO14_3	IO	0	P14_3	LVCMOS	VDD_IO_1V8
			OSPI1_SS1_B	O	1			
			UART7_TX_C	O	2			
			QEC3_Z_C	I	4			
P14_4	R19	R8	GPIO14_4	IO	0	P14_4	LVCMOS	VDD_IO_1V8
			CMP3_OUT_B	O	1			
			SPI1_MISO_C	IO	2			
			FAULT0_C	I	3			
P14_5	M16	L11	GPIO14_5	IO	0	P14_5	LVCMOS	VDD_IO_1V8
			CMP2_OUT_B	O	1			
			SPI1_MOSI_C	IO	2			
			FAULT1_C	I	3			
P14_6	L15	K12	GPIO14_6	IO	0	P14_6	LVCMOS	VDD_IO_1V8
			CMP1_OUT_B	O	1			
			SPI1_SCLK_C	IO	2			
			FAULT2_C	I	3			

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P14_7	R17	L12	GPIO14_7	IO	0	P14_7	LVCMOS	VDD_IO_1V8
			CMP0_OUT_B	O	1			
			SPI1_SS0_C	IO	2			
			FAULT3_C	I	3			
P15_0	K18	V2	GPIOV_0	IO		LPGPIO_CTRL_0	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPTMR0_CLK_IO	IO				
P15_1	N23	W2	GPIOV_1	IO		LPGPIO_CTRL_1	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPTMR1_CLK_IO	IO				
P15_2	N21	U2	GPIOV_2	IO		LPGPIO_CTRL_2	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPTMR2_CLK_IO	IO				
P15_3	P26	V1	GPIOV_3	IO		LPGPIO_CTRL_3	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPTMR3_CLK_IO	IO				
P15_4	R27	V3	GPIOV_4	IO		LPGPIO_CTRL_4	LVCMOS	VDD_IO_1V8
P15_5	J15	W4	GPIOV_5	IO		LPGPIO_CTRL_5	LVCMOS	VDD_IO_1V8
P15_6	L17	V4	GPIOV_6	IO		LPGPIO_CTRL_6	LVCMOS	VDD_IO_1V8
P15_7	M18	W5	GPIOV_7	IO		LPGPIO_CTRL_7	LVCMOS	VDD_IO_1V8
SEUART_RX	B2	A14	SEUART_RX	I			LVCMOS	VDD_IO_1V8
SEUART_TX	C5	A13	SEUART_TX	O			LVCMOS	VDD_IO_1V8
N.C.	B26, B28, C15, C23, C27, D26, D28, E21, E23, F24, F28, G11	B1, C1, J8, M18	N.C.	N.C.				
RESERVED[(b)]	C3	J11	RESERVED	RSVD				
N/A	A27, D24							
NSRST	D6	J12	NSRST	I			LVCMOS	VDD_IO_1V8
POR_N	K10	U18	POR_N	I			LVCMOS	VDD_IO_1V8
HFXO_P	A23	A4	HFXO_P	I			LVCMOS	VDD_IO_1V8
HFXO_N	A25	A3	HFXO_N	O			LVCMOS	VDD_IO_1V8
LFXO_P	R5	W17	LFXO_P	I			LVCMOS	VDD_IO_1V8

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
LFXO_N	P6	V17	LFXO_N	O			LVCMOS	VDD_IO_1V8
VREF_P	M4	N18	VREF_P	A				
VREF_N	M2	See(c)	VREF_N	A				
VDD_MAIN	L5	P19	VDD_MAIN	PWR				
VDD_BATT	K12	T18	VDD_BATT	PWR				
VDD_BUCK	P2	R18	VDD_BUCK	PWR				
VDD_IO_FLEX	P28	W1	VDD_IO_FLEX	PWR				
VDD_IO_1V8	C13, F4, P24	A5, D19, W3	VDD_IO_1V8	PWR				
VDD_CORE_0V8	A13, G3, H24, N17	B5, E1, E19, V6	VDD_CORE_0V8	PWR				
VREG_MIPI_0V8	L13	W13	VREG_MIPI_0V8	PWR				
VDD_MIPI_1V8	M12	W12	VDD_MIPI_1V8	PWR				
VDD_USB_3V3	P14	W8	VDD_USB_3V3	PWR				
VDD_SX_0V8	C21	A2	VDD_SX_0V8	PWR				
VDD_PLL_0V8	C25	A1	VDD_PLL_0V8	PWR				
VSS	B12, B22, B24, D22, E25, E27, F26, G1, H26, L9, M20, R9, R13, R25	B2, C18, J10, K9, K10, K11, L2, L10, V12	VSS	GND				
VSS_BUCK	R3	V19	VSS_BUCK	GND				
VSS_ANA	N1	P18	VSS_ANA	GND				
VREG_CORE_0V8	M6	W18	VREG_CORE_0V8	PWR				
VREG_AON	L11	U17	VREG_AON	PWR				
VREG_LP_1V8	N5	W19	VREG_LP_1V8	PWR				
VREG_DIG_1V8	J11	U19	VREG_DIG_1V8	PWR				
VREG_AUX_1V8		V18	VREG_AUX_1V8	PWR				
VREG_MIPI_1V8	G13	N19	VREG_MIPI_1V8	PWR				
VSW	P4, R1	T19	VSW	PWR				
USB_REXT	K14	V8	USB_REXT	P			USBPHY	VDD_USB_3V3
USB_DP	R15	W7	USB_DP	IO			USBPHY	VDD_USB_3V3
USB_DM	N15	V7	USB_DM	IO			USBPHY	VDD_USB_3V3

Pin Name (1)	WLCSP208 Pin Location (2)	FBGA194 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
USB_VBUS	H14	W6	USB_VBUS	A			USBPHY	VDD_USB_3V3
USB_IO_ID	P16	R9	USB_IO_ID	A			USBPHY	VDD_USB_3V3
MIPI_REXT	J13	V13	MIPI_REXT	P			DSIPHY	VDD_MIPI_1V8
MIPICSI_0_P	P8	W14	MIPICSI_0_P	I			CSIPHY	VDD_MIPI_1V8
MIPICSI_0_N	R7	V14	MIPICSI_0_N	I			CSIPHY	VDD_MIPI_1V8
MIPICSI_1_P	M10	W15	MIPICSI_1_P	I			CSIPHY	VDD_MIPI_1V8
MIPICSI_1_N	N9	V15	MIPICSI_1_N	I			CSIPHY	VDD_MIPI_1V8
MIPICSI_C_P	M8	W16	MIPICSI_C_P	I			CSIPHY	VDD_MIPI_1V8
MIPICSI_C_N	N7	V16	MIPICSI_C_N	I			CSIPHY	VDD_MIPI_1V8
MIPIDSI_0_P	P10	W11	MIPIDSI_0_P	O			DSIPHY	VDD_MIPI_1V8
MIPIDSI_0_N	N11	V11	MIPIDSI_0_N	O			DSIPHY	VDD_MIPI_1V8
MIPIDSI_1_P	N13	W9	MIPIDSI_1_P	O			DSIPHY	VDD_MIPI_1V8
MIPIDSI_1_N	M14	V9	MIPIDSI_1_N	O			DSIPHY	VDD_MIPI_1V8
MIPIDSI_C_P	R11	W10	MIPIDSI_C_P	O			DSIPHY	VDD_MIPI_1V8
MIPIDSI_C_N	P12	V10	MIPIDSI_C_N	O			DSIPHY	VDD_MIPI_1V8

a. Default mode after reset.
b. This pin must be connected to VSS.
c. Connected internally to VSS.

The list below describes the column headers:

1. **Pin Name**—Name of the pin. Px_y pins have several functions (mux modes) to select from. The functions of other pins are fixed.
2. **Pin Location**—Pad or ball number of the corresponding device package.
3. **Signal Name**—Signal(s) that can be routed to the particular pin. If a signal is routable to more than one pin, a suffix _A, _B, _C, or _D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set or Pin Group.
4. **Pin Type**—Pin designation (for the multiplexed pins, it depends on the selected mux mode):
   - A—Analog
   - I—Digital Input
   - O—Digital Output
   - IO—Digital Bi-directional (Input/Output)
   - R—Radio frequency
   - RSVD—Reserved
   - P—Passive
   - PWR—Power
   - GND—Ground

- N/A—Not Available. This ball does not exist on the package.
- N.C.—No Connect

5. **Multiplexing Number**—Function number used in the pin configuration registers:
   - 0 is the GPIO function
   - 1 through 7 are possible alternative functions
   - An empty box means Not Applicable
6. **Configuration Register**—Associated pin control register. For more information, see Section 3.9 Signal Multiplexing and I/O Buffer Configuration.
7. **Buffer Type**—Associated I/O buffer type, if applicable:
   - LVCMOS—1.8-V Low-Voltage CMOS digital I/O buffer
   - Dual-Voltage (Flex) LVCMOS—1.8-V and 3.3-V LVCMOS digital I/O buffer
   - Analog—Analog input or output
   - RF—Radio Frequency input or output
   - USBPHY—HS USB data bus PHY and I/Os
   - CSIPHY—MIPI CSI camera PHY and I/Os
   - DSIPHY—MIPI DSI display PHY and I/Os
8. **Power Rail**—I/O buffer power supply, if applicable.

4.3 Pin Function Multiplexing

Table 4-2 describes the pin functions multiplexing options.

Table 4-2 Pin Function Multiplexing

Pin Name	0	1	2	3	4	5	6	7
P0_0	GPIO0_0	OSPI0_D0_A	UART0_RX_A	I3C_SDA_A	UT0_T0_A	LPCAM_HSYNC_B	CAM_HSYNC_A	ANA_S0
P0_1	GPIO0_1	OSPI0_D1_A	UART0_TX_A	I3C_SCL_A	UT0_T1_A	LPCAM_VSYNC_B	CAM_VSYNC_A	ANA_S1
P0_2	GPIO0_2	OSPI0_D2_A	UART0_CTS_A	I2C0_SDA_A	UT1_T0_A	LPCAM_PCLK_B	CAM_PCLK_A	ANA_S2
P0_3	GPIO0_3	OSPI0_D3_A	UART0_RTS_A	I2C0_SCL_A	UT1_T1_A	LPCAM_XVCLK_B	CAM_XVCLK_A	ANA_S3
P0_4	GPIO0_4	OSPI0_D4_A	UART1_RX_A	PDM_D0_A	I2C1_SDA_A	UT2_T0_A	CAN_RXD_B	ANA_S4
P0_5	GPIO0_5	OSPI0_D5_A	UART1_TX_A	PDM_C0_A	I2C1_SCL_A	UT2_T1_A	CAN_TXD_B	ANA_S5
P0_6	GPIO0_6	OSPI0_D6_A	UART1_CTS_A	PDM_D1_A	I2C2_SCL_A	UT3_T0_A	CAN_STBY_B	ANA_S6
P0_7	GPIO0_7	OSPI0_D7_A	UART1_RTS_A	PDM_C1_A	I2C2_SDA_A	UT3_T1_A	CDC_DE_B	ANA_S7
P1_0	GPIO1_0	UART2_RX_A	SPI0_MISO_A	I2C3_SDA_A	UT4_T0_A	LPCAM_HSYNC_C	ETH_RXD0_C	ANA_S8
P1_1	GPIO1_1	UART2_TX_A	SPI0_MOSI_A	I2C3_SCL_A	UT4_T1_A	LPCAM_VSYNC_C	ETH_RXD1_C	ANA_S9
P1_2	GPIO1_2	UART3_RX_A	SPI0_SCLK_A	I3C_SDA_B	UT5_T0_A	LPCAM_PCLK_C	ETH_RST_C	ANA_S10
P1_3	GPIO1_3	UART3_TX_A	SPI0_SS0_A	I3C_SCL_B	UT5_T1_A	LPCAM_XVCLK_C	ETH_TXD0_C	ANA_S11
P1_4	GPIO1_4	OSPI0_SS0_A	UART0_RX_B	SPI0_SS1_A	UT6_T0_A	LPCAM_D0_C	ETH_TXD1_C	ANA_S12
P1_5	GPIO1_5	OSPI0_SS1_A	UART0_TX_B	SPI0_SS2_A	UT6_T1_A	LPCAM_D1_C	ETH_TXEN_C	ANA_S13
P1_6	GPIO1_6	OSPI0_RXDS_B	UART1_RX_B	I2S0_SDI_A	UT7_T0_A	LPCAM_D2_C	ETH_IRQ_C	ANA_S14
P1_7	GPIO1_7	OSPI0_SCLK_A	UART1_TX_B	I2S0_SDO_A	UT7_T1_A	LPCAM_D3_C	ETH_REFCLK_C	ANA_S15
P2_0	GPIO2_0	OSPI0_D0_B	UART2_RX_B	LPPDM_D0_A	UT8_T0_A	LPCAM_D4_C	ETH_MDIO_C	ANA_S16
P2_1	GPIO2_1	OSPI0_D1_B	UART2_TX_B	LPPDM_C0_A	UT8_T1_A	LPCAM_D5_C	ETH_MDC_C	ANA_S17
P2_2	GPIO2_2	OSPI0_D2_B	UART3_RX_B	LPPDM_D1_A	UT9_T0_A	LPCAM_D6_C	ETH_CRS_DV_C	ANA_S18
P2_3	GPIO2_3	OSPI0_D3_B	UART3_TX_B	LPPDM_C1_A	UT9_T1_A	LPCAM_D7_C	CDC_PCLK_B	ANA_S19
P2_4	GPIO2_4	OSPI0_D4_B	LPI2S_SDI_A	SPI1_MISO_A	UT10_T0_A	LPCAM_D0_B	CAM_D0_A	ANA_S20
P2_5	GPIO2_5	OSPI0_D5_B	LPI2S_SDO_A	SPI1_MOSI_A	UT10_T1_A	LPCAM_D1_B	CAM_D1_A	ANA_S21
P2_6	GPIO2_6	OSPI0_D6_B	LPI2S_SCLK_A	SPI1_SCLK_A	UT11_T0_A	LPCAM_D2_B	CAM_D2_A	ANA_S22
P2_7	GPIO2_7	OSPI0_D7_B	LPI2S_WS_A	SPI1_SS0_A	UT11_T1_A	LPCAM_D3_B	CAM_D3_A	ANA_S23
P3_0	GPIO3_0	OSPI0_SCLK_B	UART4_RX_A	PDM_D0_B	I2S0_SCLK_A	QEC0_X_A	LPCAM_D4_B	CAM_D4_A
P3_1	GPIO3_1	OSPI0_SCLKN_B	UART4_TX_A	PDM_C0_B	I2S0_WS_A	QEC0_Y_A	LPCAM_D5_B	CAM_D5_A
P3_2	GPIO3_2	OSPI0_SS0_B	PDM_D1_B	I2S1_SDI_A	I3C_SDA_C	QEC0_Z_A	LPCAM_D6_B	CAM_D6_A
P3_3	GPIO3_3	OSPI0_SS1_B	PDM_C1_B	I2S1_SDO_A	I3C_SCL_C	QEC1_X_A	LPCAM_D7_B	CAM_D7_A

Pin Name	0	1	2	3	4	5	6	7
P3_4	GPIO3_4	OSPI0_RXDS_A	UART5_RX_A	LPPDM_C0_B	I2S1_SCLK_A	I2C0_SCL_B	QEC1_Y_A	CAM_D8_A
P3_5	GPIO3_5	OSPI0_SCLKN_A	UART5_TX_A	LPPDM_D0_B	SPI0_SS1_B	I2C0_SDA_B	QEC1_Z_A	CAM_D9_A
P3_6	GPIO3_6	RESERVED	LPUART_CTS_B	LPPDM_C1_B	SPI0_SS2_B	I2C1_SDA_B	QEC2_X_A	CAM_D10_A
P3_7	GPIO3_7	RESERVED	LPUART_RTS_B	LPPDM_D1_B	SPI1_SS1_A	I2C1_SCL_B	QEC2_Y_A	CAM_D11_A
P4_0	GPIO4_0	RESERVED		I2S1_WS_A	SPI1_SS2_A	QEC2_Z_A	CDC_VSYNC_B	CAM_D12_A
P4_1	GPIO4_1	RESERVED	I2S0_SDI_B	SPI1_SS3_A	QEC3_X_A	SD_CLK_D	CDC_HSYNC_B	CAM_D13_A
P4_2	GPIO4_2	RESERVED		I2S0_SDO_B	SPI2_MISO_A	QEC3_Y_A	SD_CMD_D	CAM_D14_A
P4_3	GPIO4_3	RESERVED		I2S0_SCLK_B	SPI2_MOSI_A	QEC3_Z_A	SD_RST_D	CAM_D15_A
P4_4	GPIO4_4	JTAG_TCK	I2S0_WS_B	SPI2_SCLK_A	FAULT0_A			
P4_5	GPIO4_5	JTAG_TMS	SPI2_SS0_A	FAULT1_A				
P4_6	GPIO4_6	JTAG_TDI	SPI2_SS1_A	FAULT2_A				
P4_7	GPIO4_7	JTAG_TDO	SPI2_SS2_A	FAULT3_A				
P5_0	GPIO5_0	OSPI1_RXDS_A	UART4_RX_C	PDM_D2_A	SPI0_MISO_B	I2C2_SDA_B	UT0_T0_B	SD_D0_A
P5_1	GPIO5_1	OSPI1_SS0_A	UART4_TX_C	PDM_D3_A	SPI0_MOSI_B	I2C2_SCL_B	UT0_T1_B	SD_D1_A
P5_2	GPIO5_2	OSPI1_SCLKN_A	UART5_RX_C	PDM_C3_A	SPI0_SS0_B	LPI2C_SCL_B	UT1_T0_B	SD_D2_A
P5_3	GPIO5_3	OSPI1_SCLK_A	UART5_TX_C	SPI0_SCLK_B	LPI2C_SDA_B	UT1_T1_B	SD_D3_A	CDC_PCLK_A
P5_4	GPIO5_4	OSPI1_SS1_A	UART3_CTS_A	PDM_D2_B	SPI0_SS3_A	UT2_T0_B	SD_D4_A	CDC_DE_A
P5_5	GPIO5_5	OSPI1_SCLK_C	UART3_RTS_A	PDM_D3_B	UT2_T1_B	SD_D5_A	ETH_RXD0_A	CDC_HSYNC_A
P5_6	GPIO5_6	RESERVED	UART1_CTS_B	I2C2_SCL_C	UT3_T0_B	SD_D6_A	ETH_RXD1_A	CDC_VSYNC_A
P5_7	GPIO5_7	OSPI1_SS0_C	UART1_RTS_B	I2C2_SDA_C	UT3_T1_B	SD_D7_A	ETH_RST_A	
P6_0	GPIO6_0	OSPI0_D0_C	UART4_DE_A	PDM_D0_C	UT4_T0_B	SD_D0_D	ETH_TXD0_A	
P6_1	GPIO6_1	OSPI0_D1_C	UART5_DE_A	PDM_C0_C	UT4_T1_B	SD_D1_D	ETH_TXD1_A	
P6_2	GPIO6_2	OSPI0_D2_C	UART2_CTS_A		PDM_D1_C	UT5_T0_B	SD_D2_D	ETH_TXEN_A
P6_3	GPIO6_3	OSPI0_D3_C	UART2_RTS_A		PDM_C1_C	UT5_T1_B	SD_D3_D	ETH_IRQ_A
P6_4	GPIO6_4	OSPI0_D4_C	UART2_CTS_B		SPI1_SS0_B	UT6_T0_B	SD_D4_D	ETH_REFCLK_A
P6_5	GPIO6_5	OSPI0_D5_C	UART2_RTS_B		SPI1_SS1_B	UT6_T1_B	SD_D5_D	ETH_MDIO_A
P6_6	GPIO6_6	OSPI0_D6_C	UART0_CTS_B		SPI1_SS2_B	UT7_T0_B	SD_D6_D	ETH_MDC_A
P6_7	GPIO6_7	OSPI0_D7_C	UART0_RTS_B	PDM_C2_A	SPI1_SS3_B	UT7_T1_B	SD_D7_D	ETH_CRS_DV_A
P7_0	GPIO7_0		CMP3_OUT_A	SPI0_MISO_C	I2C0_SDA_C	UT8_T0_B	SD_CMD_A	CAN_RXD_A
P7_1	GPIO7_1		CMP2_OUT_A	SPI0_MOSI_C	I2C0_SCL_C	UT8_T1_B	SD_CLK_A	CAN_TXD_A
P7_2	GPIO7_2		UART3_CTS_B	CMP1_OUT_A	SPI0_SCLK_C	I2C1_SDA_C	UT9_T0_B	SD_RST_A
P7_3	GPIO7_3		UART3_RTS_B	CMP0_OUT_A	SPI0_SS0_C	I2C1_SCL_C	UT9_T1_B	CAN_STBY_A
P7_4	GPIO7_4		LPUART_CTS_A	LPPDM_C2_A	LPSPI_MISO_A	LPI2C_SCL_A	UT10_T0_B	

Pin Name	0	1	2	3	4	5	6	7
P7_5	GPIO7_5		LPUART_RTS_A		LPPDM_D2_A	LPSPI_MOSI_A	LPI2C_SDA_A	UT10_T1_B
P7_6	GPIO7_6		LPUART_RX_A		LPPDM_C3_A	LPSPI_SCLK_A	I3C_SDA_D	UT11_T0_B
P7_7	GPIO7_7		LPUART_TX_A		LPPDM_D3_A	LPSPI_SS_A	I3C_SCL_D	UT11_T1_B
P8_0	GPIO8_0	OSPI1_SCLKN_C	AUDIO_CLK_A	FAULT0_B	LPCAM_D0_A	SD_D0_C	CDC_D0_A	CAM_D0_B
P8_1	GPIO8_1	I2S2_SDI_A	FAULT1_B	LPCAM_D1_A	SD_D1_C	CDC_D1_A	CAM_D1_B	
P8_2	GPIO8_2	I2S2_SDO_A	SPI0_SS3_B	FAULT2_B	LPCAM_D2_A	SD_D2_C	CDC_D2_A	CAM_D2_B
P8_3	GPIO8_3	I2S2_SCLK_A	SPI1_MISO_B	FAULT3_B	LPCAM_D3_A	SD_D3_C	CDC_D3_A	CAM_D3_B
P8_4	GPIO8_4	I2S2_WS_A	SPI1_MOSI_B	QEC0_X_B	LPCAM_D4_A	SD_D4_C	CDC_D4_A	CAM_D4_B
P8_5	GPIO8_5	RESERVED	SPI1_SCLK_B	QEC0_Y_B	LPCAM_D5_A	SD_D5_C	CDC_D5_A	CAM_D5_B
P8_6	GPIO8_6	RESERVED	I2S3_SCLK_B	QEC0_Z_B	LPCAM_D6_A	SD_D6_C	CDC_D6_A	CAM_D6_B
P8_7	GPIO8_7	RESERVED	I2S3_WS_B	QEC1_X_B	LPCAM_D7_A	SD_D7_C	CDC_D7_A	CAM_D7_B
P9_0	GPIO9_0	RESERVED	I2S3_SDI_B	QEC1_Y_B	SD_CMD_C	CDC_D8_A	CAM_D8_B	
P9_1	GPIO9_1	LPUART_RX_B	I2S3_SDO_B	QEC1_Z_B	SD_CLK_C	CDC_D9_A	CAM_D9_B	
P9_2	GPIO9_2	LPUART_TX_B	I2S3_SDI_A	SPI2_MISO_B	QEC2_X_B	SD_RST_C	CDC_D10_A	CAM_D10_B
P9_3	GPIO9_3	RESERVED	UART7_RX_B	I2S3_SDO_A	SPI2_MOSI_B	QEC2_Y_B	CDC_D11_A	CAM_D11_B
P9_4	GPIO9_4	UART7_TX_B	I2S3_SCLK_A	SPI2_SCLK_B	I2C3_SDA_C	QEC2_Z_B	CDC_D12_A	CAM_D12_B
P9_5	GPIO9_5	OSPI1_D0_C	I2S3_WS_A	SPI2_SS0_B	I2C3_SCL_C	QEC3_X_B	CDC_D13_A	CAM_D13_B
P9_6	GPIO9_6	OSPI1_D1_C	AUDIO_CLK_B	SPI2_SS1_B	I2C3_SDA_B	QEC3_Y_B	CDC_D14_A	CAM_D14_B
P9_7	GPIO9_7	OSPI1_D2_C	UART7_DE_B	SPI2_SS2_B	I2C3_SCL_B	QEC3_Z_B	CDC_D15_A	CAM_D15_B
P10_0	GPIO10_0	OSPI1_D3_C	UART6_DE_B	SPI2_SS3_B	UT0_T0_C	LPCAM_HSYNC_A	CDC_D16_A	CAM_HSYNC_B
P10_1	GPIO10_1	OSPI1_D4_C		LPI2S_SDI_B	UT0_T1_C	LPCAM_VSYNC_A	CDC_D17_A	CAM_VSYNC_B
P10_2	GPIO10_2	OSPI1_D5_C		LPI2S_SDO_B	UT1_T0_C	LPCAM_PCLK_A	CDC_D18_A	CAM_PCLK_B
P10_3	GPIO10_3	OSPI1_D6_C		LPI2S_SCLK_B	UT1_T1_C	LPCAM_XVCLK_A	CDC_D19_A	CAM_XVCLK_B
P10_4	GPIO10_4	OSPI1_D7_C		LPI2S_WS_B	I2C0_SDA_D	UT2_T0_C	ETH_TXD0_B	CDC_D20_A
P10_5	GPIO10_5	UART6_RX_A	I2S2_SDI_B	SPI3_MISO_B	I2C0_SCL_D	UT2_T1_C	ETH_TXD1_B	CDC_D21_A
P10_6	GPIO10_6	UART6_TX_A	I2S2_SDO_B	SPI3_MOSI_B	I2C1_SDA_D	UT3_T0_C	ETH_TXEN_B	CDC_D22_A
P10_7	GPIO10_7	UART7_RX_A	I2S2_SCLK_B	SPI3_SCLK_B	I2C1_SCL_D	UT3_T1_C	CDC_D23_A	OSPI1_RXDS_C
P11_0	GPIO11_0	OSPI1_D0_A	UART7_TX_A	I2S2_WS_B	SPI3_SS0_B	UT4_T0_C	ETH_REFCLK_B	CDC_D0_B
P11_1	GPIO11_1	OSPI1_D1_A	UART7_DE_A	SPI3_SS1_B	UT4_T1_C	ETH_MDIO_B	CDC_D1_B	
P11_2	GPIO11_2	OSPI1_D2_A	UART6_DE_A	LPPDM_C2_B	SPI3_SS2_B	UT5_T0_C	ETH_MDC_B	CDC_D2_B
P11_3	GPIO11_3	OSPI1_D3_A	UART5_RX_B	LPPDM_C3_B	SPI3_SS3_B	UT5_T1_C	ETH_RXD0_B	CDC_D3_B
P11_4	GPIO11_4	OSPI1_D4_A	UART5_TX_B	PDM_C2_B	LPSPI_MISO_B	UT6_T0_C	ETH_RXD1_B	CDC_D4_B
P11_5	GPIO11_5	OSPI1_D5_A	UART6_RX_B	PDM_C3_B	LPSPI_MOSI_B	UT6_T1_C	ETH_CRS_DV_B	CDC_D5_B

Pin Name	0	1	2	3	4	5	6	7
P11_6	GPIO11_6	OSPI1_D6_A	UART6_TX_B	LPPDM_D2_B	LPSPI_SCLK_B	UT7_T0_C	ETH_RST_B	CDC_D6_B
P11_7	GPIO11_7	OSPI1_D7_A	UART5_DE_B	LPPDM_D3_B	LPSPI_SS_B	UT7_T1_C	ETH_IRQ_B	CDC_D7_B
P12_0	GPIO12_0	OSPI0_SCLK_C	AUDIO_CLK_C	I2S1_SDI_B	UT8_T0_C	CDC_D8_B		
P12_1	GPIO12_1	OSPI0_SCLKN_C	UART4_RX_B	I2S1_SDO_B	UT8_T1_C	CDC_D9_B		
P12_2	GPIO12_2	OSPI0_RXDS_C	UART4_TX_B	I2S1_SCLK_B	UT9_T0_C	CDC_D10_B		
P12_3	GPIO12_3	OSPI0_SS0_C	UART4_DE_B	I2S1_WS_B	UT9_T1_C	CDC_D11_B		
P12_4	GPIO12_4	OSPI0_SS1_C	SPI3_MISO_A	UT10_T0_C	CAN_RXD_C	CDC_D12_B		
P12_5	GPIO12_5		SPI3_MOSI_A	UT10_T1_C	CAN_TXD_C	CDC_D13_B		
P12_6	GPIO12_6		SPI3_SCLK_A	UT11_T0_C	CAN_STBY_C	CDC_D14_B		
P12_7	GPIO12_7	OSPI1_RXDS_B		SPI3_SS0_A	UT11_T1_C	CDC_D15_B		
P13_0	GPIO13_0	OSPI1_D0_B		SPI3_SS1_A	QEC0_X_C	SD_D0_B	CDC_D16_B	
P13_1	GPIO13_1	OSPI1_D1_B	SPI3_SS2_A	QEC0_Y_C	SD_D1_B	CDC_D17_B		
P13_2	GPIO13_2	OSPI1_D2_B	SPI3_SS3_A	QEC0_Z_C	SD_D2_B	CDC_D18_B		
P13_3	GPIO13_3	OSPI1_D3_B	SPI2_SS3_A	QEC1_X_C	SD_D3_B	CDC_D19_B		
P13_4	GPIO13_4	OSPI1_D4_B	LPI2S_SDI_C	QEC1_Y_C	SD_D4_B	CDC_D20_B		
P13_5	GPIO13_5	OSPI1_D5_B	LPI2S_SDO_C	QEC1_Z_C	SD_D5_B	CDC_D21_B		
P13_6	GPIO13_6	OSPI1_D6_B	LPI2S_SCLK_C	QEC2_X_C	SD_D6_B	CDC_D22_B		
P13_7	GPIO13_7	OSPI1_D7_B	LPI2S_WS_C	QEC2_Y_C	SD_D7_B	CDC_D23_B		
P14_0	GPIO14_0	OSPI1_SCLK_B	UART6_RX_C	QEC2_Z_C	SD_CMD_B			
P14_1	GPIO14_1	OSPI1_SCLKN_B	UART6_TX_C		QEC3_X_C	SD_CLK_B		
P14_2	GPIO14_2	OSPI1_SS0_B	UART7_RX_C		QEC3_Y_C	SD_RST_B		
P14_3	GPIO14_3	OSPI1_SS1_B	UART7_TX_C		QEC3_Z_C			
P14_4	GPIO14_4	CMP3_OUT_B	SPI1_MISO_C	FAULT0_C				
P14_5	GPIO14_5	CMP2_OUT_B	SPI1_MOSI_C	FAULT1_C				
P14_6	GPIO14_6	CMP1_OUT_B	SPI1_SCLK_C	FAULT2_C				
P14_7	GPIO14_7	CMP0_OUT_B	SPI1_SS0_C	FAULT3_C				

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above the values listed under Table 5-1 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Parameter		Condition	Min	Max	Unit
Chip power inputs	VDD_MAIN		-0.3	4.5	V
	VDD_IO_FLEX	1.8-V mode	-0.3	1.98	V
		3.3-V mode	-0.3	3.63	V
	VDD_BATT		-0.3	4.5	V
	VDD_BUCK		-0.3	4.5	V
Input/Output voltage range (1.8 V IOs)			0.3	1.98	V
Maximum junction temperature			-40	150	°C

5.1.1 Maximum Supply Current

Table 5-2 summarizes maximum current consumption ratings at power terminals of the device.

Table 5-2 Maximum Supply Current

Parameter		Condition	Max	Unit
I_{VDD_ALL}	Supply current into all power pins		600	mA
I_{VSS_ALL}	Supply current out of all ground pin(s)		1000	mA
I_{VDD_MAIN}	Supply current rating for the VDD_MAIN pins		10	mA
I_{VDD_VBAT}	Supply current rating for the VDD_BATT pins		1	mA
$I_{VDDIO\_1.8V}$	Supply current rating for the VDD_IO_1V8 pins		500	mA
$I_{VDDIO\_3.3V}$	Supply current rating for the VDD_IO_FLEX pins		200	mA
I_{1V8_IO}	Current sunk, sourced by any 1.8 V I/O pin		65	mA
I_{3V6_IO}	Current sunk, sourced by any 3.6 V I/O pin		35	mA
I_{IO_ALL}	Current sunk, sourced by all pins (I/O and control)		700	mA

5.1.2 Maximum Performance Ratings

Table 5-3 lists the maximum performance per module on this device.

Table 5-3 Maximum Performance Ratings

Parameter		Max	Unit
High-Performance Arm Cortex-M55	M55-HP	400	MHz
High-Efficiency Arm Cortex-M55	M55-HE	160	MHz
Ethos-U55 Neural Processing Units	NPU-HP	400	MHz
	NPU-HE	160	MHz
D/AVE 2D Graphics Processing Unit	GPU2D	400	MHz

Parameter		Max	Unit
Controller Area Network	CANFD	10	Mbps
Ethernet 10/100 Controller	ETH	100	Mbps
Inter-Integrated Circuit	I2C	3.4	Mbps
	LPI2C	400	kbps
Inter-IC Sound	I2S(1)	192	kHz
	LPI2S(1)	192	kHz
MIPI Improved Inter-Integrated Circuit	I3C	20	Mbps
Pulse Density Modulator	PDM	4.8	MHz
	LPPDM	4.8	MHz
Serial Peripheral Interface	SPI	50	MHz
	LPSPI	25	MHz
Universal Asynchronous Receiver/Transmitter	UART	2.5	Mbps
	LPUART	2.5	Mbps
Universal Serial Bus	USB	480	Mbps
Octal SPI	OSPI	100(2)	MHz
Memory Card Controller	SD Card	50(2)	MHz
	eMMC	50(2)	MHz
	SDIO	50(2)	MHz
Camera Parallel Interface	LPCPI	60(2)	MHz
	CPI	60(2)	MHz
MIPI Camera Serial Interface	CSI	2.5	Gbps/lane
Display Parallel Interface	DPI	50	MHz
MIPI Display Serial Interface	DSI	2.5	Gbps/lane
Analog-to-Digital Converters	ADC12	1.25	MSPS
	ADC24	16	kSPS
Digital-to-Analog Converters	DAC12	1	kHz

1. Sampling frequency
2. Some pin multiplex options will reduce the max operating frequency. Please see Cautionary information at the start of Section 4.2 Pin Function Options by Location.

5.2 Operating Conditions

5.2.1 General Operating Conditions

Table 5-4 presents recommended operating conditions over free-air temperature range (unless otherwise noted).

Table 5-4 General Operating Conditions

Parameter			Min	Typ	Max	Unit
VDD_MAIN(1)	Main power supply	When supplied by external wide-range unregulated voltage source.	1.75		4.2	V
		When supplied by external 1.8 V regulated source.	1.75	1.8	1.9	
VDD_BATT(2)	Always-On domain power input		1.75		4.2	V
VDD_BUCK	Internal DC-DC converter power input		1.75		4.2	V
VDD_USB_3V3	USB power input		3.0	3.3	3.6	V

Parameter			Min	Typ	Max	Unit
VDD_IO_FLEX	GPIO flex pads (1.8 V - 3.3 V) power input	1.8-V mode[3]	1.62	1.8	1.98	V
		3.3-V mode	3.0	3.3	4.2	V
VDD_IO_1V8	GPIO standard pads (1.8 V) power input		1.08	1.8	1.98	V
VREG_DIG_1V8[4]	Internal 1.8 V regulator output		1.7	1.8	1.9	V
VREG_AUX_1V8	Auxiliary 1.8 V regulator output		1.7	1.8	1.9	V
VREG_AON[5]	Always-On 0.8 V regulator output		0.76	0.825	0.9	V
VREF_P	External positive voltage reference for ADC		1.2	1.8	1.9	V
VREF_N	External negative voltage reference for ADC		0	0	900	mV
VSS_BUCK	DC-DC converter ground			0		V
VSS_ANA	Analog ground			0		V
VSS	Digital ground			0		V
t_a	Operating ambient temperature range	Extended	-40		85	°C
t_j	Operating junction temperature range	Extended	-40		125	°C

1. BOR and BOD functions not supported below 1.9 V.
2. VDD_BATT must be connected to VDD_MAIN on the printed circuit board.
3. VDD_IO_FLEX should be connected to VDD_IO_1V8 when 1.8-V mode is used.
4. VREG_DIG_1V8 must be bypassed to ground in one of two ways:
   - Through a 1-µF capacitor in series with a 10 Ω resistor if VDD_MAIN supply range is 1.9 V to 4.2 V.
   - Through a 100-nF capacitor if VDD_MAIN supply range is 1.75 V to 1.9 V.
5. VREG_AON must be bypassed to ground through a 1-µF capacitor in series with a 1.0 kΩ resistor.

CAUTION

The decoupling for VREG_AON and VREG_DIG_1V8 pins must be present on the PCB or otherwise the device may be at risk for damage.

NOTE

Refer to Application Note AAPN0027, *PCB Layout Guidelines for Ensemble MCUs and Fusion Processors*, for detailed information about power decoupling for all power pins.

5.2.2 Device Power Modes

5.2.2.1 Power Modes Case Definition

NOTE

Specifications shown in Table 5-5 Power Modes Case Definition are subject to change.

Table 5-5 provides status of each module during different power modes of the device.

Table 5-5 Power Modes Case Definition

Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	Utility					Typ	Units	Typ	Units
GO Modes															
GO_1	All CPU cores running CoreMark at max frequency. Both NPU cores running power indicative inference.	DC-DC	ON	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	45[3]	mA	N/A	
GO_2	Both CPU cores running CoreMark at max frequency. No NPU enabled.											26[3]	mA		
GO_3	Only M55-HP running CoreMark at 400 MHz. No NPU is enabled.		OFF	OFF		OFF						23[3] 57	mA µA/MHz		
GO_4	Only M55-HE running CoreMark at 76.8 MHz.				OFF	ON		HFRC	All OFF			2.2	mA		

Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	Utility					Typ	Units	Typ	Units
	No NPU is enabled.											29	µA/MHz		
GO_5	Only M55-HE running CoreMark at 19.2 MHz. No NPU is enabled.											980 51	µA µA/MHz		
READY Modes															
RDY_1	M55-HP WFI[2] at 400 MHz from PLL. M55-HE powered off.	DC-DC	OFF	OFF	ON	OFF	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	14.5[4]	mA	< 40	ns
RDY_2	M55-HE WFI at 78.6 MHz from HFRC. M55-HP powered off.				OFF	ON		HFRC	All OFF			1.5	mA	< 200	ns
IDLE Modes															
IDLE_1	All CPU cores powered off. 38.4 MHz clock from HFXO.	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral [1]	4.1	mA	2 - 4	µs
IDLE_2	All CPU cores powered off. 600 kHz clock from HFRC.							HFRC				1800	µA	2 - 4	µs
STANDBY Modes															
STBY_1	All CPU cores powered off. HFRC ready.	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral	80	µA	5[5]	µs
STOP Modes															
STOP_1	STOP_2 plus 256KB of M55-HE TCM SRAM retained.	LDO	OFF	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, LPCMP, BOD,	Any interrupt from a powered	4.0	µA	1.1	ms

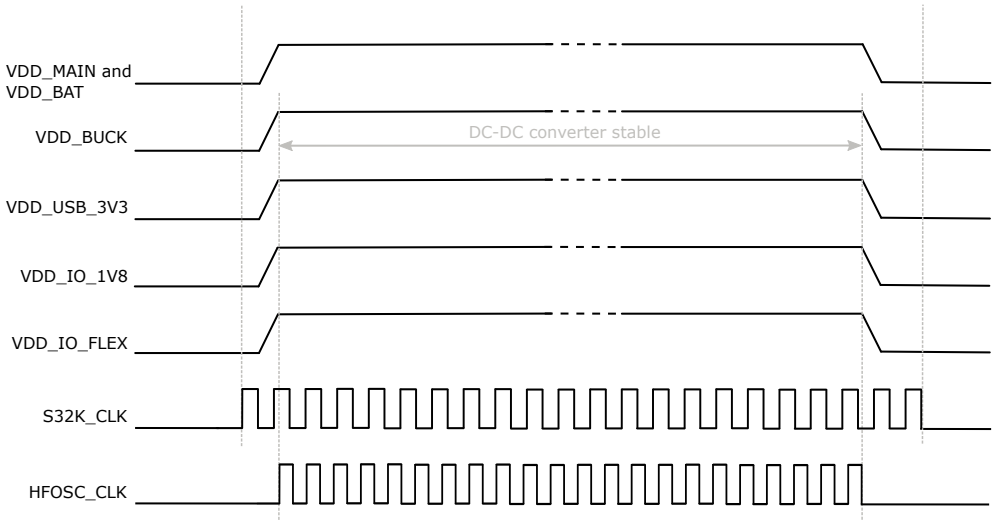
Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	Utility					Typ	Units	Typ	Units
STOP_2	STOP_3 plus 4KB Utility SRAM retained. Boot from MRAM.											1500	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, LPCMP, and LPGPIO active. Boot from MRAM.					OFF				LPGPIO ON		1450	nA		
STOP_4	STOP_5 plus LPRTC running from 32.768 kHz LFXO. Boot from MRAM.						OFF			LPRTC + LPGPIO ON	peripheral	1400	nA	1.1	ms
STOP_5	32.7 kHz LFRC running, all other functions off. Boot from MRAM.							LFRC		LPGPIO ON		1300	nA		
I/O Domain Adder for STOP in all cases		N/A										STOP Mode current adder $I_{VDD\_IO\_1V8}$ when VDD_IO_1V8 = 1.8 V		N/A	
												200	nA		
Cold boot time from Power-On Reset		N/A												130	ms
Power Mode Entry														**Time to Enter Mode**	
Time to enter any STOP Mode		N/A												12.1	ms

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.
2. WFI: Wait for Interrupt.
3. At ACLK = 200 MHz, HCLK = 200 MHz.
4. At ACLK = 100 MHz, HCLK = 50 MHz, PCLK = 25 MHz.
5. Wake interrupt source is LPTIMER.

5.2.3 Power Sequence

Figure 5-1 shows the power-up and power-down sequencing of the device.

Figure 5-1 Power-Up/Power-Down Sequencing



The following restrictions and considerations apply to Figure 5-1 Power-Up/Power-Down Sequencing:

- The power supply ramp-up time (10% to 90%) must be between 1 µs and 1 ms.
- During power-up phase, the VDD_BATT and VDD_MAIN power supplies (must be connected to each other on circuit board) must come up at the same time or before the other supplies. All other power supplies can come up in any order.
- During power-down phase, the VDD_BATT and VDD_MAIN power supplies (must be connected to each other on circuit board) must come down at the same time or after the other supplies. All other power supplies can come down in any order.
- The low-frequency S32K_CLK comes up after VDD_BATT.
- The high-frequency HFOSC_CLK comes up after DC-DC converter is stable.

5.2.4 Reference Voltage Characteristics

Table 5-6 presents reference voltage characteristics.

Table 5-6 Reference Voltage Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{REFBUF_OUT}	Voltage reference output		1.7	1.8	1.9	V
TRIM	Trim step resolution			6	7	mV
C_{LOAD}	Load capacitor		0.8	1		µF
ESR	Equivalent series resistor of C_{LOAD}				0.2	Ω
I_{LOAD}	Static load current				10	mA
I_{LINE_REG}	Line regulation			100	400	ppm/V
T_{Coeff}	Temperature coefficient			50		ppm/°C

Parameter		Conditions	Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	DC	40	60		dB
		100 kHz	20	30		dB
t_{START}	Start-up time				100	µs
$I_{DDA(VREFBUF)}$	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA		200	250	µA
		I_{LOAD} = 1 mA		1.2		mA

5.2.5 Electrical Sensitivity Characteristics

Table 5-7 presents Electrostatic Discharge (ESD) characteristics of the device.

Table 5-7 ESD Characteristics

Parameter		Conditions	Package	Value	Unit
ESD_{HBM}	All pins except for ones listed in(1)	ESD Human Body Model (HBM)	WLCSP/FBGA	±2000	V
ESD_{CDM}	All pins	ESD Charged Device Model (CDM)	WLCSP/FBGA	±250	V

1. ESD_{HBM} for HFXO_P, HFXO_N, LFXO_P, and LFXO_N pins: ±1000 V

Table 5-8 presents latch-up characteristics of the device.

Table 5-8 Latch-up Characteristics

Parameter		Conditions	Value	Unit
I_{LU}	Latch-Up current level	Per JEDEC JESD 78	±100	mA

5.3 Clock Characteristics

5.3.1 External Clock Source Characteristics

Table 5-9 presents the HFXO external clock source characteristics.

Table 5-9 External HFXO Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency		38.4		MHz
C_{CS}	On chip shunt capacitance (programmable by SE only)	4		20	pF
I_{CC}	Current consumption at 3 V		75		µA
t_j	Period jitter			1	ps
t_s	Start-up time		200		µs
t_{acr}	Frequency accuracy		25		ppm

Table 5-10 presents the LFXO external clock source characteristics.

Table 5-10 External LFXO Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency		32.768		kHz
C_{CS}	On chip shunt capacitance (programmable)	2		18	pF
I_{CC}	Current consumption at 3 V		150		nA
t_s	Start-up time		0.1	0.5	s

Parameter		Min	Typ	Max	Unit
t_{acr}	Frequency accuracy		250		ppm

5.3.2 Internal Clock Source Characteristics

Table 5-11 presents the HFRC internal clock source characteristics.

Table 5-11 Internal HFRC Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency at 25 °C and VDD_BATT = 3 V (uncalibrated)	65	76.8	88.8	MHz
f_{cs}	Calibration step		0.768		MHz
t_s	Start-up time		0.5	1	µs
t_j	Frequency variation over temperature and voltage	-2		2	%
I_{CC}	Current consumption		1.1		µA
t_{pj}	RMS period jitter		42		ps

Table 5-12 presents the LFRC internal clock source characteristics.

Table 5-12 Internal LFRC Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency at 25 °C and VDD_BATT = 3 V (factory trimmed)		32.7		kHz
t_j	Frequency variation over temperature and voltage	-4		4	%

5.3.3 PLL Characteristics

Table 5-13 presents the PLL characteristics.

Table 5-13 PLL Characteristics

Parameter		Min	Typ	Max	Unit
f_{C_IN}	Input clock frequency (HFXO only)		38.4		MHz
f_{C_OUT}	Output clock frequency		800		MHz
t_{SET}	Settling time		20		µs
f_{DC}	Output clock duty cycle		50		%
$t_{j(CLK)}$	Output clock jitter (period jitter)			2	ps
I_{CC}	Current consumption at 3 V supply		0.6		mA
$I_{CC(PWR-DWN)}$	Power-down current consumption			0.1	µA

5.4 Memory Characteristics

Table 5-14 presents MRAM characteristics.

Table 5-14 MRAM Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
I_{MRAM}	MRAM current consumption	3.3 V device supply. 25 °C ambient temperature.	Write		30		mA
			Read		10		mA
			Power down		50		µA
N_{MRAMR}	Number of read cycles					Unlimited	Cycles
N_{MRAME}	Number of erase cycles					100000	Cycles
$t_{MRAMW16}$	Write time, non-DMA	Write operation, 16 bytes (minimum number of bytes that can be written in one write operation)			51.6		µs
		Effective write time and rate			3.22		µs
					0.31		MB/s
$t_{MRAMWDMA}$	Write time, DMA	DMA write operation, 128 bytes (maximum DMA cycle payload)			56.1		µs
		Effective write time and rate			438		ns
					2.28		MB/s
$t_{MRAMR16}$	Read time	Read operation, 16 bytes		69		276	ns
				58		232	MB/s

Table 5-15 presents SRAM characteristics.

Table 5-15 SRAM Characteristics

Memory Block	Transaction Data Width (Bytes)	Achievable Read Throughput (MB/s) Read Originating from:		Achievable Write Throughput (MB/s) Write Originating from:	
		M55-HP at 400 MHz	M55-HE at 160 MHz	M55-HP at 400 MHz	M55-HE at 160 MHz
SRAM0	8	1,350	558	1,824	731
SRAM1	8	1,350	558	1,824	731
SRAM2	4	1,600	509	1,600	731
SRAM3	8	3,200	518	3,184	731
SRAM4	4	320	640	640	640
SRAM5	8	417	1,280	1,280	1,278
SRAM6_A	4	317	315	640	640
SRAM6_B	8	418	407	640	640
SRAM7	8	589	454	640	640
SRAM8	8	587	454	640	640
SRAM9_A	4	317	315	640	640
SRAM9_B	8	418	407	640	640

NOTE

User SRAM size and availability is device part number dependent. For more information on SRAM block enabled for each part number and their size, see Section 7 Ordering Information.

5.5 I/O Buffer Characteristics

5.5.1 I/O Parameter Test Conditions

Unless otherwise specified, typical values are taken at t_a = 25 °C and typical supply voltages as specified in Table 5-4 General Operating Conditions. Where statistical variation is relevant and unless otherwise specified, typical values represent parts at the mean of the distribution.

Unless otherwise specified the minimum and maximum values are taken across the full temperature and voltage range. Where statistical variation is relevant and unless otherwise specified, minimum and maximum values represent parts that are three standard deviations away from the mean of the distribution.

All values are based on laboratory characterization.

5.5.2 LVCMOS DC Specifications

Table 5-16 presents the LVCMOS I/O DC specifications.

Table 5-16 LVCMOS DC Specifications (1.8 V Logic)

Parameter		Min	Typ	Max	Unit
Input					
V_{IH}	Input logic high voltage	0.65 × VDD_IO_1V8		VDD_IO_1V8 + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDD_IO_1V8	V
R_{pu}	Input pull-up resistance		50		kΩ
R_{pd}	Input pull-down resistance		50		kΩ
Output					
$V_{OH(DC)}$	DC Output logic high voltage	VDD_IO_1V8 - 0.4			V
$V_{OL(DC)}$	DC Output logic low voltage			0.4	V
I_{OL}	Output drive current (programmable)			2, 4, 8, or 12	mA

5.5.3 Dual-Voltage (Flex) LVCMOS DC Specifications

Table 5-17 presents the dual-voltage (Flex) LVCMOS I/O DC specifications.

Table 5-17 Dual-Voltage (Flex) LVCMOS DC Specifications (1.8 V / 3.3 V Logic)

Parameter		Min	Typ	Max	Unit
Input					
V_{IH}	Input logic high voltage	0.65 × VDD_IO_FLEX (1)		VDD_IO_FLEX(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDD_IO_FLEX (1)	V

Parameter		Min	Typ	Max	Unit
R_{pu}	Input pull-up resistance		50		kΩ
R_{pd}	Input pull-down resistance		50		kΩ
Output					
$V_{OH(DC)}$	DC Output logic high voltage	VDD_IO_FLEX(1) - 0.4			V
$V_{OL(DC)}$	DC Output logic low voltage			0.4	V
I_{OL}	Output drive current (programmable)			2, 4, 8, or 12	mA

1. The voltage supply can be 1.8 V or 3.3 V.

5.5.4 MIPI CSI DC Specifications

The CSI interface (CSIPHY port type) electrical characteristics are compliant with MIPI Alliance Specification for D-PHY, Version 1.2.

5.5.5 MIPI DSI DC Specifications

The DSI interface (DSIPHY port type) electrical characteristics are compliant with MIPI Alliance Specification for D-PHY v1.2.

5.5.6 USB DC Specifications

The USB interface (USBPHY port type) electrical characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

5.6 Analog Peripherals Characteristics

5.6.1 ADC Characteristics

Table 5-18 presents the ADC12 electrical characteristics.

Table 5-18 ADC12 Electrical Characteristics

Parameter		Conditions			Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V from external 3.3 V supply (DC-DC) Internal ADC voltage reference = 1.8 V				12		Bits
f_s	Operational speed				312		5000	kHz
E_G	Gain error (calibrated)					6.1		LSB
E_O	Offset error					0.41		LSB
E_L	Integral nonlinearity						3	LSB
E_D	Differential nonlinearity						2	LSB
ENOB	Effective number of bits		Single-ended	1.25 MSPS (2.5 MHz, Ave(1) = 2)		9.25		Bits
				0.5 MSPS (1 MHz, Ave = 2)		9.65		
				1.0 MSPS (5 MHz, Ave = 4)		10.00		
				0.625 MSPS (2.5 MHz, Ave = 4)		10.00		
				0.25 MSPS (1 MHz, Ave = 4)		10.15		

Parameter		Conditions			Min	Typ	Max	Unit
		Ambient temperature = 25 °C	Differential	1.25 MSPS (2.5 MHz, Ave = 2)		10.25		
				0.5 MSPS (1 MHz, Ave = 2)		10.50		
				1.0 MSPS (5 MHz, Ave = 4)		11.00		
				0.625 MSPS (2.5 MHz, Ave = 4)		11.00		
				0.25 MSPS (1 MHz, Ave = 4)		11.25		
SNR	Signal-to-noise ratio		Single-ended	1.25 MSPS (2.5 MHz, Ave = 2)		58.8		dB
			Differential			64.8		
T_{HD}	Total harmonic distortion		Single-ended	1.25 MSPS (2.5 MHz, Ave = 2)		-63.3		dB
			Differential			-68.8		
I_{DDA}	Current consumption		f_s = 5 MHz			0.50	0.80	mA
			f_s = 2.5 MHz			0.30	0.47	

1. Ave: Averaging factor

Table 5-19 presents the ADC24 electrical characteristics.

Table 5-19 ADC24 Electrical Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V provided by on-die DC-DC with external 3.3 V supply			24		Bits
f_s	Sampling rate			1		16	kSPS
E_G	Gain error				1.5		% of FSR
E_O	Offset error				50		µV
T_{HD}	Total harmonic distortion	Internal ADC voltage reference = 1.8 V	1 kSPS		-80		dB
			16 kSPS		-74		
SNR	Signal to noise ratio	Differential mode, PGA off Ambient temperature = 25 °C	1 kSPS		106		dB
			16 kSPS		93.5		
I_{DDA}	Current consumption				0.45	1.0	mA

5.6.2 DAC12 Characteristics

Table 5-20 presents the DAC12 electrical characteristics.

Table 5-20 DAC12 Electrical Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V provided by on-die DC-DC with external 3.3 V supply			12		Bits
f_c	Conversion rate					1.0	kHz
I_{OUT}	Output drive current		High-performance mode			1.5	mA
E_G	Gain error		High-performance mode		1.5		% of FSR
			Low-power mode		1.5		
E_{Off}	Offset error	Internal ADC voltage reference = 1.8 V	High-performance mode		0.14		% of FSR
			Low-power mode		0.01		
I_{DDA}	Current consumption	Ambient temperature = 25 °C	High-performance mode		2.0		mA
			Low-power mode		150		µA

Parameter		Conditions		Min	Typ	Max	Unit
INL	Integral nonlinearity		High-performance mode	-2		3.2	LSB
			Low-power mode	-1.5		2.6	
DNL	Differential nonlinearity		High-performance mode	-2.2		1.5	LSB
			Low-power mode	-1.1		1.8	

5.6.3 CMP Characteristics

Table 5-21 presents the high-speed comparator electrical characteristics.

Table 5-21 CMP Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{IN}	Comparator input voltage range		-0.3		VDD(1) + 0.3	V
V_{OFFSET_IN}	Input offset	Full common mode range			20	mV
I_{CC}	Current consumption	High-speed mode			200	µA
V_{HYS}	Hysteresis	0.7 V ≤ Vin ≤ VDD(1) - 0.7 V	5		30	mV
I_{bias}	Comparator input bias current				10	nA
t_{RES}	Response time	High-speed mode			5	ns

1. Power supply from LDO-5. For more information on configuration, refer to the CMP_COMP_REG2[ANA_PERIPH_LDO_CONT] register field in the corresponding series-specific Hardware Reference Manual.

5.6.4 LPCMP Characteristics

Table 5-22 presents the low power comparator electrical characteristics.

Table 5-22 LPCMP Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage (from VDD_IO_1V8)		1.62	1.8	1.98	V
V_{IN}	Comparator input voltage range		-0.3		V_{DDA} + 0.3	V
V_{OFFSET_IN}	Input offset	Full common mode range			20	mV
I_{CC}	Current consumption	Low power mode			20	µA
V_{HYS}	Hysteresis	0.7 V ≤ Vin ≤ V_{DDA}–0.7 V	5		30	mV
I_{bias}	Comparator input bias current				10	nA
t_{RES}	Response time	Low power mode			10	µs

5.7 Timing Characteristics

5.7.1 Timing Test Conditions

Table 5-23 shows general description of used symbols, adopted standards, terminology, and test process. Unless otherwise specified, all timing parameters are characterized assuming load capacitance of 10 pF.

Table 5-23 Timing Test Conditions

Parameter	Description
f_{op}	Operating frequency
t_c	Cycle time (period)
t_d	Delay time
t_{dsbl}	Disable time
t_{en}	Enable time
t_h	Hold time
t_s	Setup time
t_{tr}	Transition time
t_v	Valid time
t_{pd}	Pulse duration
t_F	Fall time
t_R	Rise time
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{REF}	Reference voltage
t_{RES}	Timer resolution time
RES	Timer resolution
$t_{P\_COUNTER}$	Counter clock period
t_{MAX_COUNT}	Maximum possible count
$f_{(baud)}$	Maximum programmable baud rate
$t_{(BUF)}$	Bus free time
start	Start bit
C_b	Capacitive load
Dc	Duty cycle
JIT	Jitter
t_{CAS}	Clock after START condition
t_{CBT}	Clock before STOP condition
t_{CASr}	Clock after repeated START
t_{CBSr}	Clock before repeated START
$t_{MMovrLAP}$	Current master to secondary master overlap time during hand off
t_{MMLOCK}	Time internal where new master not driving SDA low
t_{BAC}	Bus available condition
T_{BIC}	Bus idle condition

5.7.2 Timers and Counters

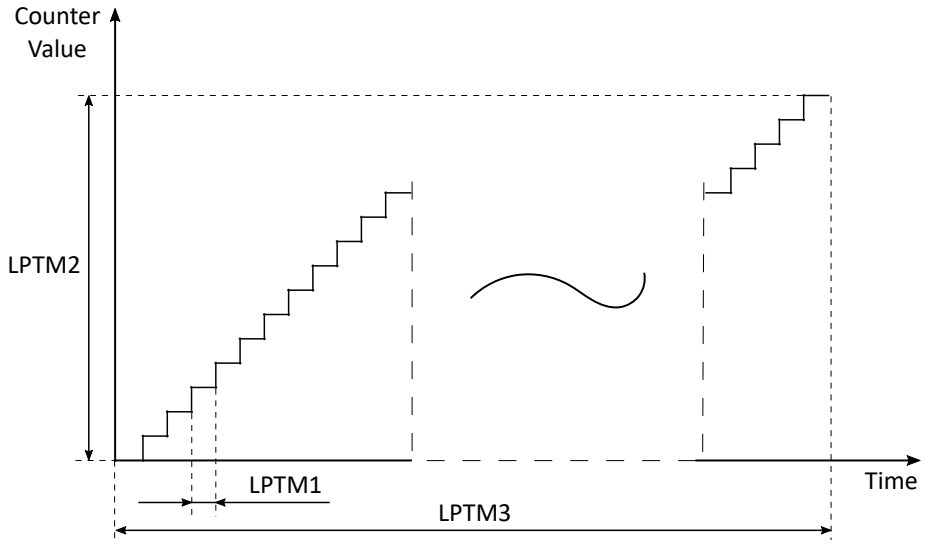
5.7.2.1 LPTIMER Timing Characteristics

Table 5-24 and Figure 5-2 present the LPTIMER timing characteristics.

Table 5-24 LPTIMER Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
Condition: f_{LPTIM_CLK} = 128 kHz (see Table 5-12 Internal LFRC Clock Source Characteristics)						
LPTM1	t_{RES}	Timer resolution time		7.8		µs
LPTM2	$t_{P\_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
LPTM3	t_{MAX_COUNT}	Maximum possible count per timer			32000	s
Condition: f_{LPTIM_CLK} = 32.768 kHz (see Table 5-10 External LFXO Clock Source Characteristics)						
LPTM1	t_{RES}	Timer resolution time		30.5		µs
LPTM2	$t_{P\_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
LPTM3	t_{MAX_COUNT}	Maximum possible count per timer			120000	s

Figure 5-2 LPTIMER Timing Diagram



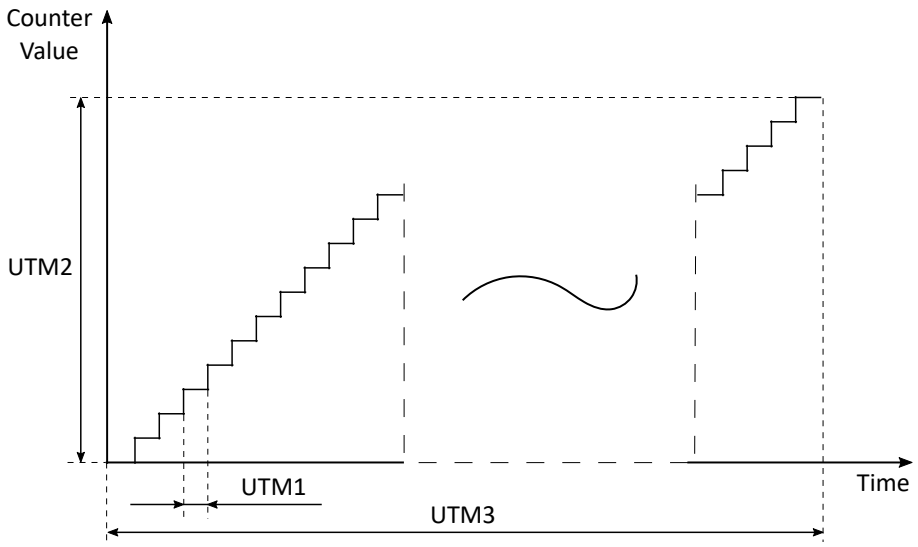
5.7.2.2 UTIMER Timing Characteristics

Table 5-25 and Figure 5-3 present the UTIMER timing characteristics.

Table 5-25 UTIMER Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
Condition: f_{UTIM_CLK} = 400 MHz						
UTM1	t_{RES}	Timer resolution time		2.5		ns
UTM2	$t_{P\_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
UTM3	t_{PERIOD}	Timer period	5×10^{-9}		10.74	s

Figure 5-3 UTIMER Timing Diagram



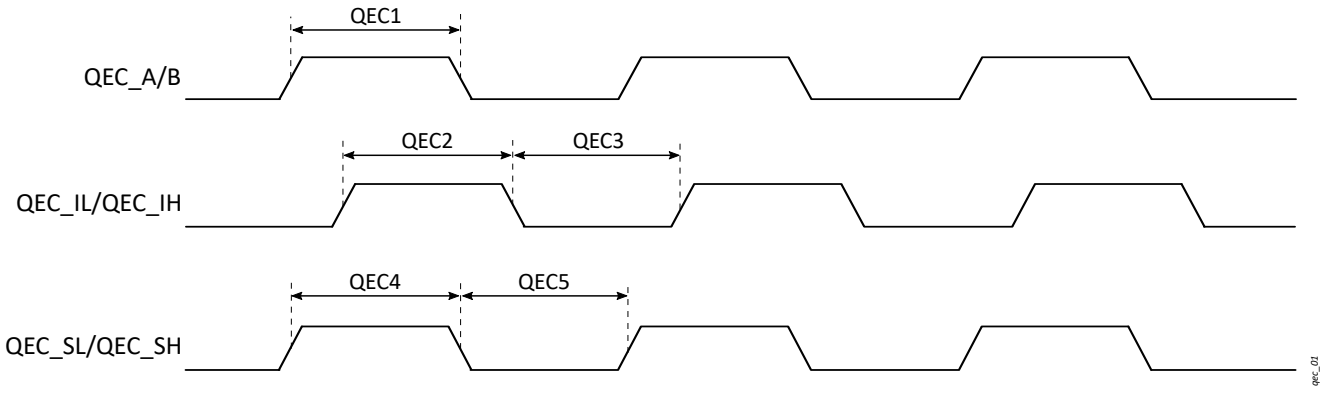
5.7.2.3 QEC Timing Characteristics

Table 5-26 and Figure 5-4 present the QEC timing characteristics.

Table 5-26 QEC Timing Characteristics

No	Parameter		Min	Max	Unit
QEC1	$t_{pd\_QEC\_in}$	Pulse duration, QEC input	10		ns
QEC2	t_{pd_QEC-IH}	Pulse duration, QEC index input high	10		ns
QEC3	t_{pd_QEC-IL}	Pulse duration, QEC index input low	10		ns
QEC4	t_{pd_QEC-SH}	Pulse duration, QEC strobe high	10		ns
QEC5	t_{pd_QEC-SL}	Pulse duration, QEC strobe low	10		ns
QEC6	$t_{d\_QEC-CNTR}$	Delay time, external clock to counter increment		10	ns

Figure 5-4 QEC Timing Diagram



5.7.3 Communication Peripherals

5.7.3.1 CANFD Timing Characteristics

Table 5-27 presents the CANFD timing characteristics.

Table 5-27 CANFD Timing Characteristics

No	Parameter		Min	Max	Unit
CAN1	$f_{(baud)}$	Maximum programmable baud rate		10	Mbps
CAN2	$t_{d\_shift\_TX}$	Delay time, transmit shift register to Tx pin		10	ns
CAN3	$t_{d\_RX\_shift}$	Delay time, Rx pin to receive shift register		30	ns

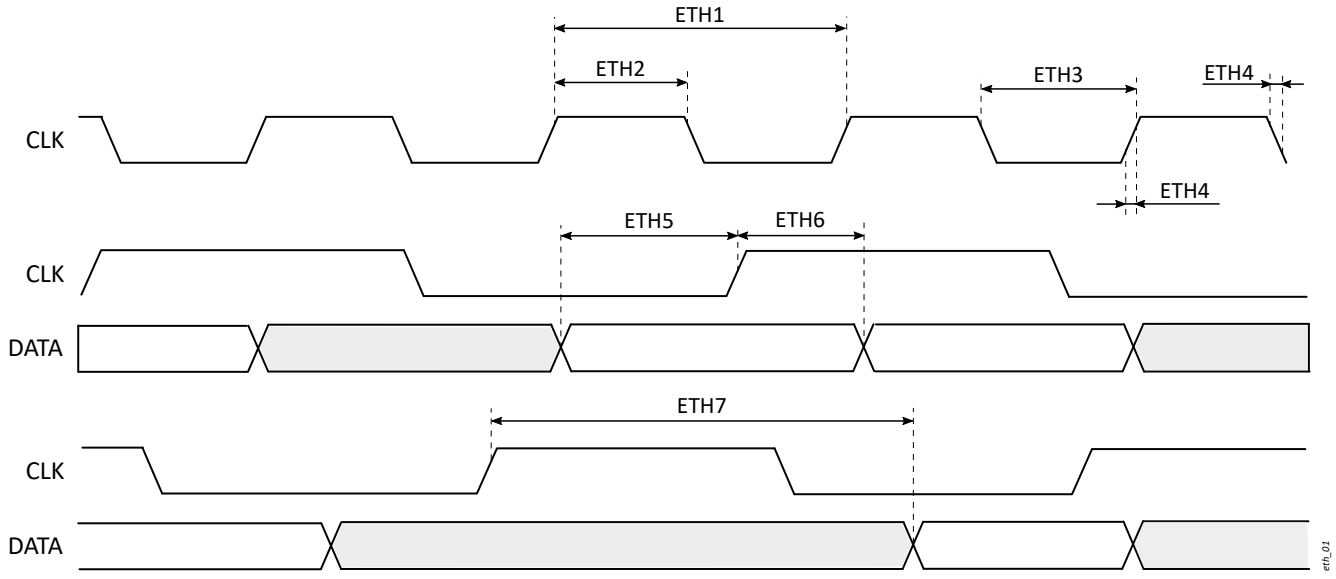
5.7.3.2 ETH Timing Characteristics

Table 5-28 and Figure 5-5 present the ETH RMII timing characteristics

Table 5-28 ETH RMII Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
ETH1	t_{c_CLK}	Cycle time, CLK		20		ns
ETH2	t_{pd_CLK-H}	Pulse duration, CLK high	9	10	11	ns
ETH3	t_{pd_CLK-L}	Pulse duration, CLK low	9	10	11	ns
ETH4	t_{tr_CLK}	Transition time, CLK			1	ns
ETH5	$t_{s\_DATA\_CLK-H}$	Setup time, DATA valid before CLK high	4			ns
ETH6	$t_{h\_DATA\_CLK-H}$	Hold time, DATA valid after CLK high	2			ns
ETH7	$t_{d\_CLK-L\_DATA}$	Delay time, CLK low to DATA valid	7	10	13	ns

Figure 5-5 ETH Timing Diagram



5.7.3.3 I2C Timing Characteristics

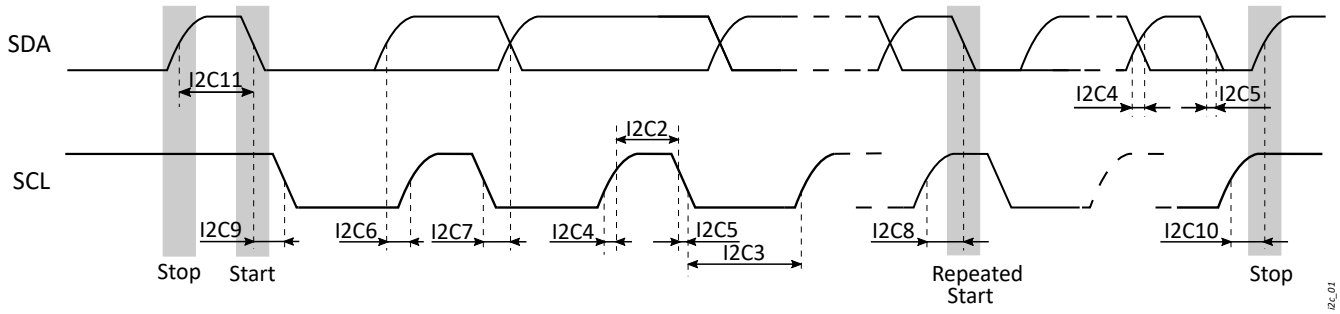
Table 5-29 and Figure 5-6 present the I2C timing characteristics.

Table 5-29 I2C Timing Characteristics

No	Parameter		SS[2]		FS[2]		FM+[3]		HS[3]		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
	t_{c_SCL}	Cycle time	10		2.5		1				µs
I2C2	t_{pd_SCL-H}	Pulse duration, SCL high		0.450		1.320		0.500			µs
I2C3	t_{pd_SCL-L}	Pulse duration, SCL low		0.450		1.320		0.500			µs
I2C4	$t_{R\_SDA\_SCL}$	Rise time of SDA and SCL signals	20	300	20	300	20	120			ns
I2C5	$t_{F\_SDA\_SCL}$	Fall time of SDA and SCL signals	See table note(1)	300	See table note(1)	300	See table note(1)	120			ns
I2C6	$t_{s\_SDA\_SCL}$	Setup time, SDA to SCL		0.1		0.1		0.1			µs
I2C7	$t_{h\_SDA\_SCL}$	Hold time, SDA to SCL									µs
I2C8	$t_{s\_SCL\_start}$	Setup time, SCL to repeated START condition		0.6		0.26		0.26			µs
I2C9	$t_{h\_start\_SCL}$	Hold time, START condition to SCL		0.6		0.26		0.26			µs
I2C10	$t_{h\_SCL\_stop}$	Setup time, SCL to STOP condition		0.6		0.26		0.26			µs
I2C11	$t_{BUF\_start\_stop}$	Bus free time between STOP and START condition		1.3		0.5		0.5			µs
	C_{b_bus}	Capacitive load for each bus line		50		50		50		100	pF

1. 20 × (VDD_IO_1V8 ÷ 5.5 V)
2. Supported by I2C and LPI2C modules
3. Supported only by I2C modules

Figure 5-6 I2C Timing Diagram



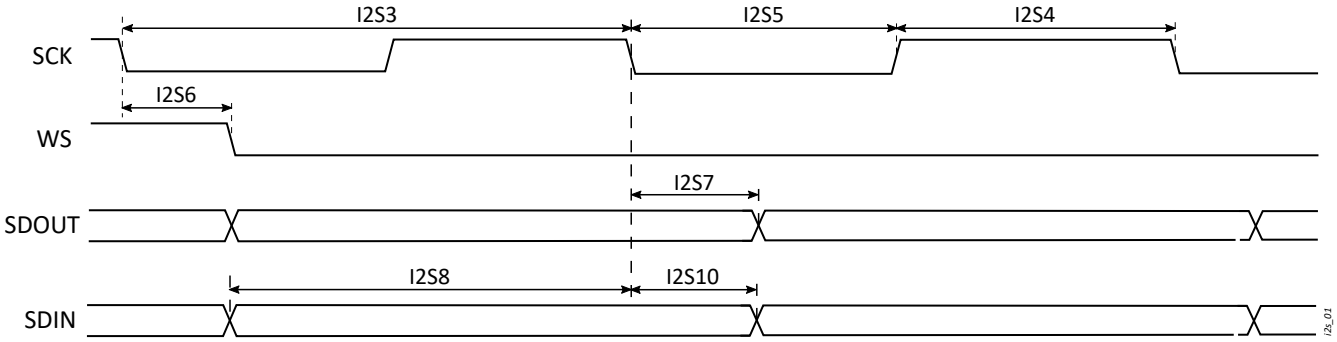
5.7.3.4 I2S Timing Characteristics

Table 5-30 and Figure 5-7 present the I2S timing characteristics.

Table 5-30 I2S Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
	f_{op_SCK}	Operation frequency, SCK (serial clock)	2.27	2.5	2.78	MHz
I2S3	t_{c_SCK}	Cycle time, SCK (serial clock)	440	400	360	ns
I2S4	t_{pd_SCK-H}	Pulse duration, SCK high	160			ns
I2S5	t_{pd_SCK-L}	Pulse duration, SCK low	160			ns
I2S6	$t_{d\_SCK\_WS}$	Delay time, SCK output low to WS valid			$0.8 \times t_{c\_SCK}$	ns
I2S7	$t_{d\_SCK\_SDOUT}$	Delay time, SCK output low to SDOUT valid			$0.8 \times t_{c\_SCK}$	ns
I2S8	$t_{s\_SDIN\_master}$	Setup time, SDIN master mode	60			ns
I2S9	$t_{s\_SDIN\_slave}$	Setup time, SDIN slave mode	60			ns
I2S10	$t_{h\_SDIN\_master}$	Hold time, SDIN master mode	100			ns
I2S11	$t_{h\_SDIN\_slave}$	Hold time, SDIN slave mode	0			ns

Figure 5-7 I2S Master Mode Timing Diagram



5.7.3.5 I3C Timing Characteristics

Table 5-31, Table 5-32, Figure 5-8, and Figure 5-9 present the I3C timing characteristics.

Table 5-31 I3C Open Drain Timing Characteristics

No	Parameter		Mode	Min	Max	Unit
I3C1	t_{pd_SCL-L}	Pulse duration, SCL low	Master	200		ns
I3C2	t_{pd_SCL-H}	Pulse duration, SCL high	Master	200		ns
I3C3	t_{F_SDA}	Fall time, SDA	Master		11	ns
I3C4	t_{s_SDA-OD}	Setup time, SDA open drain	Master	3		ns
I3C5	t_{CAS}	Clock after START condition	Master	38.4		ns
I3C6	t_{CBT}	Clock before STOP condition	Master	19.2		ns
I3C7	$t_{MMovrLAP}$	Current master to secondary master overlap time during hand off	Master	212		ns
I3C8	t_{BAC}	Bus available condition	Master	1000		ns
I3C9	T_{BIC}	Bus idle condition	Master	200000		ns
I3C10	t_{MMLOCK}	Time internal where new master not driving SDA Low	Master	1000		ns

Table 5-32 I3C Push-Pull Timing Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
I3C1	t_c	Cycle time, SCL	Master	100000	77.52	ns

NO.	PARAMETER		MODE	MIN	MAX	UNIT
I3C2	t_{pd_SCL-L}	Pulse duration, SCL low	Master	32		ns
I3C4	t_{pd_SCL-H}	Pulse duration, SCL high	Master	32		ns
I3C5	$t_{d\_SCL\_SDA}$	Delay time, SCL to SDA out	Master		12	ns
I3C6	t_{R_SCL}	Rise time, SCL	Master		12	ns
I3C7	t_{F_SCL}	Fall time, SCL	Master		12	ns
I3C8	th_SDA	Hold time, SDA	Master in push-pull	15		ns
I3C9	ts_SDA	Setup time, SDA	Master in push-pull	15		ns
I3C10	t_{CASr}	Clock after repeated START	Master	19.2		ns
I3C11	t_{CBSr}	Clock before repeated START	Master	19.2		ns
	C_b	Capacitive load per bus line (SDA/SCL)	Master, Slave	50		pf

Figure 5-8 I3C Open Drain Timing Diagram

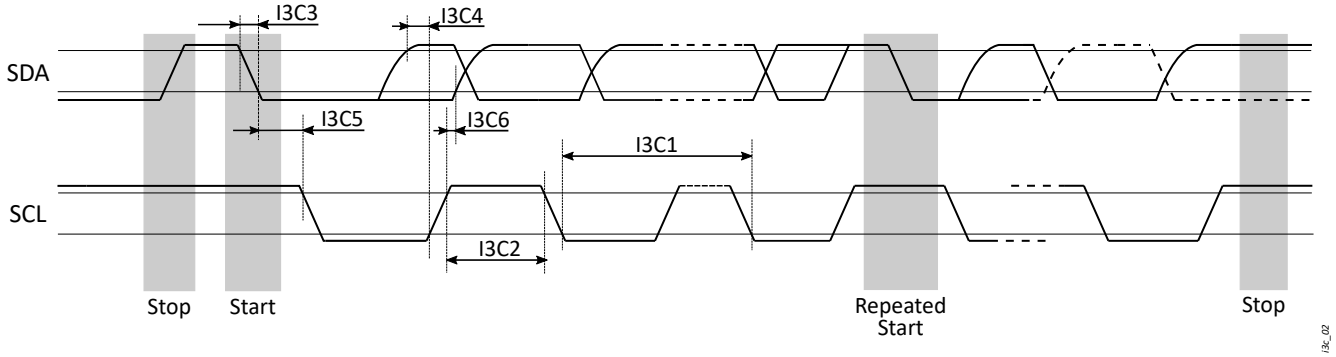
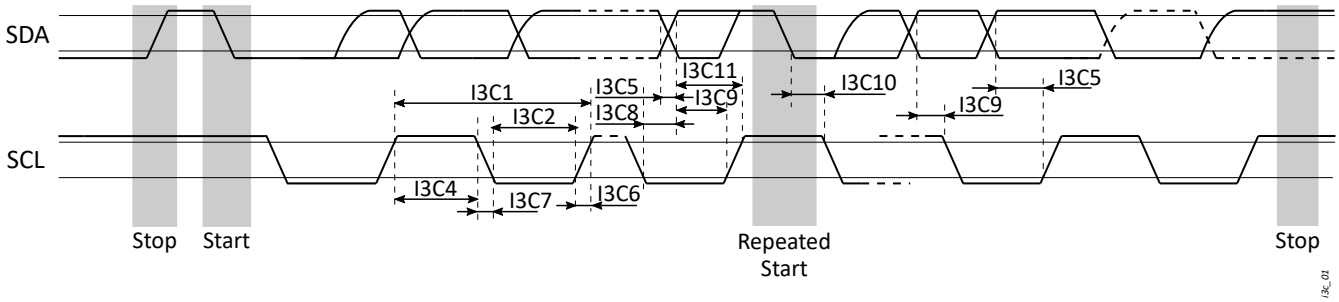


Figure 5-9 I3C Push-Pull Timing Diagram



5.7.3.6 PDM Timing Characteristics

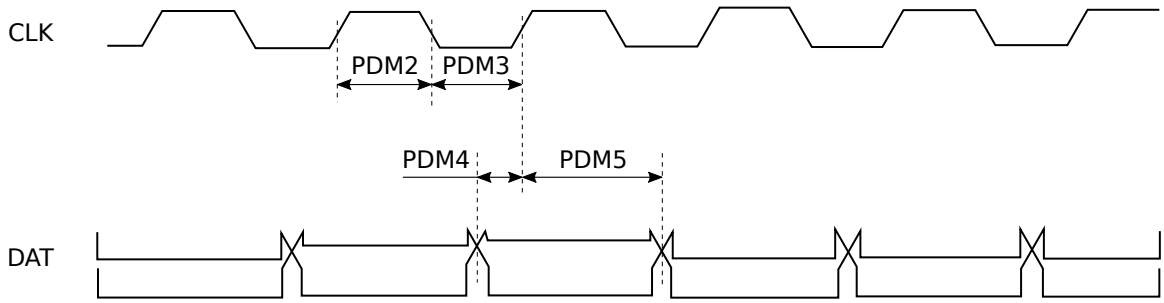
Table 5-33 and Figure 5-10 present the PDM timing characteristics.

Table 5-33 PDM Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
	f_{OP}	Operating frequency, PDM_CLK	0.128		4.8	MHz
PDM2	$t_{W\_CLK\_H}$	Pulse duration, CLK high		48.4		% of total f_{OP} period

No	Parameter		Min	Typ	Max	Unit
PDM3	$t_{W\_CLK\_L}$	Pulse duration, CLK low		48.4		% of total f_{OP} period
PDM4	t_{SU_DAT}	Setup time, DAT	65			ns
PDM5	t_{H_DAT}	Hold time, DAT	0			ns

Figure 5-10 PDM Timing Diagram



5.7.3.7 SPI Timing Characteristics

Table 5-34, Figure 5-11, and Figure 5-12 present the SPI timing characteristics.

Table 5-34 SPI Timing Characteristics

No	Parameter			Min	Typ	Max	Unit
SP1	t_{c_SCLK}	Cycle time, SCLK	SPI	20			ns
			LPSPI	40			ns
SP2	t_{R_SCLK}	Rise time, SCLK				3	ns
SP3	t_{F_SCLK}	Fall time, SCLK				3	ns
SP4	t_{pd_CLK-L}	Pulse duration, SCLK low		$0.45 \times t_{c\_SCKL}$			ns
SP5	t_{pd_CLK-H}	Pulse duration, SCLK high		$0.45 \times t_{c\_SCKL}$			ns
SP6	t_{s_SS}	Setup time, SS				3	ns
SP7	t_{h_SS}	Hold time, SS		0.5	0.6	0.8	ns
SP8	$t_{s\_MISO\_SCLK}$	Setup time, MISO to SCLK		3			ns
SP9	$t_{h\_MISO\_SCLK}$	Hold time, MISO to SCLK		3			ns
SP10	$t_{d\_MOSI\_SS}$	Delay time, MOSI to SS		3			ns
SP11	$t_{d\_MOSI\_SCLK}$	Delay time, MOSI to SCLK		3			ns

Figure 5-11 SPI Receive Timing Diagram

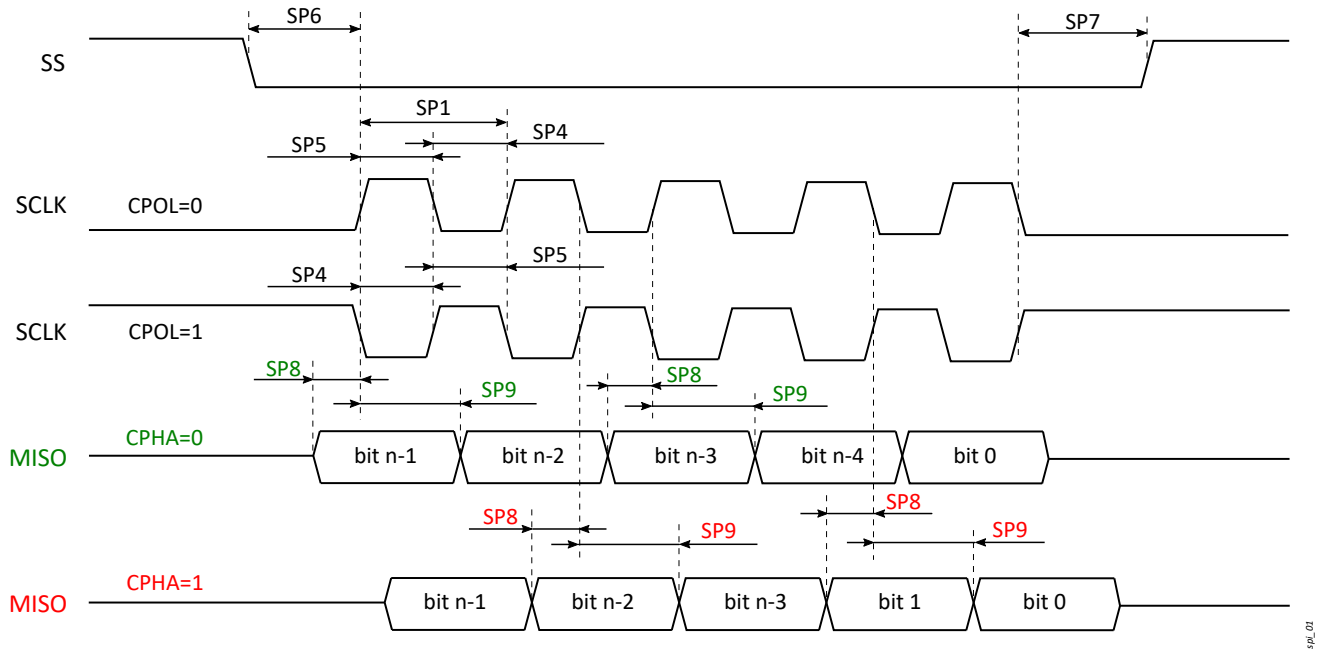
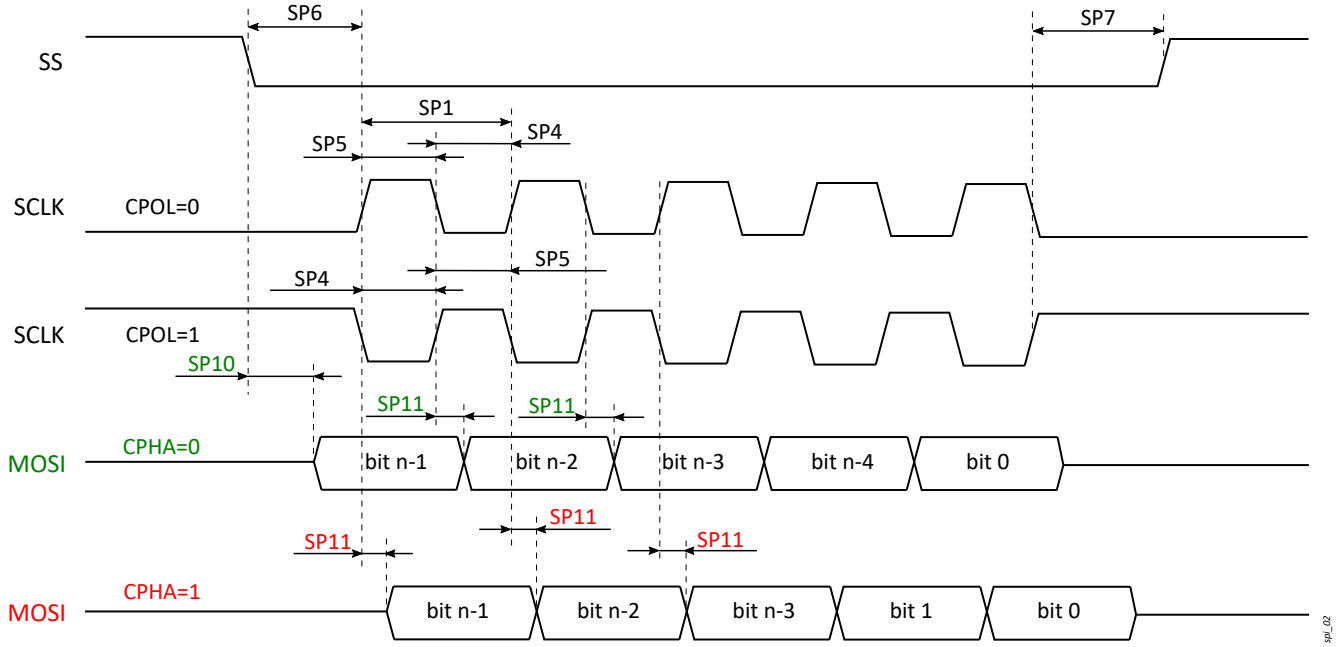


Figure 5-12 SPI Transmit Timing Diagram



5.7.3.8 UART Timing Characteristics

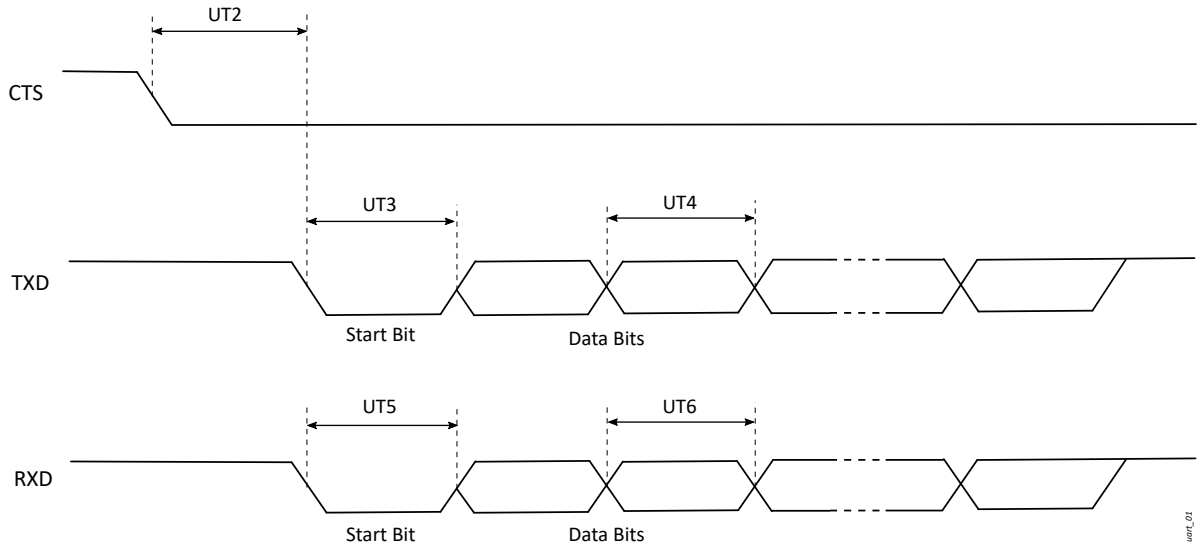
Table 5-35 and Figure 5-13 present the UART timing characteristics.

Table 5-35 UART Timing Characteristics

No	Parameter		Mode	Min	Max	Unit
	$f_{(baud)}$	Maximum programmable baud rate			2.5	Mbps
UT2	$t_{d\_CTS\_ST\_TX}$	Delay time, receive CTSn low to start bit low		100	200	ns
UT3	$t_{pd\_ST\_TX}$	Pulse duration, transmit start bit, low		400	400	ns

No	Parameter		Mode	Min	Max	Unit
UT4	$t_{pd\_DAT\_TX}$	Pulse duration, transmit data bit, high or low		400	400	ns
UT5	$t_{pd\_ST\_RX}$	Pulse duration, receive start bit, low		400	400	ns
UT6	$t_{pd\_DAT\_RX}$	Pulse duration, receive data bit, high or low		400	400	ns

Figure 5-13 UART Timing Diagram



5.7.3.9 USB Timing Characteristics

The USB interface timing characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

5.7.4 External Memory Interfaces

5.7.4.1 OSPI Timing Characteristics

Table 5-36, Figure 5-14, Figure 5-15, and Figure 5-16 present the OSPI timing characteristics.

Table 5-36 OSPI Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
OSPI Common Parameters						
	f_{op}	Operating frequency	80	100 (1)	120	MHz
O2	t_{c_CLK}	Cycle time, CLK	12.5	10	8.33	ns
O3	t_{pd_CLK-H}	Pulse duration, CLK high	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	ns
O4	t_{pd_CLK-L}	Pulse duration, CLK low	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	ns
O5	t_{R_CLK}	Rise time, CLK			0.05 × t_{c_CKL}	ns
O6	t_{F_CLK}	Fall time, CLK			0.05 × t_{c_CKL}	ns
O7	$t_{s\_DATA\_IN}$	Setup time, DATA input	3			ns
O8	$t_{h\_DATA\_IN}$	Hold time, DATA input	0.8	0.6	0.5	ns
O9	$t_{d\_DATA\_OUT}$	Delay time, DATA output	2.375	1.8	1.45	ns
O10	$t_{h\_DATA\_OUT}$	Hold time, DATA output	0			ns
OSPI0 Specific Parameters (@ f_{op} = 100 MHz)						

No	Parameter			Min	Typ	Max	Unit
O11	t_{RXD_DLY} (2)	DATA input delay (compared to RXDS line)	Pin set A	N/A	N/A	N/A	-
			Pin set B	1.5	4.0	5.2	ns
			Pin set C	1.6	2.6	4.0	ns
O12	t_{RXDS_DLY} (2)	Programmable RXDS line delay to compensate for t_{RXD_DLY}		$t_{RXD\_DLY\_min}$ + 0.25 × 1/f_{op}	$t_{RXD\_DLY\_typ}$ + 0.25 × 1/f_{op}	$t_{RXD\_DLY\_max}$ + 0.25 × 1/f_{op}	ns
OSPI1 Specific Parameters (@ f_{op} = 100 MHz)							
O11	t_{RXD_DLY} (2)	DATA input delay (compared to RXDS line)	Pin set A	0.3	1.2	3.7	ns
			Pin set B	1.1	1.9	2.3	ns
			Pin set C	1.4	2.2	3.5	ns
O12	t_{RXDS_DLY} (2)	Programmable RXDS line delay to compensate for t_{RXD_DLY}		$t_{RXD\_DLY\_min}$ + 0.25 × 1/f_{op}	$t_{RXD\_DLY\_typ}$ + 0.25 × 1/f_{op}	$t_{RXD\_DLY\_max}$ + 0.25 × 1/f_{op}	ns

1. Some pin multiplex options will reduce the operating frequency. Please see Cautionary information at the start of Section 4.2 Pin Function Options by Location.
2. The OSPI data input lines are being delayed inside the device compared to the RXDS data strobe line. A programmable delay should be added to the RXDS line itself to overcome the delay of the data input lines. The objective is to ensure that the RXDS line is delayed by ¼ OSPI clock cycle with respect to the leading edge of the valid data lines. For more information on the programming of the RXDS line delay, refer to Section *OSPI Read Data Strobe Signal (OSPI_RXDS)* within Chapter *Cryptographic Octal SPI (OSPI)* of the device series-specific HWRM.

Figure 5-14 OSPI Timing Diagram - SDR Mode

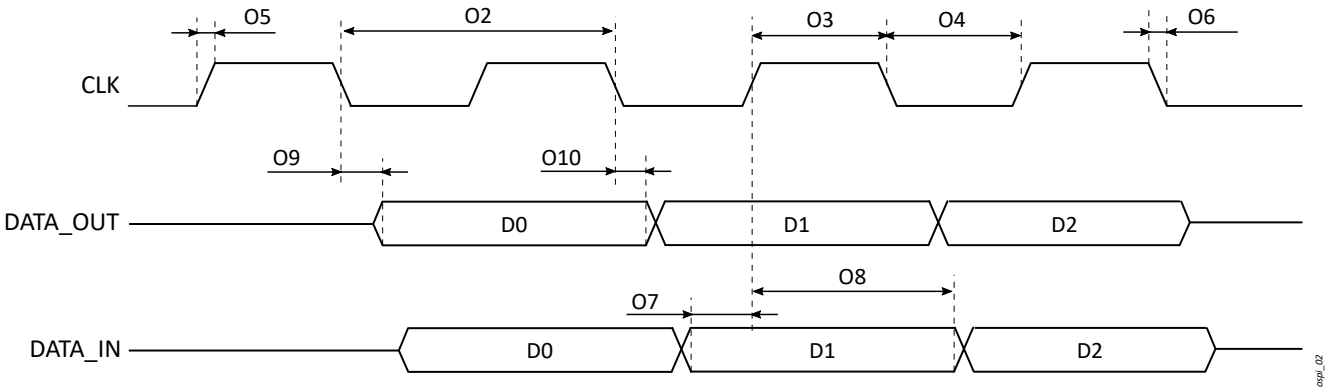


Figure 5-15 OSPI Timing Diagram - DDR Mode (Transmit)

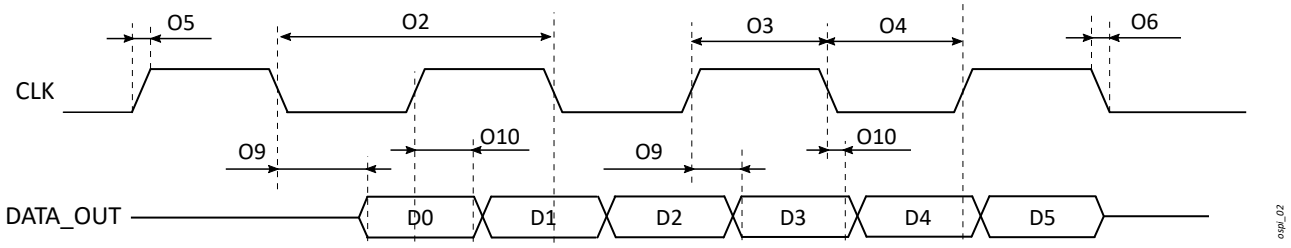
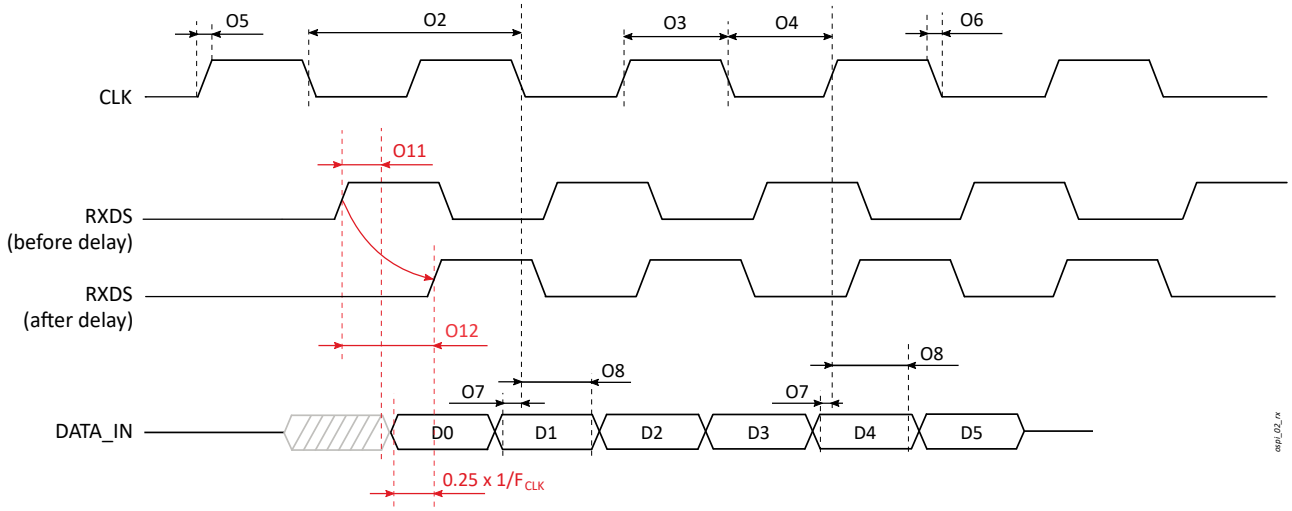


Figure 5-16 OSPI Timing Diagram - DDR Mode (Receive)



O12 (programmable RXDS delay) = O11 + 0.25 x $1/F_{CLK}$

5.7.4.2 SDMMC Timing Characteristics

Table 5-37 and Figure 5-17 present the SDMMC timing characteristics in DS mode.

Table 5-37 SDMMC Timing Characteristics (DS mode)

No	Parameter		Min	Max	Unit
DS1	t_{c_CLK}	Cycle time, CLK		40[(1)]	ns
DS2	t_{R_CLK}	Rise time, CLK		10	ns
DS3	t_{F_CLK}	Fall time, CLK		10	ns
	D_{C_CLK}	Duty cycle	45	55	%
DS5	$t_{s\_CMD\_CLK}$	Setup time, CMD valid before CLK rising edge	11.7		ns
DS6	$t_{h\_CMD\_CLK}$	Hold time, CMD valid after CLK rising edge	8.3		ns
DS7	$t_{s\_DATA\_CLK}$	Setup time, DATA valid before CLK rising edge	11.7		ns
DS8	$t_{h\_DATA\_CLK}$	Hold time, DATA valid after CLK rising edge	8.3		ns

1. Some pin multiplex options will reduce the operating frequency. Please see Cautionary information at the start of Section 4.2 Pin Function Options by Location.

Figure 5-17 SDMMC Timing Diagram (DS mode)

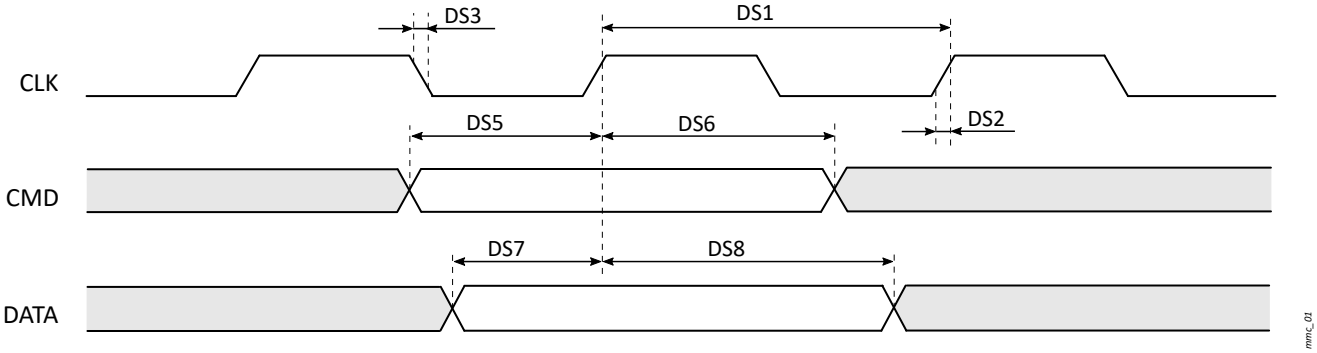


Table 5-38 and Figure 5-18 present the SDMMC timing characteristics in HS mode.

Table 5-38 SDMMC Timing Characteristics (HS mode)

No	Parameter		Min	Max	Unit
HS1	t_{c_CLK}	Cycle time, CLK		20	ns
HS2	t_{R_CLK}	Rise time, CLK		3	ns
HS3	t_{F_CLK}	Fall time, CLK		3	ns
	D_{C_CLK}	Duty cycle	45	55	%
HS5	$t_{s\_CMD\_CLK}$	Setup time, CMD valid before CLK rising edge	6.3		ns
HS6	$t_{h\_CMD\_CLK}$	Hold time, CMD valid after CLK rising edge	2.5		ns
HS7	$t_{s\_DATA\_CLK}$	Setup time, DATA valid before CLK rising edge	6.3		ns
HS8	$t_{h\_DATA\_CLK}$	Hold time, DATA valid after CLK rising edge	2.5		ns

Figure 5-18 SDMMC Timing Diagram (HS mode)

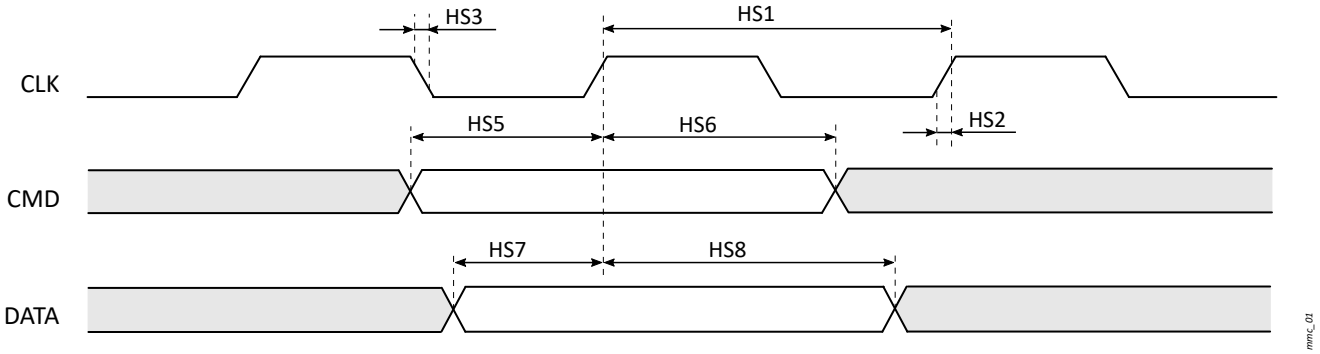
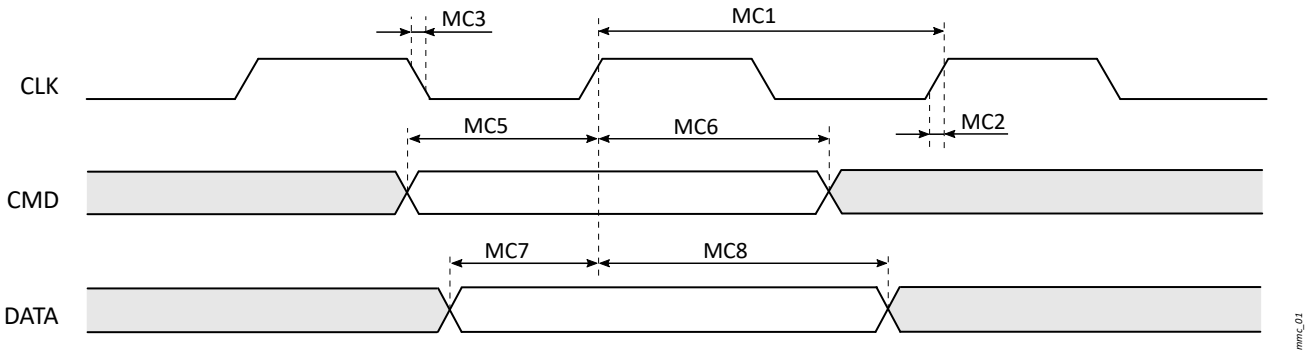


Table 5-39 and Figure 5-19 present the SDMMC timing characteristics in SDR12/SDR25/SDR50 modes.

Table 5-39 SDMMC Timing Characteristics (SDR12/SDR25/SDR50)

No	Parameter		Mode	Min	Max	Unit
MC1	t_{c_CLK}	Cycle time, CLK	SDR12		40	ns
			SDR25		20	ns
			SDR50		10	ns
MC2	t_{R_CLK}	Rise time, CLK			3	ns
MC3	t_{F_CLK}	Fall time, CLK			3	ns
	D_{C_CLK}	Duty cycle		45	55	%
MC5	$t_{s\_CMD\_CLK}$	Setup time, CMD valid before CLK rising edge	SDR12	3		ns
			SDR25	3		ns
			SDR50	3		ns
MC6	$t_{h\_CMD\_CLK}$	Hold time, CMD valid after CLK rising edge	SDR12	0.8		ns
			SDR25	0.8		ns
			SDR50	0.8		ns
MC7	$t_{s\_DATA\_CLK}$	Setup time, DATA valid before CLK rising edge	SDR12	3		ns
			SDR25	3		ns
			SDR50	3		ns
MC8	$t_{h\_DATA\_CLK}$	Hold time, DATA valid after CLK rising edge	SDR12	0.8		ns
			SDR25	0.8		ns
			SDR50	0.8		ns

Figure 5-19 SDMMC Timing Diagram (SDR12/SDR25/SDR50)



5.7.5 Camera Interfaces

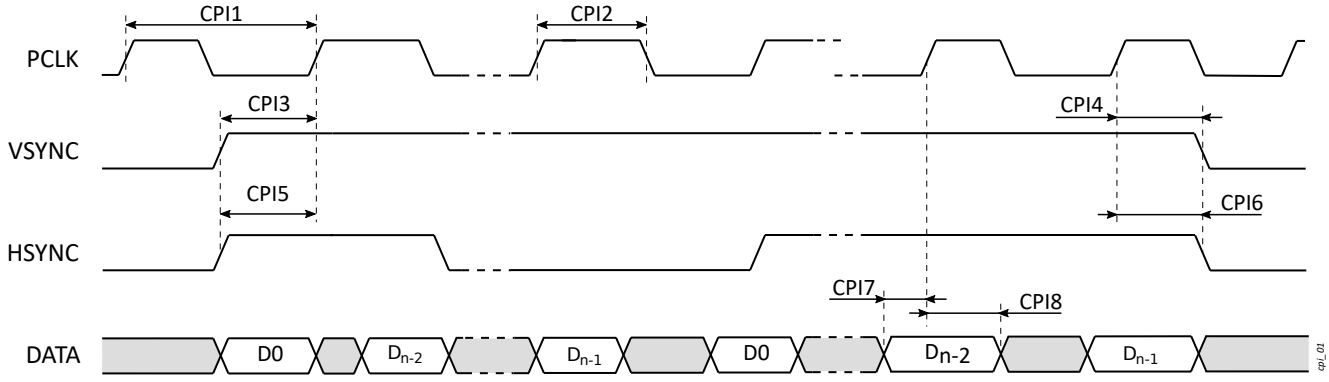
5.7.5.1 CPI Timing Characteristics

Table 5-40 and Figure 5-20 present the CPI timing characteristics.

Table 5-40 CPI Timing Characteristics

No	Parameter		Min	Max	Unit
CPI1	t_{c_MCLK}	Cycle time, PCLK	16.7		ns
CPI2	t_{pd_MCLK}	Pulse duration, PCLK	8.33		ns
CPI3	$t_{s\_VSYNC\_PCLK}$	Setup time, input vertical sync VSYNC valid before PCLK	3		ns
CPI4	$t_{h\_VSYNC\_PCLK}$	Hold time, input vertical sync VSYNC valid after PCLK	3		ns
CPI5	$t_{s\_HSYNC\_PCLK}$	Setup time, input horizontal sync HSYNC valid before PCLK	3		ns
CPI6	$t_{h\_HSYNC\_PCLK}$	Hold time, input horizontal sync HSYNC valid after PCLK	3		ns
CPI7	$t_{s\_DATA\_PCLK}$	Setup time, input DATA valid before PCLK	5		ns
CPI8	$t_{h\_DATA\_PCLK}$	Hold time, input DATA valid after PCLK	5		ns

Figure 5-20 CPI Timing Diagram



5.7.5.2 CSI Timing Characteristics

The CSI interface timing characteristics are compliant with MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.2, and MIPI Alliance Specification for D-PHY, Version 1.2.

5.7.6 Display Interfaces

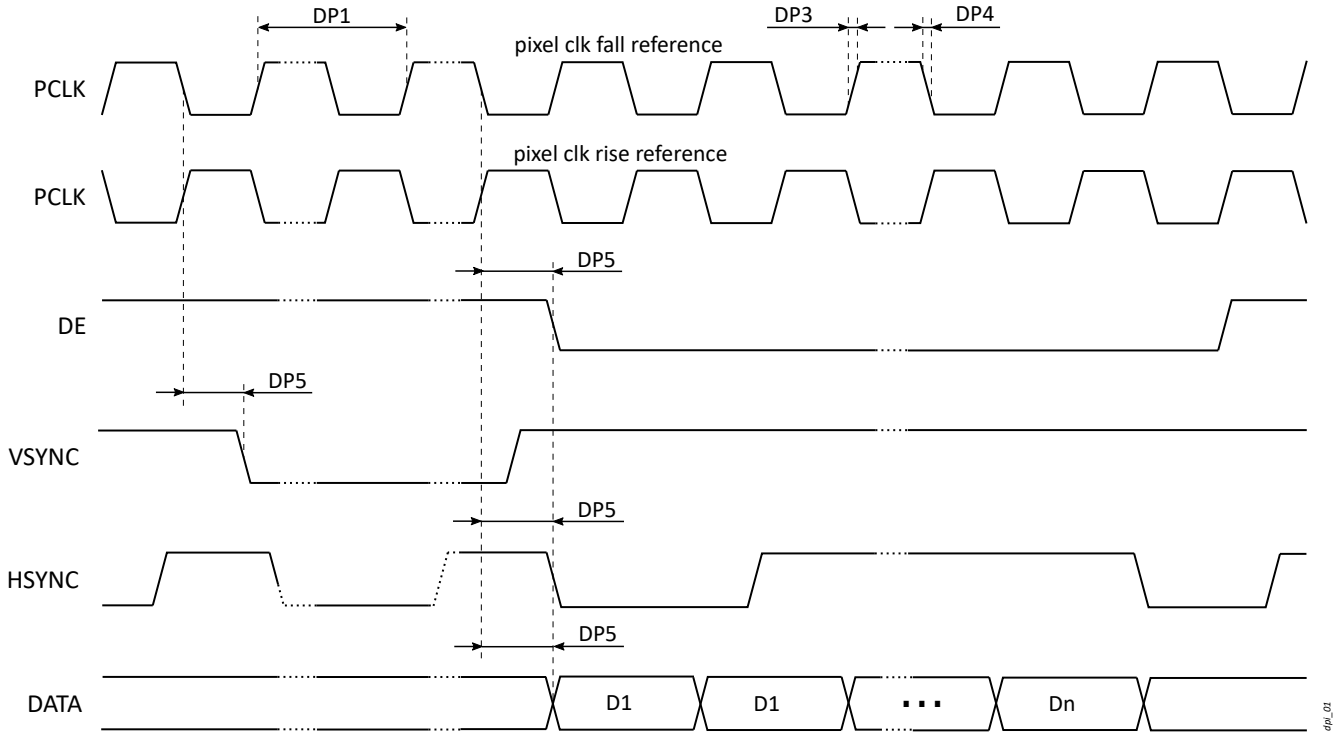
5.7.6.1 DPI Timing Characteristics

Table 5-41 and Figure 5-21 present the DPI timing characteristics.

Table 5-41 DPI Timing Characteristics

No	Parameter		Min	Max	Unit
DP1	t_C	Cycle time	20		ns
	D_{C_CLK}	Duty cycle, PCLK	40	60	%
DP3	t_{R_CLK}	Rise time, PCLK		1	ns
DP4	t_{F_CLK}	Fall time, PCLK		1	ns
DP5	$t_{d\_all\_to\_CLK}$	Delay time, DE, VSYNC, HSYNC, DATA signals to PCLK	5		ns

Figure 5-21 DPI Timing Diagram



5.7.6.2 DSI Timing Characteristics

The DSI interface timing characteristics are compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.2, and MIPI Alliance Specification for D-PHY, Version 1.2.

5.7.7 Debug Interface

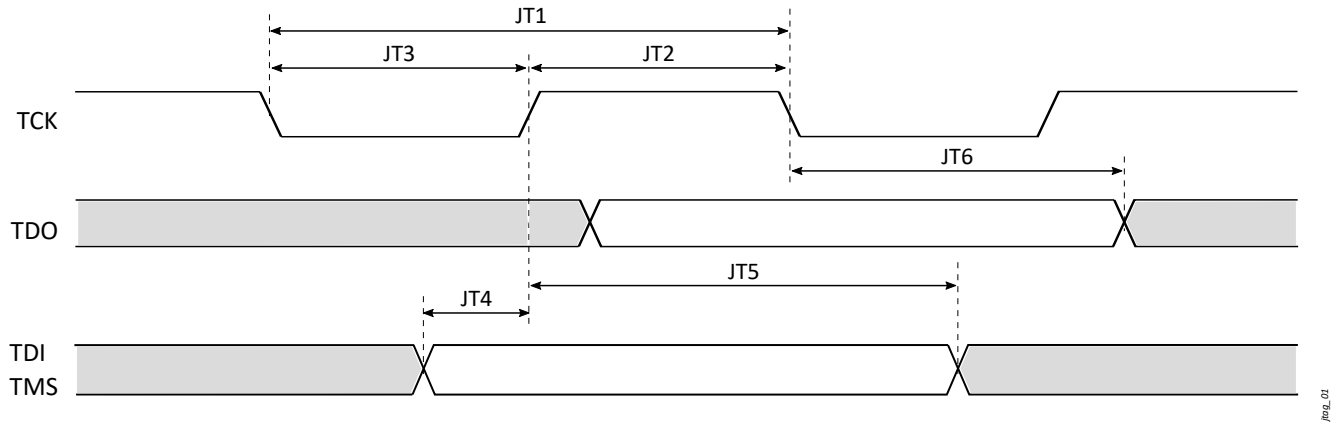
Table 5-42 and Figure 5-22 present the JTAG timing characteristics.

Table 5-42 JTAG Timing Characteristics

No	Parameter		Min	Max	Unit
JT1	t_C	Cycle time, TCK	50	100	ns

No	Parameter		Min	Max	Unit
JT2	t_{pd_TCK-H}	Pulse duration, TCK high	24	49	ns
JT3	t_{pd_TCK-L}	Pulse duration, TCK low	24	49	ns
JT4	$t_{s\_TDI/TMS-TCK}$	Setup time, TDI/TMS valid before TCK rising edge	7	7	ns
JT5	$t_{h\_TDI/TMS-TCK}$	Hold time, TDI/TMS valid after TCK rising edge	7	7	ns
JT6	t_{d_TDO}	Delay time, TDO valid after TCK falling edge	7	7	ns

Figure 5-22 JTAG Timing Diagram



6 Package Information

6.1 Device Marking Definition

Figure 6-1 and Figure 6-2 present the top marking reference view.

Figure 6-1 WLCSP Device Top Marking Reference

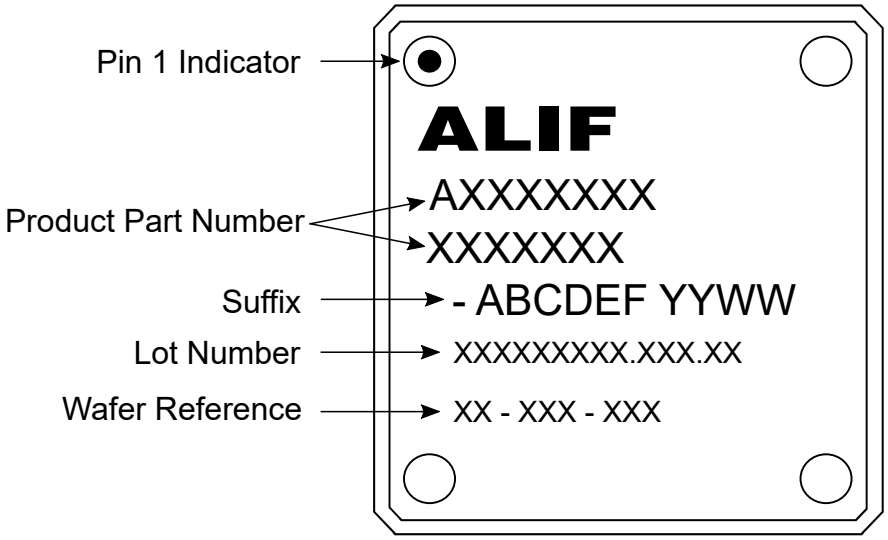


Figure 6-2 FBGA Device Top Marking Reference

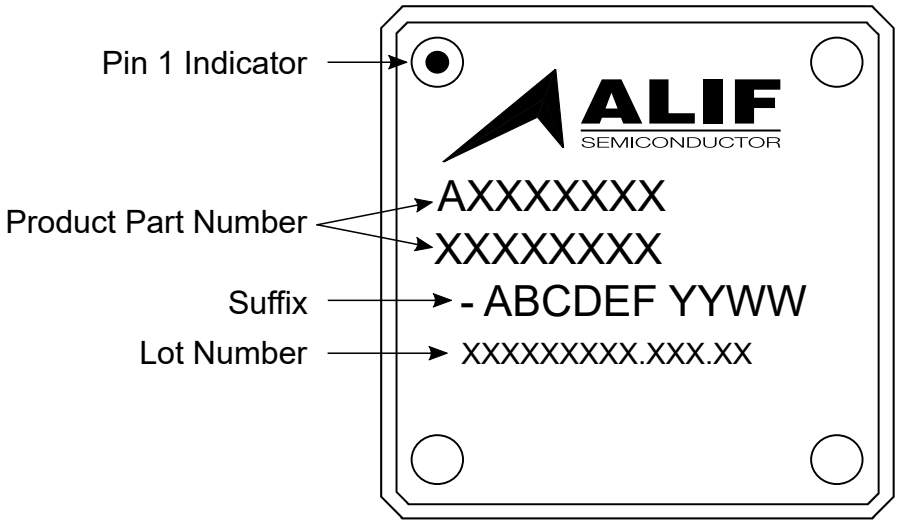


Table 6-1 presents the part number decoding.

Table 6-1 Product Identification

Example Part Number:	A	E	3	0	2	F	8	0	F	55	D5	A	E
Device Manufacturer													
A - Alif Semiconductor													
Device Family													
B - BLE-connected embedded microcontrollers													
E - Ensemble, embedded processors													
Device Series													
0 - Service MCU													
1 - Efficiency MCU													
3 - Performance MCU													
5 - Fusion processor MCU/MPU													
7 - Extreme fusion processor MCU/MPU													
Number of Application Processing Cores													
0 - Zero cores													
1 - One cores													
2 - Two cores													
Number of Real Time Processing Cores													
0 - Zero cores													
1 - One cores													
2 - Two cores													
Security Attribute													
B - Basic security													
F - Full security, complete life cycle management													
Machine Learning and AI Capability													
0 - Hardware Acceleration for AI/ML													
1 - MCU Vector Extension (Helium)													
4 - Single Neural Processing Unit (Ethos-U55) + MCU Vector Extension (Helium)													
8 - Dual Neural Processing Units (Ethos-U55) + MCU Vector Extension (Helium)													
9 - Dual Neural Processing Units (Ethos-U55 and Ethos-U85) + MCU Vector Extension (Helium)													
A - Triple Neural Processing Units (2× Ethos-U55 and Ethos-U85) + MCU Vector Extension (Helium)													
Wireless Capability													
0 - No wireless													
M - BLE + IEEE 802.15.4													
Peripheral Set													
0 through 9, A through Z = Level of peripheral selection mix, higher is typically more peripherals													
On-Chip Application MRAM Size													
MRAM memory size in MB													
1st digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB													
2nd digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB													
On-Chip Application SRAM Size													
SRAM memory size in MB													
1st digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB													

Example Part Number:	A	E	3	0	2	F	8	0	F	55	D5	A	E
2nd digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB													
Package Type and Pin Count													
A - WLCSP208, 0.5 mm pitch													
B - WLCSP212, 0.4 mm pitch													
H - WLCSP90, 0.4 mm pitch													
L - FBGA194, 0.5 mm pitch													
P - FBGA120, 0.5 mm pitch													
5 - TQFP64, 0.5 mm pitch													
Operating Temperature													
S - Standard (see Section 5.2.1 General Operating Conditions)													
E - Extended (see Section 5.2.1 General Operating Conditions)													
H - Industrial (see Section 5.2.1 General Operating Conditions)													

Table 6-2 presents the Suffix (characters after main part number) decoding.

Table 6-2 Suffix Definition

Position	Description
A	ID
B	ID revision
C	Firmware version
D	Fab site. D = Dresden
E	Final assembly site. M = Malaysia, K = South Korea
F	Final test site. S = Singapore, E = USA
Space	
Y	Calendar year of device production
Y	
W	Work week of device production
W	

6.2 Package Specifications

6.2.1 WLCSP208 Package Information

6.2.1.1 WLCSP208 Thermal Operating Specifications

Table 6-3 provides thermal operating specifications for WLCSP208 package.

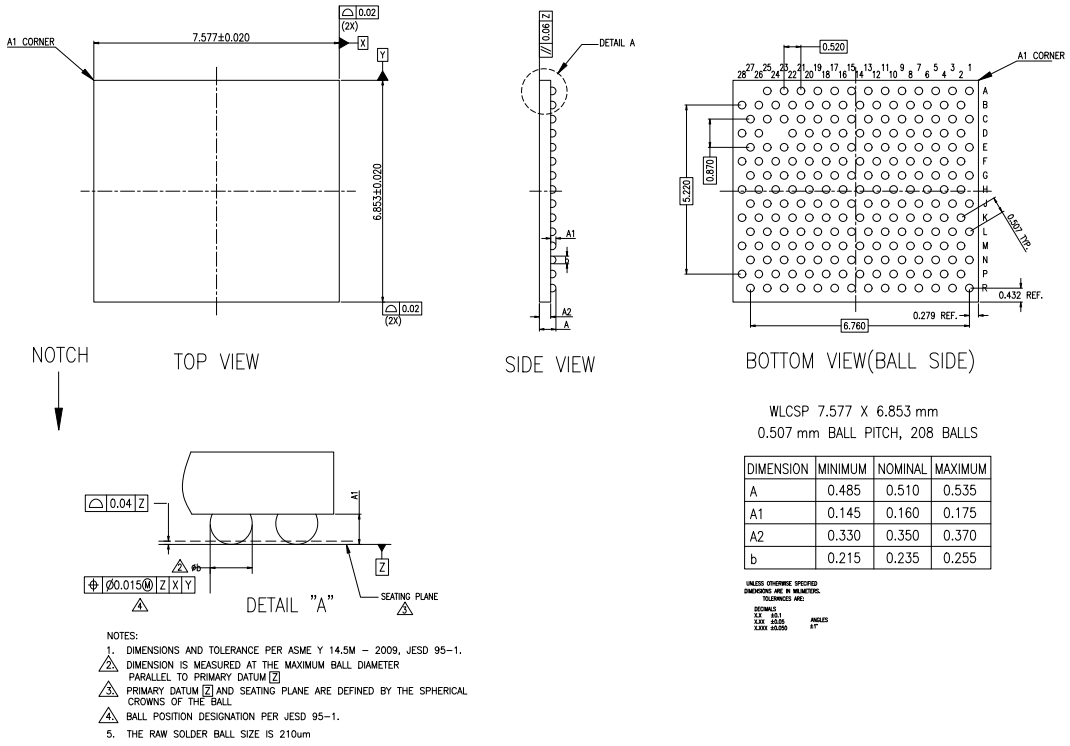
Table 6-3 WLCSP208 Thermal Operating Specifications

Parameter		Value	Unit
$R\theta_{JA}$	Thermal resistance in natural convection (junction-to-free air)	19.5	°C/W
$R\theta_{JC}$	Thermal resistance (junction-to-case)	0.2	°C/W
Ψ_{JT}	Thermal characterization parameter (junction-to-package top)	19.2	°C/W

6.2.1.2 WLCSP208 Package Outline

Figure 6-3 presents WLCSP208 package outline.

Figure 6-3 WLCSP208 Package Outline (1)

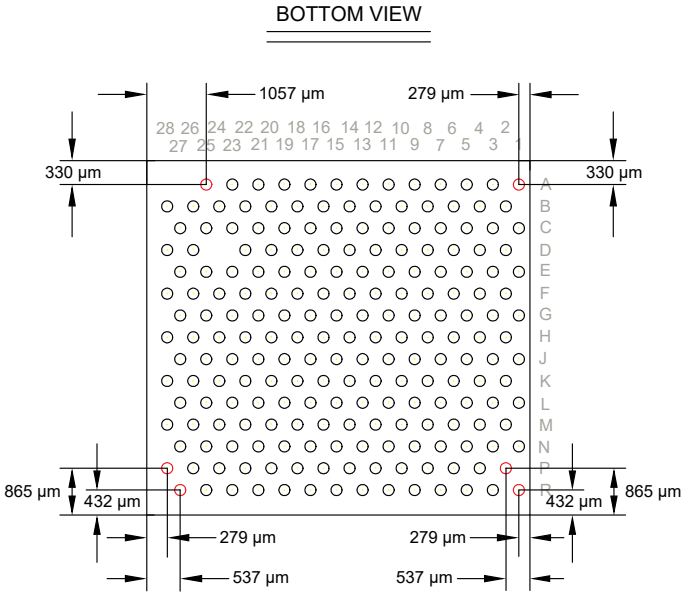


DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.485	0.510	0.535
A1	0.145	0.160	0.175
A2	0.330	0.350	0.370
b	0.215	0.235	0.255

1. All linear dimensions are in millimeters.

Figure 6-4 presents the bump distances from the cut edge of the WLCSP208 package.

Figure 6-4 WLCSP208 Package Bump Distances from Cut Edge



6.2.2 FBGA194 Package Information

6.2.2.1 FBGA194 Thermal Operating Specifications

Table 6-4 provides thermal operating specifications for FBGA194 package.

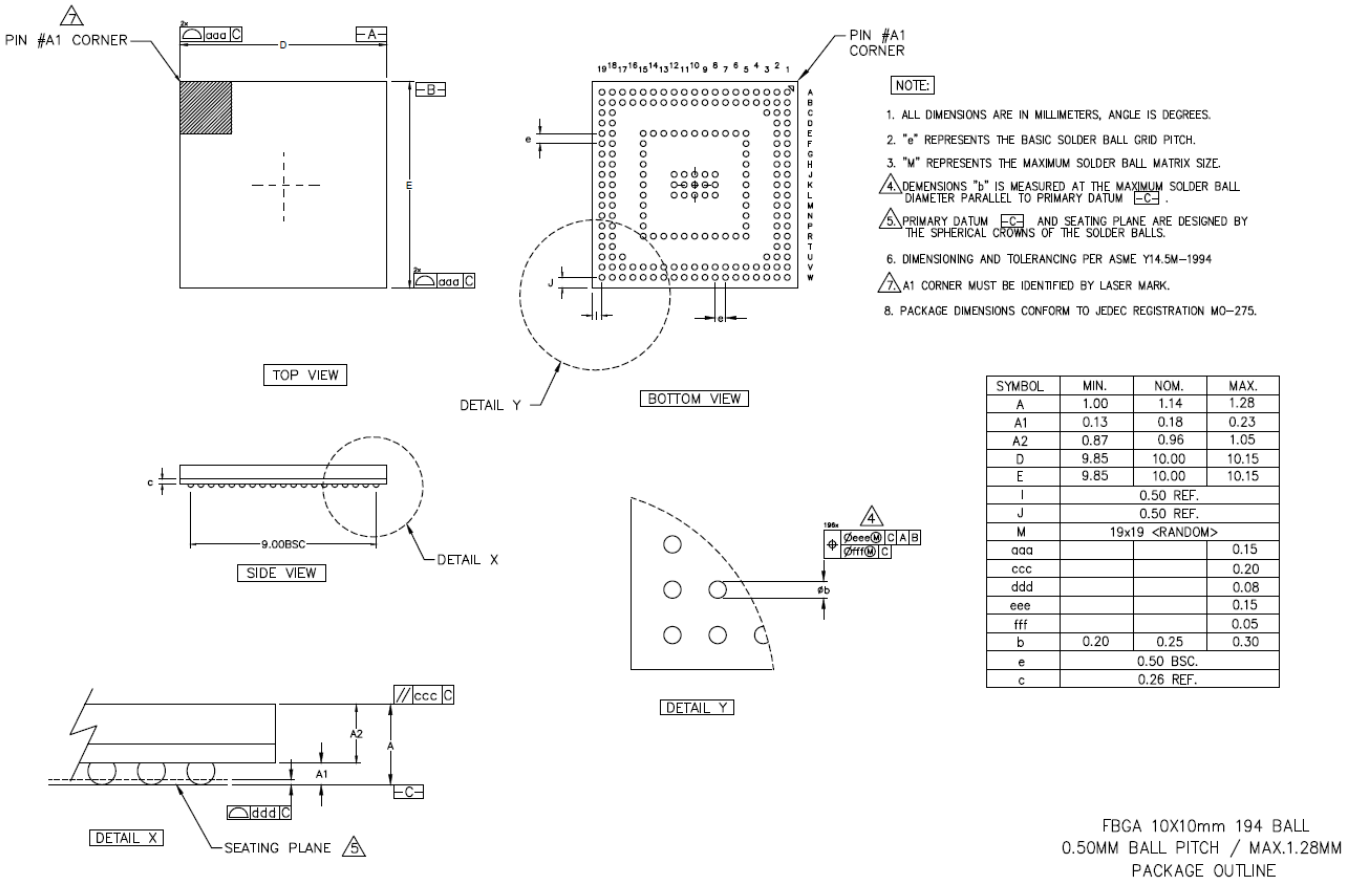
Table 6-4 FBGA194 Thermal Operating Specifications

Parameter		Value	Unit
θ_{JA}	Thermal resistance in natural convection (junction-to-free air)	21.1	°C/W
θ_{JC}	Thermal resistance (junction-to-case)	17.0	°C/W
Ψ_{JT}	Thermal characterization parameter (junction-to-package top)	21.0	°C/W

6.2.2.2 FBGA194 Package Outline

Figure 6-5 presents FBGA194 package outline.

Figure 6-5 FBGA194 Package Outline (1)



SYMBOL	MIN.	NOM.	MAX.
A	1.00	1.14	1.28
A1	0.13	0.18	0.23
A2	0.87	0.96	1.05
D	9.85	10.00	10.15
E	9.85	10.00	10.15
I		0.50 REF.	
J		0.50 REF.	
M		19x19 <RANDOM>	
aaa			0.15
ccc			0.20
ddd			0.08
eee			0.15
fff			0.05
b	0.20	0.25	0.30
e		0.50 BSC.	
c		0.26 REF.	

1. All linear dimensions are in millimeters.

6.3 Storage Conditions

Table 6-5 defines specifics in the storage conditions.

Table 6-5 Storage Conditions

Parameter			Min	Max	Unit
T_{STG}	Storage temperature		-40	150	°C
%RH	Relative Humidity	WLCSP package: MSL1 (Moisture Sensitivity Level)			
		FBGA package: MSL3			

7 Ordering Information

Table 7-1 presents the optional features for each orderable part number.

Table 7-1 Orderable Part Numbers

Part Number[(1)]	NPU-HP	CANFD	MRAM	SRAM	GPIO (1.8 V)	Package	Operating Temperature
AE302F80F55D5AE	Yes	Yes	5.5MB	13.5MB	120	WLCSP208	Extended
AE302F80F5582AE	Yes	Yes	5.5MB	8.25MB	120	WLCSP208	Extended
AE302F80F55D5LE	Yes	Yes	5.5MB	13.5MB	120	FBGA194	Extended
AE302F80F5582LE	Yes	Yes	5.5MB	8.25MB	120	FBGA194	Extended
AE302F80C1557LE	Yes	No	1.5MB	5.75MB	120	FBGA194	Extended
AE302F40C1537LE	No	No	1.5MB	3.75MB	120	FBGA194	Extended

1. Ordering designation for shipment packaging:
   - Add the following suffix to base part number
     - -T, for Tape and Reel
     - -Y, for Tray
   - Example: AE302F80F55D5AE-T is Tape and Reel

Table 7-2 shows the user SRAM banks with their corresponding sizes (in KB) available for each part number.

Table 7-2 Part Numbers SRAM Breakdown

Part Number	Total SRAM (KB)	SRAM0 (KB)	SRAM1 (KB)	SRAM2 (M55-HP ITCM) (KB)	SRAM3 (M55-HP DTCM) (KB)	SRAM4 (M55-HE ITCM) (KB)	SRAM5 (M55-HE DTCM) (KB)	SRAM6 (KB)	SRAM7 (KB)	SRAM8 (KB)	SRAM9 (KB)
AE302F80F55D5AE	13824	4096	2560	256	1024	256	256	2048	512	2048	768
AE302F80F5582AE	8448	4096	2560	256	1024	256	256	N/A	N/A	N/A	N/A
AE302F80F55D5LE	13824	4096	2560	256	1024	256	256	2048	512	2048	768
AE302F80F5582LE	8448	4096	2560	256	1024	256	256	N/A	N/A	N/A	N/A
AE302F80C1557LE	5888	4096	N/A	256	1024	256	256	N/A	N/A	N/A	N/A
AE302F40C1537LE	3840	N/A	2048	256	1024	256	256	N/A	N/A	N/A	N/A

It is possible to configure address ranges within SRAM0 and SRAM1 to appear as contiguous address space to a given M55 core through configuration of the firewall controllers. For more information on the firewalls, refer to the corresponding device series-specific Hardware Reference Manual, Section Interconnect Firewall Functional Description.

For complete part number decoding, see Section 6.1 Device Marking Definition.

8 Legal and Support Information

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8.2 Related Documents and Tools

- Alif Semiconductor E3 Series Hardware Reference Manual (HWRM)
- Alif Semiconductor E Series Software Reference Manual (SWRM)

For additional Alif Semiconductor technical documentation and software resources please visit:

- User Guides & App Notes
- Software & Tools

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

8.3 Contact Information

For more information visit our website Alif Semiconductor or contact us:

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8.5 Acronyms

3

3GPP
3rd Generation Partnership Project

A

ACP
Accelerator Coherency Port

ADC
Analog to Digital Converter

AES
Advanced Encryption Standard

AHI
Application Host Interface

AI
Artificial Intelligence

aiPM
autonomous intelligent Power Management

AON
Always On

API
Application Programming Interface

APSS
Application Processor Subsystem

ATOC
Application Table of Content

B

BER
Bit-Error Ratio

BLE
Bluetooth Low Energy

BLIT
Block Image Transfers

BOD
Brown-Out Detect

BOR
Brown-Out Reset

BPU
Breakpoint Unit

C

CAN
Controller Area Network

CANFD
Controller Area Network with Flexible Data rate

CCC
Common Command Code

CDC
Configurable DPI Controller

CDM
Charged Device Model

CLUT
Color Look-Up Table

CMP
Comparator

CMSIS
Common Microcontroller Software Interface Standard

CNN
Convolutional Neural Network

CPI
Camera Parallel Interface

CPU
Central Processing Unit

CRC
Cyclic Redundancy Check

CSI
Camera Serial Interface

D

DAC
Digital to Analog Converter

DAP
Debug Access Port

DDR
Double Data Rate

DL
Display List / Download

DLR
Display List Reader

DM
Device Manufacturer

DMA
Direct Memory Access

DMAC
Direct Memory Access Controller

DMIC
Digital Microphone

DPA
Differential Power Analysis

DPI
Display Parallel Interface / Display Pixel Interface

DPU
Data Processing Unit

DRD
Dual-Role Device

DSC
Display Stream Compression

DSI
Display Serial Interface

DTCM
Data Tightly-Coupled Memory

DWT
Data Watchpoint and Trace

E

ECB
Electronic Codebook

ECC
Error-Correcting Code / Elliptic-Curve Cryptography

eDRX
Extended Discontinuous Reception

EMC
Electromagnetic Compatibility

EMFI
Electromagnetic Fault Injection

EMI
Electromagnetic Interference

EMS
Electromagnetic Susceptibility

EOL
End of Life

EoTp
End of Transmission Packet

EPU
Extension Processing Unit

ESD
Electrostatic Discharge

eSIM
Embedded Subscriber Identity Module

ETH
Ethernet

EVTRTR
Event Router

EWIC
External Wakeup Interrupt Controller

F

FC
Firewall Component

FIR
Finite Impulse Response

FSR
Full-Scale Range

G

GIC
Generic Interrupt Controller

GNSS
Global Navigation Satellite Subsystem

GOPS
Giga Operations Per Second

GPIO
General-Purpose Input/Output

GPS
Global Positioning System

GPU
Graphics Processing Unit

H

HBM
Human Body Model

HCI
Host Communication Interface

HDR
High Data Rate

HE
High Efficiency

HFRC
High-Frequency Resistor-Capacitor

HFXO
High-Frequency Crystal Oscillator

HMI
Human Machine Interface

HP
High Performance

HPP
High Performance Point

HUK
Hardware Unique Key

HWRM
Hardware Reference Manual

HWSEM
Hardware Semaphore

I

I2C
Inter-Integrated Circuit

I2S
Inter-IC Sound

I3C
Improved Inter-Integrated Circuit

IBI
In-Band Interrupt

ICMP
Internet Control Message Protocol

ICV
Integration Circuit Vendor

IDE
Integrated Design Environment

IFG
Interframe Gap

IFU
Instruction Fetch Unit

IIR
Infinite Impulse Response

IMD
Intermodulation Distortion

IoT
Internet of Things

IPC
Inter-Process Communication

IPI
Image Pixel Interface

IRQRTR
Interrupt Router

iSIM
Integrated Subscriber Identity Module

ISP
In-System Programming

ITCM
Instruction Tightly-Coupled Memory

iUICC
integrated Universal Integrated Circuit Card

IWIC
Internal Wakeup Interrupt Controller

L

LCD
Liquid Crystal Display

LCS
Life Cycle State

LDE
Lockdown Extension

LDO
Low Drop-Out

LE
Low Energy

LFRC
Low-Frequency Resistor-Capacitor

LFXO
Low-Frequency Crystal Oscillator

LOM
Listen Only Mode

LP
Low-Power

LPCMP
Low-Power Comparator

LPGPIO
Low-Power General-Purpose Input/Output

LPI2C
Low-Power Inter-Integrated Circuit

LPI2S
Low-Power Inter-IC Sound

LPM
Link Power Management

LPP
Low Performance Point

LPPDM
Low-Power Pulse Density Modulation

LPRTC
Low-Power Real-Time Counter

LPSPI
Low-Power Serial Peripheral Interface

LPTIMER
Low-Power Timer

LSB
Least Significant Bit

LTE
Long-Term Evolution

LUT
Look-Up Table

M

MAC
Media Access Controller

MAU
Memory Authentication Unit

MBI
Master Bus Interface

MCU
Microcontroller Unit

ME
Monitor Extension

MHU
Message Handling Unit

ML
Machine Learning

MMU
Memory Management Unit

MPE
Master Permission Entry

MPU
Memory Protection Unit

MRAM
Magnetoresistive Random-Access Memory

MSL
Moisture Sensitivity Level

MTL
MAC Transaction Layer

MVE
M-profile Vector Extension

MWS
Mobile Wireless Standard

N

NMI
Non-Maskable Interrupt

NPP
Nominal Performance Point

NPU
Neural Processing Unit

NPU-HE
Neural Processing Unit-High Efficiency

NPU-HP
Neural Processing Unit-High Performance

NRZ
Non-Return-to-Zero

NS
Non-Secure

NVIC
Nested Vectored Interrupt Controller

NVM
Non-Volatile Memory

O

OCS
OEM-signed Configuration Settings

OEM
Original Equipment Manufacturer

OPP
Operating Performance Point

OSPI
Octal Serial Peripheral Interface

OToC
OEM-signed Table of Contents

OTP
One Time Programmable

P

PCB
Printed Circuit Board

PCM
Pulse Code Modulation

PD
Power Domain

PDM
Pulse Density Modulation

PE
Protection Extension

PLL
Phase-Locked Loop

PMU
Performance Monitoring Unit

POR
Power-On-Reset

PPI
PHY Protocol Interface / Private Peripheral Interrupt

PPS
Precise Positioning Service

PPU
Power Policy Unit

PSC
Power Sequence Controller

PSM
Power Saving Mode

PSRAM
Pseudo-Static Random-Access Memory

PSRR
Power Supply Rejection Ratio

PWM
Pulse Width Modulation

Q

QEC
Quadrature Encoder Counter

R

RAI
Release Assistance Indication

RDC
Receiver Delay Compensation

RF
Radio Frequency

RFI
Radio Frequency Interference

RLE
Run-Length Encoding

RMA
Return Merchandise Authorization

RNN
Recurrent Neural Network

RO
Read Only

ROM
Read Only Memory

RoT
Root-of-Trust

RSA
Rivest–Shamir–Adleman

RSE
Region Size Extension

RSSI
Received Signal Strength Indicator

RSTC
Reset Controller

RTC
Real-Time Counter

RTOS
Real-Time Operating System

RTSS
Real-Time Subsystem

RW
Read/Write

S

SAR
Successive Approximation Register

SAU
Security Attribution Unit

SBI
Slave Bus Interface

SCU
Snoop Control Unit

SDA
Serial Data

SDIO
Secure Digital Input/Output

SDMMC
Secure Digital / Embedded Multimedia Card

SDR
Single Data Rate

SE
Secure Enclave / Secure Enable

SESS
Secure Enclave Subsystem

SFD
Start of Frame Data / Start Frame Delimiter

SGI
Software Generated Interrupt

SHA
Secure Hash Algorithm

SIM
Subscriber Identity Module

SIMD
Single Instruction Multiple Data

SJW
Synchronization Jump Width

SMP
Symmetric Multi-Processing

SNR
Signal-to-Noise Ratio

SPA
Simple Power Analysis

SPI
Serial Peripheral Interface / Shared Peripheral Interrupt

SRAM
Static Random-Access Memory

SSP
Synchronous Serial Protocol

SST
Single Shot Transmission

STB
Store Buffer

STOC
System Table of Content

SWD
Serial Wire Debug

SWRM
Software Reference Manual

T

TCM
Tightly-Coupled Memory

TCP
Transmission Control Protocol

TDC
Transmitter Delay Compensation

TE
Translation Extension

TEE
Trusted Execution Environment

TFT
Thin-Film-Translator

TGU
TCM Gate Unit

TOC
Table of Content

TRNG
True Random Number Generator

TSENS
Temperature Sensor

U

UART
Universal Asynchronous Receiver/Transmitter

UDE
Unprivileged Debug Extension

UDP
User Datagram Protocol

UI
Unit Interval / User Interface

UL
Upload

UPP
Ultra-Low Performance Point

USB
Universal Serial Bus

UTIMER
Universal Timer

V

VTOR
Vector Table Offset Register

W

WDT
Watchdog Timer

WFE
Wait For Event

WFI
Wait For Interrupt

X

XIP
eXecute-in-Place

XO
Execute Only

Z

ZI
Zero Initialized

9 Revision History

Table 9-1 provides the history of changes to this document.

Table 9-1 Revision History

Date	Revision	Changes
January 2025	2.11	Changes from previous revision include: ■ Updated the caution statement at the beginning of Section 4.2 Pin Function Options by Location ■ Updated bump distances from cut edge in Figure 6-3 WLCSP208 Package Outline and Figure 6-4 WLCSP208 Package Bump Distances from Cut Edge. Note: The dimensions of the actual WLCSP208 device remain unchanged. ■ Editorial enhancements
December 2024	2.10	Changes from previous revision include: ■ Added note regarding Low Power peripherals access in Table 2-1 Device Features and Peripherals ■ Updated Section 3.2 Neural Processing Unit (NPU) ■ Updated note under Figure 3-5 Device Clocking Scheme Overview ■ Added notes regarding Low Power peripherals access in Section 3.14.1 LPTIMER Overview, Section 3.14.4 LPRTC Overview, Section 3.15 General-Purpose Input/Output Module, Section 3.16.4 I2C Overview, Section 3.16.5 I2S Overview, Section 3.16.7 PDM Overview, Section 3.16.9 UART Overview, Section 3.18.1 CPI Overview, and Section 3.20.4 LPCMP Overview ■ Updated Table 5-36 OSPI Timing Characteristics with information on DATA input line delay and RXDS line compensation ■ Added Figure 5-15 OSPI Timing Diagram - DDR Mode (Transmit) and Figure 5-16 OSPI Timing Diagram - DDR Mode (Receive) ■ Updated Table 6-1 Product Identification ■ Editorial enhancements