DATASHEET

ENSEMBLE™ FAMILY
E1C SERIES
EMBEDDED MICROCONTROLLERS

EXTREME LOW POWER MCU: CORTEX-M55 CPU w/HELIUM VECTOR EXT, ETHOS-U55 NPU, DEEP SECURITY, MIPI-DSI, CAN-FD, 2D GPU, CAMERA I/F, ANALOG, 2MB SRAM, 1.9MB MRAM

Features

High-Efficiency MCU Core

- High-Efficiency (HE) Arm® Cortex®-M55 Core, up to 160 MHz, with Helium™ Vector Processing Extension, Double-Precision FPU, 2MB of SRAM 0-wait State Tightly Coupled Memory, 16KB Instruction and Data Caches, Armv8.1-M ISA with Arm TrustZone®, and 4.37 CoreMark®/MHz Performance Benchmark
- High-Performance 64-bit AXI Bus Fabric

Efficient Micro NPU for ML/AI Acceleration

- 1× Ethos-U55 NPU (NPU-HE), 128 MAC/cycle up to 160 MHz and 46 GOPS, Supporting RNN and CNN Networks
- Up to Two Orders of Magnitude Uplift in Performance and Power Efficiency per ML Inference Compared to Same ML Model Running on Typical Previous Generation Cortex-M Cores without Neural Processing Acceleration

Extreme-Low Power Technology

- Autonomous Intelligent Power Management (*ai*PM™)
- FD-SOI Low Leakage Process
- 700 nA at 3.3 V Consumed in STOP Mode with LPRTC Running, 5.0 ms Wake Time from STOP Mode
- As Low as 27 µA/MHz Dynamic Consumption for High-Efficiency Cortex-M55 at 3.3 V

On-Chip Application Memory

- High Endurance MRAM Non-Volatile Memory
  - Up to 1.9MB
- SRAM
  - Up to 2MB Zero Wait-State with Optional Retention in Increments of 64KB (450 nA), 128KB (900 nA), 256KB (1.8 µA), 512KB (3.6 µA), 1MB (7.2 µA), 2MB (14.4 µA)

External Memory Interfaces

- 1× Octal SPI at up to 80 MHz for up to 80 MB/s SDR, 160 MB/s DDR, with Inline AES Decryption, XIP Mode Support, HyperBus Protocol Support, Enabling External Memory Expansion, QSPI Support
- 1× SD® v4.2, eMMC™ v5.1 Channel with DMA

Secure Enclave

- Hardware-based Root-of-Trust (RoT) with Unique Device ID
- Secure Boot
- Crypto API for AES, AEAD, SHA, CMAC, TRNG operations
- Crypto Accelerators—AES (up to AES-256), SHA (up to SHA-256), RSA (up to RSA-3072), and NIST compliant TRNG
- Secure Debugging with Certificate Authentication
- Complete Secure Lifecycle Management

Timing Control and Measurement

- 4× Universal High-Resolution 32-bit Timers, Quadrature Encoder/Decoder (QEC) Enabled
- 1× Watchdog Timer
- 2× Low-Power 32-bit Timers
- 1× Real-Time Counter

Serial Communication Interfaces

- 1× USB 2.0 HS/FS Device with DMA
- 1× SDIO v4.1 Channel with DMA
- 2× CAN FD Channels up to 10 Mbps
- 1× MIPI® I3C® Channel
- 2× I2C Channels up to 1.0 Mbps Throughput
- 1× Low-Power I2C Channel
- 6× UART Channels up to 2.5 Mbps (2× with RS-485 Driver Control)
- 1× Low-Power UART Channel
- 3× SPI Channels up to 40 Mbps Throughput
- 1× Low-Power SPI Channel

Analog Interface Capabilities

- 2× 12-bit SAR ADC (12 Single-Ended Inputs)
- 1× 24-bit Sigma-Delta ADC (4 Differential Inputs)
  - Programmable Gain Instrumentation Amplifier (1× to 128×)
- 1× 12-bit DAC (1 channel)
- 2× High-Speed Analog Comparator (8 Inputs)
- 1× Low-Power Analog Comparator (4 Inputs)
- Internal Temperature Sensor
- Internal Precision Reference Voltage

Camera Interfaces

- 1× Low-Power Camera Parallel Interface (LPCPI), up to 8 bits

Display Interfaces

- Graphics LCD Controller
- 1× Display Parallel Interface (DPI), up to 24-bit RGB
- 1× 1-Lane MIPI D-PHY DSI®

Graphics

- D/AVE 2D Graphics Processing Unit

Audio Interfaces

- 2× I2S Synchronous Stereo Audio Interfaces
- 1× Low-Power I2S Stereo Audio Interface
- 4× 2-channel Low-Power Pulse Density Modulation (LPPDM) Microphone Inputs (8 Mono Microphones)

General Input/Output

- Up to 68× 1.8-V GPIOs (Shared with Peripherals)
- Up to 6× Selectable 1.8-V to 3.3-V GPIOs (Shared with Peripherals)

Clock Generation

- LFRC - Internal Low-Frequency RC Oscillator (32.7 kHz, ±4%)
- HFRC - Internal High-Frequency RC Oscillator (Up to 76.8 MHz, ±2%)
- LFXO - External Low-Power Crystal Oscillator or Quartz Crystal (32.768 kHz)
- HFXO - External High-Frequency Crystal Oscillator or Quartz Crystal (24 MHz to 38.4 MHz)
- One User Fractional Mode PLL, One Fractional Audio PLL

System

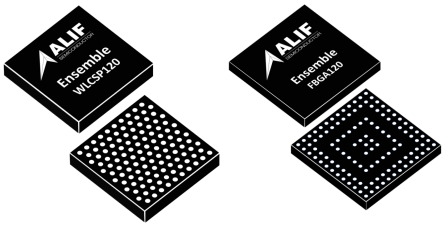
- General DMA Controller
- CRC Calculation Accelerator with Programmable Polynomials
- Programmable Low Supply Voltage Detect Warning (Brown-Out Detect)
- Power-On Reset and Brown Out Reset
- Real-Time Clock
- JTAG/SWD Debug Interface

Operating Parameters

- 1.75 V to 4.8 V Primary Supply Range
- -40 °C to 105 °C Industrial Ambient Temperature Range
- -40 °C to 125 °C Industrial Junction Temperature Range

Packages

- WLCSP120, 3.9 mm x 3.9 mm, 0.35 mm Pitch
- FBGA120, 6.6 mm x 6.6 mm, 0.5 mm Pitch



WLCSP FBGA

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1 Preface

This document contains fundamental technical information for the E1 Compact (E1C) embedded microcontrollers from the Ensemble™ family.

Device information herein includes features description, electrical and mechanical characteristics with specifications, and ordering information.

There are references to third-party technical documents as noted within this document.

For more information on processors, peripheral functions, and programming settings, refer to the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

2 Device Overview

2.1 Device Description

Alif Semiconductor's E1C family of MCUs are highly integrated embedded processor devices for use in wearables and intelligent IoT end-point applications. Architected for power efficiency, these devices deliver high computation and ML/AI capability, wired connectivity, multi-layered security, computer vision, and highly interactive human-machine interface. Across all devices are common peripherals, common power management schemes, and a common interconnection fabric making it easy to re-use software and hardware over many varied projects.

Power efficiency—In addition to the use of FD-SOI silicon process technology, *ai*PM provides fine granular control over the processing, memory, and peripheral resources of the device, resulting in extreme power conservation that consumes only what is needed, when its needed, at any given instant based on use case.

Computation and ML/AI—Single-core design with one Arm Cortex-M55 Real-Time core, optimized for extreme low power operation. Machine Learning and AI tasks are accelerated by an Arm Ethos-U55 neural processing unit generating as much as 46 GOPS. E1C devices can operate with an RTOS, while using only the on-chip memory resources. Additional RAM or Flash memory may be accessed externally through a high-speed Octal SPI interface supporting XIP mode and HyperBus protocol. An in-line AES decryption module in the Octal SPI interface ensures the confidentiality of the data and/or code stored in the external memory devices.

Connectivity—E1C devices support many wired interfaces including USB, UART, SDIO, CANFD, I3C, I2C, and more.

Security—An isolated Secure Enclave manages the entire life cycle of the end application from manufacture, to deployment, to secure Firmware Over-The-Air updates, and to retirement. A unique Root-of-Trust existing in the enclave enables a trusted on-chip platform for key generation, secure storage, secure boot, cryptographic acceleration, and more. The Secure Enclave also enables certificate-based secure debugging.

Computer Vision—Integrated camera interface enables connection of low-power image sensors for AI image classification using the Arm Ethos-U55 NPU. Biometric ID, face detection, object classification, barcode reading, and other vision applications can execute while consuming very little energy.

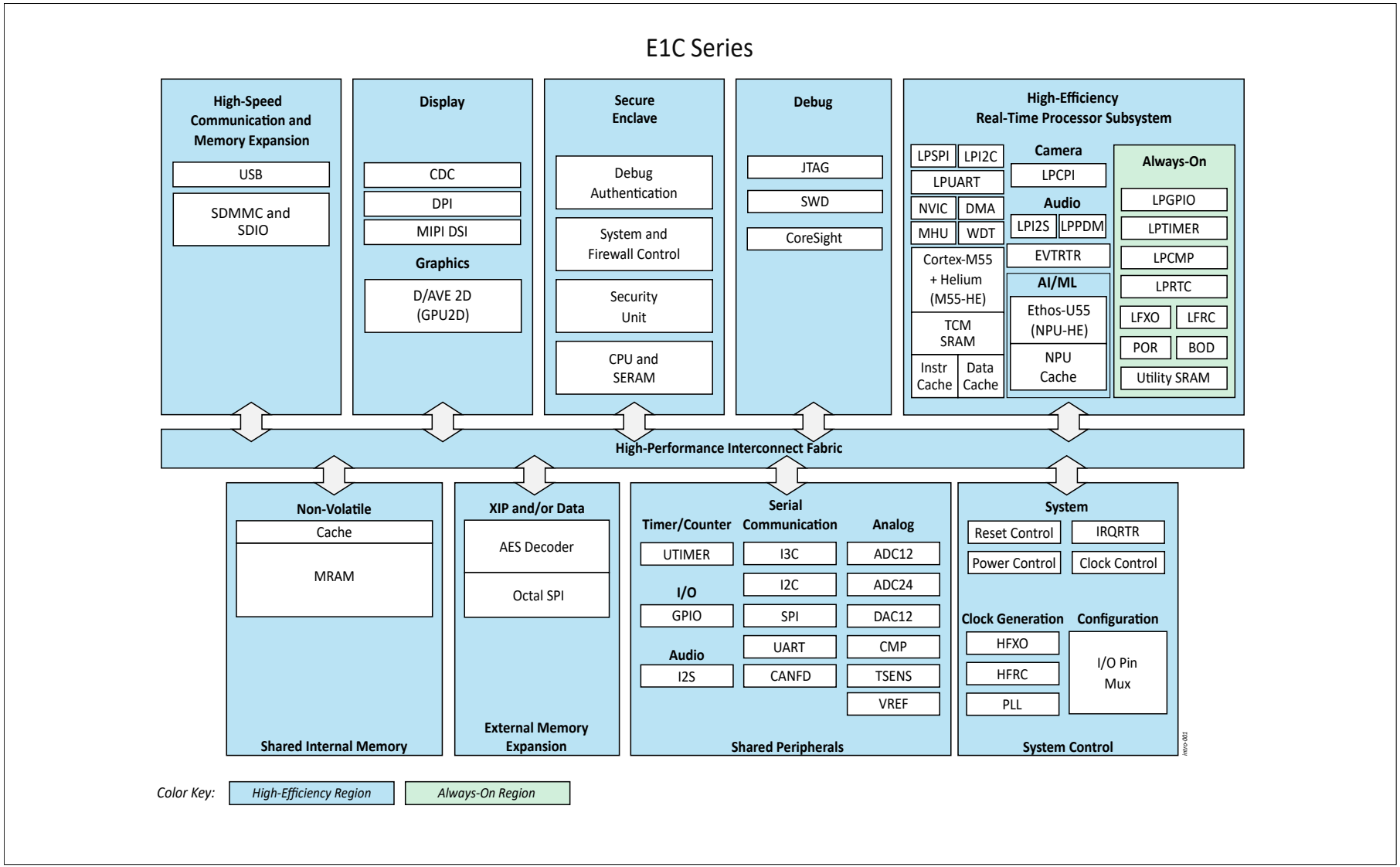
Sensor Fusion and Voice Processing—The Arm Ethos-U55 NPU and the Helium vector extension on the Cortex-M55 CPU can be utilized to enable extremely fast and energy efficient processing of digitized sensor inputs from multiple sources. Helium accelerates DSP functions and Ethos brings ML-enhanced processing to portable applications measuring human metrics, mechanical vibrations, sounds, as well as key word spotting and interpreting voice commands through microphone inputs via LPPDM and LPI2S interfaces.

Color Display—Integrated color display interfaces, including MIPI DSI, can drive a wide range of display panels with vivid graphics supported by the on-chip 2D graphics processing unit for attractive user interfaces.

2.2 Device Block Diagram

Figure 2-1 presents a simplified diagram of the operating regions and main internal components of the Alif Semiconductor E1C Series of devices.

Figure 2-1 Device Block Diagram



2.3 Device Features Summary and Comparison

Table 2-1 presents device features supported and package options.

Table 2-1 Device Features and Peripherals

Feature		Definition
Package options		WLCSP120, FBGA120
Processors and Accelerators		
High-Efficiency Arm Cortex-M55	M55-HE	Up to 160 MHz
Arm Ethos-U55 Neural Processing Units	NPU-HE	Optional (3) Up to 46 GOPS
D/AVE 2D Graphics Processing Unit	GPU2D	Optional (3)
Security Subsystem		
Secure Enclave	SE	Yes
Memory		
On-Chip Non-volatile Application Memory	MRAM	Up to 1.9MB (3)
On-Chip Application SRAM	SRAM	Up to 2MB (3)
Timers and Counters		
Low-Power Timer	LPTIMER (2)	2 × 32-bit
Universal Timer	UTIMER	4 × 32-bit
Watchdog Timer	WDT	1
Low-Power Real-Time Counter	LPRTC (2)	1
General Input and Output		
General Purpose I/O pins	GPIO	Optional (3) 67 (1.8 V) 5 (1.8 V or 3.3 V)
Low-Power General Purpose I/O pins	LPGPIO (2)	1 (1.8 V) 1 (1.8 V or 3.3 V)
Communication Peripherals		
Controller Area Network	CANFD	Optional (3)
Inter-Integrated Circuit	I2C	2
	LPI2C (2)	1
Inter-IC Sound	I2S	2
	LPI2S (2)	1
MIPI Improved Inter-Integrated Circuit	I3C	1
Pulse Density Modulation	LPPDM (2)	4× 2-channel
Serial Peripheral Interface	SPI	3
	LPSPI (2)	1
Universal Asynchronous Receiver/Transmitter	UART	6
	LPUART (2)	1
Universal Serial Bus	USB	USB 2.0 HS/FS Device Mode
Secure Digital Input Output	SDIO	SDIO v4.1 (1)

Feature		Definition
External Memory Interfaces		
Octal SPI	OSPI	1
Secure Digital Multimedia Card	SDMMC	SD v4.2, eMMC v5.1 (1)
Camera Subsystem		
Camera Parallel Interface	LPCPI (2)	Up to 8-bit
Display Subsystem		
Graphics LCD Controller	CDC	Optional (3)
Display Parallel Interface	DPI	Optional (3) Up to 24-bit RGB
MIPI Display Serial Interface	DSI	Optional (3) 1-Lane
Analog Peripherals		
Analog-to-Digital Converter	ADC12	2 × 12-bit (Up to 12 inputs)
	ADC24	1 × 24-bit (Up to 4 differential inputs)
Digital-to-Analog Converter	DAC12	1 × 12-bit
High-Speed Comparator	CMP	2 (8 inputs)
Low Power Comparator	LPCMP (2)	1 (4 inputs)
Temperature Sensor	TSENS	Yes

1. SDIO, SD, and eMMC are functions of memory card controller. There is only one memory card controller in the device.
2. All Low Power (LP) peripherals are single-master accessible. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.
3. For devices supporting optional features, see Section 7 Ordering Information.

3 Functional Overview

3.1 Real-Time Processor

3.1.1 M55-HE Overview

The Cortex-M55 High-Efficiency (M55-HE) processor implements the Armv8.1-M Mainline architecture that includes support for the M-profile Vector Extension (MVE), also known as Helium™. The M55-HE achieves high compute efficiency across scalar and vector operations, operating up to 160 MHz.

The M55-HE memories are based on ultra-low leakage memory cells which results in low power consumption in sleep mode. The choice of TCM retention allows application-optimized tradeoff between current leakage during sleep and fast wake-up time.

The device includes a single M55-HE processor that resides in the High-Efficiency Real-Time Subsystem (RTSS-HE). The RTSS-HE also includes various memories and peripherals.

The M55-HE processor supports the following main features:

- CPU revision: r1p0
- CPU core logic that includes:
  - In-order, four-stage integer pipeline with early completion of common arithmetic instructions
  - Instruction Fetch Unit (IFU) with 32-bit instruction fetch data width
  - Data Processing Unit (DPU) with 64-bit load/store data width
  - Support for up to 2 × 32-bit vector load operations in parallel
- Extension Processing Unit (EPU) that works closely with the CPU core to support:
  - Scalar floating-point (VFPv5) operations: half-, single-, and double-precision
  - Vectored operations through MVE (Helium)
    - Integer
    - 128-bit SIMD floating-point: half- and single-precision
- Double-Precision FPU
- Support for other Extensions such as:
  - Armv8.1-M Main Extension (16-bit and 32-bit Thumb instruction set)
  - Armv8-M Security Extension (TrustZone)
  - DSP Extension
  - DSP Debug Extension
  - Reliability, Availability, and Serviceability (RAS) Extension
  - Unprivileged Debug Extension (UDE)
- Memory architecture that includes:
  - Memory Authentication Unit (MAU) for memory access control:
    - Secure Memory Protection Unit (MPU) supporting 16 regions
    - Non-secure MPU supporting 16 regions
    - Security Attribution Unit (SAU) supporting 8 regions
    - TCM Gate Units (TGU):
      - Instruction TGU (ITGU) protecting 4 RAM regions, each 128KB in size
      - Data TGU (DTGU) protecting 12 RAM regions, each 128KB in size
  - Memory system:
    - 32KB L1 Instruction Cache (IRAM)
    - 32KB L1 Data Cache (DRAM)
    - Up to 512KB Instruction TCM (ITCM); access to ITCM is over a single interface

    - Up to 1536KB Data TCM (DTCM); access to DTCM is over four interfaces
    - Master AXI (M-AXI) interface for high latency memory or peripheral access
- Interrupt control:
  - Nested Vectored Interrupt Controller (NVIC) for low-latency interrupt processing:
    - Supports 480 external interrupts, with 256 priority levels per interrupt
  - Wakeup interrupt control to allow the processor to enter low-power state:
    - Internal Wakeup Interrupt Controller (IWIC)
    - External Wakeup Interrupt Controller (EWIC)
- Secure and non-secure Vector Table Offset Register (VTOR)
- Debug and trace support:
  - Full set debug:
    - Breakpoint Unit (BPU) with 8 comparators
    - Data Watchpoint and Trace (DWT) unit with 4 comparators and Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - CoreSight-compliant Debug Access Port (DAP):
    - Supports dynamic switching—Serial Wire / JTAG Debug Port (SWJ-DP)

3.2 Neural Processing Unit (NPU)

The Arm Ethos-U55 Neural Processing Unit (NPU) is a Machine Learning (ML) coprocessor that improves the inference performance of neural networks (NN).

The NPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN). The NPU includes a Direct Memory Access (DMA) controller that can read and write to external memory. The DMA controller reads the neural network description and transfers the input and output feature maps.

The device includes up to one NPU coprocessor in the device High-Efficiency Region—NPU-HE.

3.2.1 NPU-HE Overview

The NPU-HE supports the following main features:

- Up to 46 GOPS performance using up to 128 MAC/cycle
- Network support: CNN, RNN
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)
- Activation functions:
  - ReLU, ReLU1, ReLU6, and Leaky ReLU (LReLU)
  - Tanh
  - Sigmoid
  - Configurable Look-Up Table (LUT)
  - None or bypass
- Element-wise operations:
  - Element-wise ADD and SUB
  - Element-wise Multiplication (MUL)
  - Element-wise Min and Max
  - Element-wise ABS
  - Element-wise Shift Left (SHL) and Shift Right (SHR)
  - Element-wise Count-Leading Zero (CLZ)
- 24KB of internal shared cache memory (SHRAM)

- Integrated DMA controller
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

3.3 2D-Graphics Accelerator (GPU)

The D/AVE 2D Graphics Processing Unit (GPU2D) provides hardware acceleration for sophisticated vector-based graphical applications.

The device includes one GPU2D module.

The GPU2D supports the following main features:

- Subpixel accurate rendering
- Resolutions of up to 2048 × 2048 pixels
- Operating clock frequency at 160 MHz. GPU render pipeline produces one pixel per clock cycle.
- 16 blending modes
- Patterns and gradients with alpha channel on all primitives
- Render to texture
- Textures up to 2048 × 1024 pixels
- Texture blending
- Bilinear filtering
- Graphical primitives available:
  - Block Image Transfers (BLIT)—direct and stretch
  - Box
  - Circle—filled or empty (ring)
  - Convex polygon
  - Line
    - Supported caps:
      - Butt
      - Round
      - Square
    - Supported line joins:
      - Bevel
      - Miter
      - Round
    - Supporting different start and end widths
  - Quad
  - Triangle
  - Triangle fan
  - Triangle list
  - Triangle stripe
  - Wedge-filled or empty
- Graphical primitives attributes:
  - Anti-aliasing
  - Blend modes
  - Color
  - Edge blur
  - Linear alpha gradient
  - Pattern
  - Texture
    - U/V clamp, repeat support
    - No-, linear-, bilinear-filtering support

    - Run-Length Encoding (RLE)
- Supported color coding formats:
  - Input
    - ARGB8888, RGB565, ARGB4444, ARGB1555, ALPHA8, AI44, RGBA8888, RGBA4444, RGBA5551, I8, I4, I2, I1, ALPHA4, ALPHA2, ALPHA1
  - Output
    - ARGB8888, RGB565, ARGB4444, ALPHA8, RGBA8888, RGBA4444

3.4 Secure Enclave Subsystem (SESS)

3.4.1 Security Architecture Overview

The device contains an advanced Secure Enclave (SE) that is responsible for managing the device security. The SE is an isolated subsystem with its own dedicated resources. The isolated subsystem reduces the attack surface for the SE along with the minimal software interfaces that are restricted to the Inter-Process Communication (IPC) Message Handling Units (MHUs).

The SE boots first on Power-On-Reset (cold start) while all other cores are held in wait. The SE runs the First Stage bootloader code from a private, immutable ROM. The SE performs certificate-based integrity and authenticity check on the Second Stage bootloader image stored in the Alif dedicated portion of MRAM. It is loaded to the SE's SRAM (SERAM) and the flow of execution is transferred to it. This mechanism enables the secure update of the Second Stage bootloader in the field. The boot process continues with processing of the application-ATOC. The SE applies configuration settings in the ATOC that partition the system resources (memory and peripherals) between the different application cores. Next, as specified in the ATOC, the SE bootloader performs a signature verification of the installed application binaries. If needed, it copies the specified binaries to their designated SRAM regions. Finally, the designated core is released from wait to run the application. This completes the secure boot procedure.

The SE is also involved in the process of waking up from STOP mode. When a wakeup event is triggered, the SE boots first and checks if the SERAM is retained and continues the execution flow there. If not, then the SE will first load SERAM. The SERAM execution maps the wakeup event to the RTSS-HE core and promptly boots it. The retention of SERAM in the Secure Enclave or the SRAM (M55-HE TCM) in the RTSS-HE offers trade-off options between the leakage current and the wakeup time of the device.

The SE provides traditional security functions such as:

- Secure boot
- Secure device configuration
- HW Root-of-Trust (RoT)
- Signature validation
- Crypto operations
- Life cycle management
- Manage the OEM provisioning process and the Life Cycle State (LCS)
- Apply the system configuration settings to the security firewalls and security HW in the system

3.4.2 Cryptographic Services

The Secure Enclave (SE) supports a variety of Runtime Security and Cryptographic services that enable the OEM's application code to control security functions for the device and request cryptographic operations. These runtime services make use of IPC MHU's.

The Runtime Cryptographic services include the ability of the OEM application code to make requests for standard and device-specific cryptographic operations like:

- Validate the signature of images against the provisioned keys in the device
- Secure boot a core
- Get RNG values from hardware TRNG
- Crypto operations via an MBedTLS-based API: AES (128/192/256-bit keys), AEAD (GCM, CCM, CCM*), Stream ciphers (ChaCha20, ChaCha20-Poly1305), Hashing (SHA-1, SHA-224, SHA-256), MAC (AES-CMAC, Poly1305)
- Device Identity: read-only retrieval of factory-provisioned ECC public key
- Process Alif Semiconductor's firmware updates

3.5 Interconnect

The system interconnect provides the means of connecting bus masters (CPU cores, DMA controllers) to memory modules and peripherals. It is based on the Arm AMBA bus architecture utilizing a mix of AXI, AHB and APB buses.

The backbone of the device interconnect is based on an AXI4 bus, featuring multiple master and slave ports. The processing subsystems have their own local buses connected as masters to the main AXI bus. The memory blocks and the peripheral subsystems connect as slaves to the main AXI bus. Some peripherals (such as SDMMC and USB) also can act as bus masters and connect via both master and slave ports. The master ports serve their DMA controllers to transfer data without CPU intervention, while the slave ports are intended for accessing their registers.

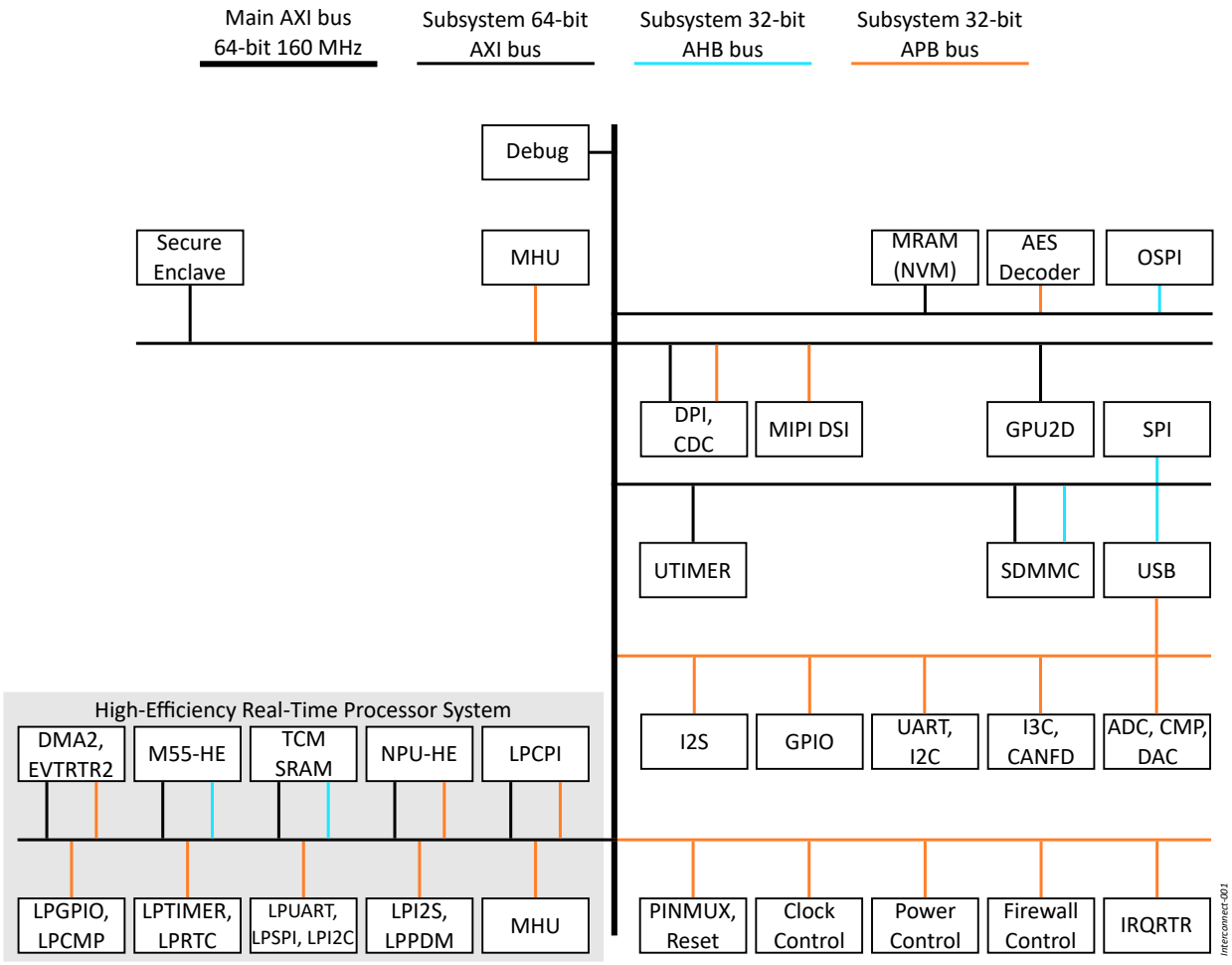
Each master and slave port connects to the main AXI bus through Firewall Components (FC). They enforce run-time configurable access rights policy and address translation. Transaction gating is based on master ID, transaction type (instruction or data fetch) and TrustZone-defined secure world context. The FC configuration settings are set by the SE during the secure boot process. The applications specify their desired access paths and address regions in a dedicated region of the on-chip Non-Volatile Memory (NVM), which is MRAM. The SE applies these settings during the device boot process.

The device interconnect supports the following main features:

- High-performance AXI4 bus protocol
- 64-bit wide read and write data paths
- 160 MHz bus clock frequency
- Burst-based transactions for optimizing bandwidth efficiency
- TrustZone aware
- Firewall controller and 14 firewall components to enforce secure policy constraining the bus master's access to the device resources
- Firewall security monitoring function raising an interrupt when unauthorized access is attempted

Figure 3-1 provides a high-level overview of the system interconnect implementation in the device.

Figure 3-1 Interconnect Overview



NOTE

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

3.6 Power Supply Management

The device has two operating regions that encapsulate top-level functions from a power consumption perspective:

- **Always-On (AON) Region**—a group of rudimentary functions that are always powered as long as a power source is connected to the VDD_MAIN pin.
- **High-Efficiency (HE) Region**—a group of compute, sensing, AI and high-speed connectivity functions designed to operate at the highest efficiency.

The device block diagram (see Figure 2-1) illustrates these two operating regions and the functions available within each of the regions.

A smart power management scheme named *ai*PM (autonomous intelligent Power Management) utilizes a hierarchy of multiple power domains, multiple internal voltage supplies, and multiple power modes to power on, in fine granularity, portions of the device only when they are needed based on use case, and off when not needed. Powering on and off portions of the device occurs automatically in hardware as required, but the power management policies are configured by software.

Multiple power domains—There are six independent power domains in the device, each one with a dedicated power controller that is coordinated by digital logic and software configuration for automatic transitions—from power-up to full GO mode, and all modes in between. This scheme achieves optimum power efficiency based on the dynamic power demand of the device at any given moment in time.

Multiple voltage supplies—There are internal device voltage supplies consisting of a series of Low Drop-Out (LDO) regulators and a dual-mode DC-to-DC buck converter (DC-DC) to generate 0.55 V, 0.8 V, and 1.8 V internal voltage rails that are automatically switched on and off as required for optimum performance and efficiency.

Multiple power modes—Below are top-level device modes listed from highest to lowest power consumption:

- RUN:
  - GO—M55-HE processing core operating up to its max frequency
  - READY—M55-HE processing core is powered on with its clock gated off, but peripherals can run
  - IDLE—M55-HE processing core is powered off, but some peripherals can run
- STANDBY—M55-HE processing core is powered off, but a few low-power peripherals can run
- STOP—Entire device is powered off except the AON Region where rudimentary low-power peripherals and wake-up sources are active, as well as optional retained SRAM blocks

3.6.1 Power Domains

The device Power Domains (PD) are managed by a Power Sequence Controller (PSC) and several Power Policy Units (PPU). The PSC is a state machine that monitors a fixed set of inputs and automatically acts to turn power on or off in power domains at the lower levels. PPUs take inputs from the PSC, inputs from the device condition status, and inputs from configuration settings from the application code, then PPUs act autonomously to turn on or off power to the domains, and PPUs also control domain clock sources. Thus, the operational processes of the PSC and PPUs automatically and dynamically achieve the best power consumption based on instantaneous power demand.

Figure 3-2 illustrates the power domains, control hierarchy, transition possibilities, and relevance to the two operating regions of the device. The power-up sequence of the shown regions and domains is:

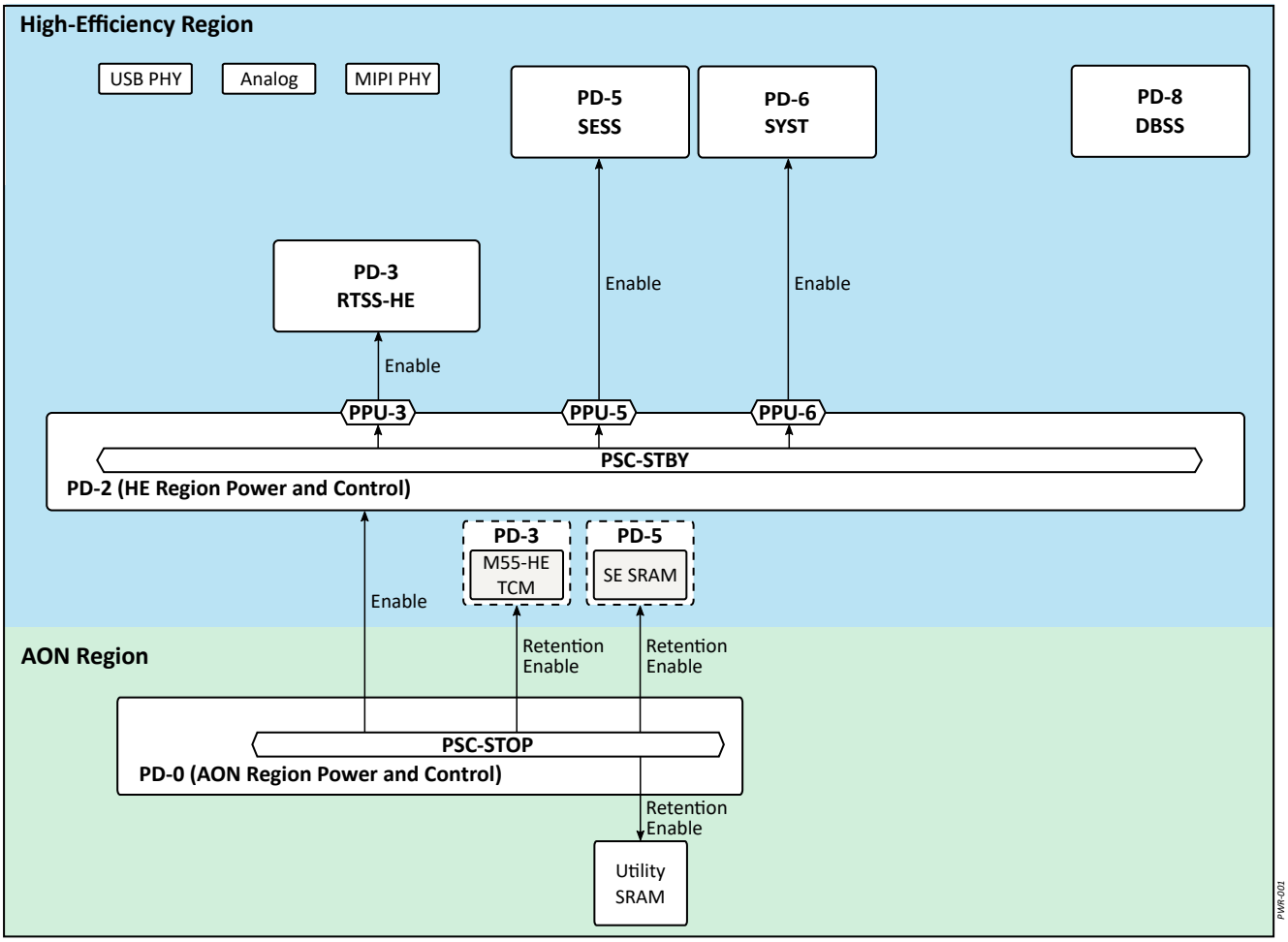
1. If VDD_MAIN is connected to a constant power source, the PD-0 domain and the AON Region are Always-On.

2. The PD-2 domain is first to power up.
3. The next order of powering up the domains depends on whether the device executes an initial boot (cold), or a wake up (warm).

PDs in each of the two device regions are defined as follows:

- AON Region
  - PD-0, AON power and control
- HE Region
  - PD-2, High Efficiency Region power and control
  - PD-3, Real Time Subsystem-High Efficiency (RTSS-HE)
  - PD-5, Secure Enclave Subsystem (SESS)
  - PD-6, Shared Peripherals / Shared System Resources (SYST)
  - PD-8, Debug Subsystem (DBSS)

Figure 3-2 Device Power Domain Hierarchy and Transitions



For more details about PDs power-up and transitions, see the device series-specific Hardware Reference Manual.

Table 3-1 illustrates which specific resources are available within each of the power domains, and how the power domains are related to the two operational regions.

Table 3-1 Device Resources per Power Domain

AON Region	High-Efficiency Region				
PD-0	PD-2	PD-3	PD-5	PD-6	PD-8
PSC-STOP	PPU-3	M55-HE	SE CPU	GPIO	SWD
LPTIMER	PPU-5	M55-HE L1 Cache	SE SRAM (SERAM)	MRAM	
LPCMP	PPU-6	M55-HE TCM (SRAM0, SRAM1)	Security Unit	USB	
LPGPIO	PINMUX	NPU-HE	System Controls	CANFD/CAN-CNT	
LPRTC	LPUART	LPCPI	SEUART	GPU2D	
BOD	LPI2C	LPPDM		DSI	
POR	EWIC	LPI2S		DPI/CDC	
VTOR	IRQRTR	LPSPI		OSPI/AES	
LFRC	JTAG	DMA2		SDMMC/SDIO	
LFXO	HFRC	MHU		UTIMER	
VBAT	HFXO	WDT_HE		I3C	
ANA	PLL	EVTRTR2		I2C	
STOP_MODE	PPU-HE	M55HE_CFG		SPI	
LPGPIO_CTRL	CGU			I2S	
	AON			UART	
Optional SRAM Retention:	CLKCTL_SYS			ADC12	
• Utility SRAM	Host Debug			ADC24	
• M55-HE TCM (SRAM0, SRAM1)				DAC12	
• SE SRAM (SERAM)				CMP	
				TSENS	
				VREF	
				CLKCTL_PER_MST	
				CLKCTL_PER_SLV	
				CRC	
				AXI Bus	

3.6.2 Voltage Supplies

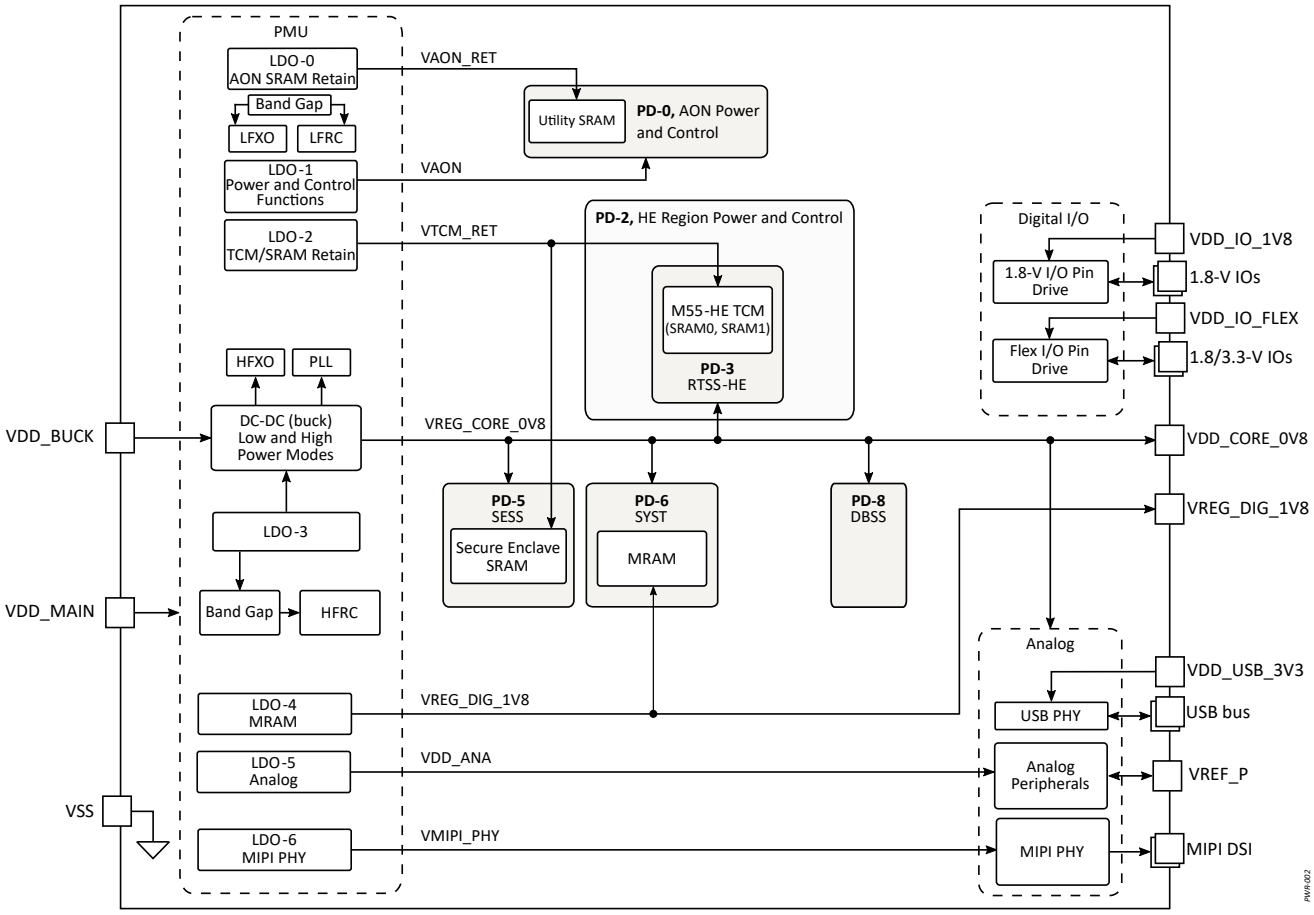
The device power domains are supplied with voltages from several internal supply sources. Power domains that feature SRAM retention have dual voltage supplies.

The device voltage supply and distribution system is architected to:

- Implement the *ai*PM strategy to dynamically power on only what is needed within the most optimum region of the device
- Minimize leakage current in STOP and STANDBY modes
- Rapidly exit low power modes upon a wake-up event
- Minimize dynamic current consumption in GO mode

Figure 3-3 illustrates the voltage distribution inside the device including highly efficient LDO regulators and a DC-DC buck converter. Very few external power sources are required because of the power management capability within the device to generate multiple voltage rails and to correctly sequence the supplies during power up and power down.

Figure 3-3 Device Voltage Distribution



For more information about power supply voltage ranges and general operating conditions, see Section 5.2.1 General Operating Conditions.

Table 3-2 presents power supply signals and provides descriptions to their functions.

Table 3-2 Power Supply Signal Descriptions

Signal Name	Pin Name	Type	Description
VDD_MAIN[7]	VDD_MAIN [1]	PWR	Main power supply
VDD_BUCK	VDD_BUCK	PWR	Internal DC-DC converter power input
VDD_USB_3V3	VDD_USB_3V3	PWR	USB power input
VDD_IO_FLEX	VDD_IO_FLEX	PWR	GPIO flex pads (1.8 V [3] - 3.3 V) power input
VDD_IO_1V8	VDD_IO_1V8	PWR	GPIO standard pads (1.8 V) power input
VREG_DIG_1V8	VREG_DIG_1V8 [4]	PWR	Internal 1.8 V regulator output
VDD_MIPI_0V8	VDD_MIPI_0V8	PWR	MIPI PHY power input
VDD_MIPI_1V8	VDD_MIPI_1V8	PWR	MIPI PHY power input (connect to VREG_MIPI_1V8)
VREG_MIPI_1V8	VREG_MIPI_1V8	PWR	Internal MIPI PHY 1.8 V power output
VDD_CORE_0V8	VDD_CORE_0V8	PWR	Main digital supply (connect to VREG_CORE_0V8)
VREG_CORE_0V8	VREG_CORE_0V8 [7]	PWR	Internal DC-DC converter power output
VDD_TRX_0V8	VDD_TRX_0V8	PWR	Analog power supply (connect to VREG_CORE_0V8)
VDD_SX_0V8	VDD_SX_0V8	PWR	Power supply for the HFXO, as well as the digital sections of PLL and Audio PLL (connect to VREG_CORE_0V8)
VDD_LNAPA_0V8	VDD_LNAPA_0V8	PWR	Internal supply for Analog circuitry (not driven by external off-chip circuitry)
VREG_AON	VREG_AON [5]	PWR	Internal voltage supply - output of internal Always-On 0.8 V LDO regulator
VREG_LP_1V8	VREG_LP_1V8 [6]	PWR	Internal voltage supply - output of internal low-power LDO regulator
VREF_P	VREF_P	A	External positive voltage reference input to chip or output from internal reference generator. Used for ADC12, ADC24, DAC12, and DAC6.
VSW	VSW	PWR	DC-DC converter switching output (connect to inductor)
VSS_BUCK	VSS_BUCK	GND	DC-DC converter ground
VSS_ANA	VSS_ANA	GND	Analog ground
VSS	VSS	GND	Digital ground

1. When an external reset supervisor device is used, and VDD_MAIN is less than 1.8 V, it is important that the supply voltage to the supervisor device does not dip during start-up and trigger the supervisor device.
2. BOR and BOD functions not supported below 1.9 V.
3. VDD_IO_FLEX should be connected to VDD_IO_1V8 when 1.8-V mode is used.
4. VREG_DIG_1V8 must be bypassed to ground through a 1-µF capacitor in series with a 10 Ω resistor.
5. VREG_AON must be bypassed to ground through a 1-µF capacitor in series with a 1.0 kΩ resistor.
6. VREG_LP_1V8 must be bypassed to ground through a 1-µF capacitor.
7. VREG_CORE_0V8 output voltage level should not be set below 825 mV at runtime by the user application code.

CAUTION

The decoupling for VREG_AON pin must be present on the PCB or otherwise the device may be at risk for damage.

It is possible to change the output voltage value of VREG_CORE_0V8 during runtime by the user application code. Correct device operation over full operating conditions cannot be expected if the output of VREG_CORE_0V8 is set below 825 mV.

NOTE

An external brownout supervisor must be connected to VDD_MAIN/VDD_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65 V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Refer to the Alif Application Note AAPN0040, *PCB Layout Guidelines for Ensemble E1C MCUs*, for more details and detailed information about power decoupling for all power pins.

For use of the device with external reference for VREF_P please contact an Alif representative.

For more information about power supply voltage ranges and general operating conditions, see Section 5.2.1 General Operating Conditions.

3.6.3 Power Modes

Using *ai*PM, this device provides significant flexibility to balance power, performance, and wake-up time per application use case. The device-level power modes described in Table 3-4 make use of the power domains and the voltage supplies, described in Section 5.2.1 General Operating Conditions, to achieve this balance. Within each power mode the clock speed and clock gating can be fine-tuned for each core and peripheral to reduce power consumption.

Table 3-3 CPU State Summary

CPU State	Description
RUN	When CPU core is running and executing code.
LIGHTSLEEP	When CPU core is clock-gated and quickly resumes on any NVIC interrupt.
DEEPSLEEP	When CPU core, CPU cache, TCM, and NVIC are clock-gated and resume on any IWIC interrupt.
OFF(1)	When CPU core is powered down and register context is lost.

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.

Table 3-4 Device Power Mode Summary

Device Power Mode	Sub-mode	Description	Wake-Up Peripherals
RUN	GO	RTSS-HE is in RUN state. See Table 3-3.	All
	READY	RTSS-HE is in LIGHT SLEEP state. See Table 3-3.	All
	IDLE	RTSS-HE is in OFF state. See Table 3-3.	All(1)
STANDBY	-	RTSS-HE and shared resources associated with PD-6 are powered down.	LPUART, LPI2C, plus STOP mode peripherals

Device Power Mode	Sub-mode	Description	Wake-Up Peripherals
STOP	-	RTSS-HE and shared resources associated with PD-6 and PD-2 are powered down. Few peripherals remain on with extremely low leakage.	LPTIMER, LPCMP, LPRTC, and LPGPIO

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.

For more details about specific power consumption and wake-up times per power mode, see Section 5.2.2 Device Power Modes.

3.6.4 Power Supply Supervisors

The device has integrated supervisory circuits for Brown-Out Reset (BOR), Brown-Out Detect (BOD), and Power-On-Reset (POR).

There is one POR circuit, VBAT_POR, which monitors the VDD_MAIN (AON Region) and keeps the entire device in reset during initial power ramp to the device.

The BOD circuit monitors the VDD_MAIN power supply and generates interrupts when the voltage falls below a programmable threshold. The BOD interrupt can be used as a wake-up source from STANDBY and from STOP low-power modes. For applications utilizing the BOD, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

The BOR circuit monitors the VDD_MAIN power supply and causes an immediate reset to the main SoC when the voltage falls below a programmable threshold. For applications utilizing the BOR, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

The POR circuit is described further in Section 3.7 Reset Management Overview.

Table 3-5 summarizes the power supply supervisory functions.

Table 3-5 Power Supply Supervisory Functions

Power Supply	Supervisor Type	Supervisory Function
VDD_MAIN	POR	Fixed threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains.
VDD_MAIN	BOR	Programmable threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains. For applications utilizing the BOR function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.
VDD_MAIN	BOD	Programmable threshold, triggers interrupts to the M55-HE and SE, and a request to DMA. For applications utilizing the BOD function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

3.7 Reset Management Overview

A reset brings the entire device (cold reset) or part of the device (warm reset) to a known good state.

The reset subsystem of the device is based on a Reset Controller (RSTC). The RSTC handles top-level reset conditions—VBAT_POR and software reset requests.

Figure 3-4 shows the main reset sources in the device.

Figure 3-4 Top-Level Reset Diagram

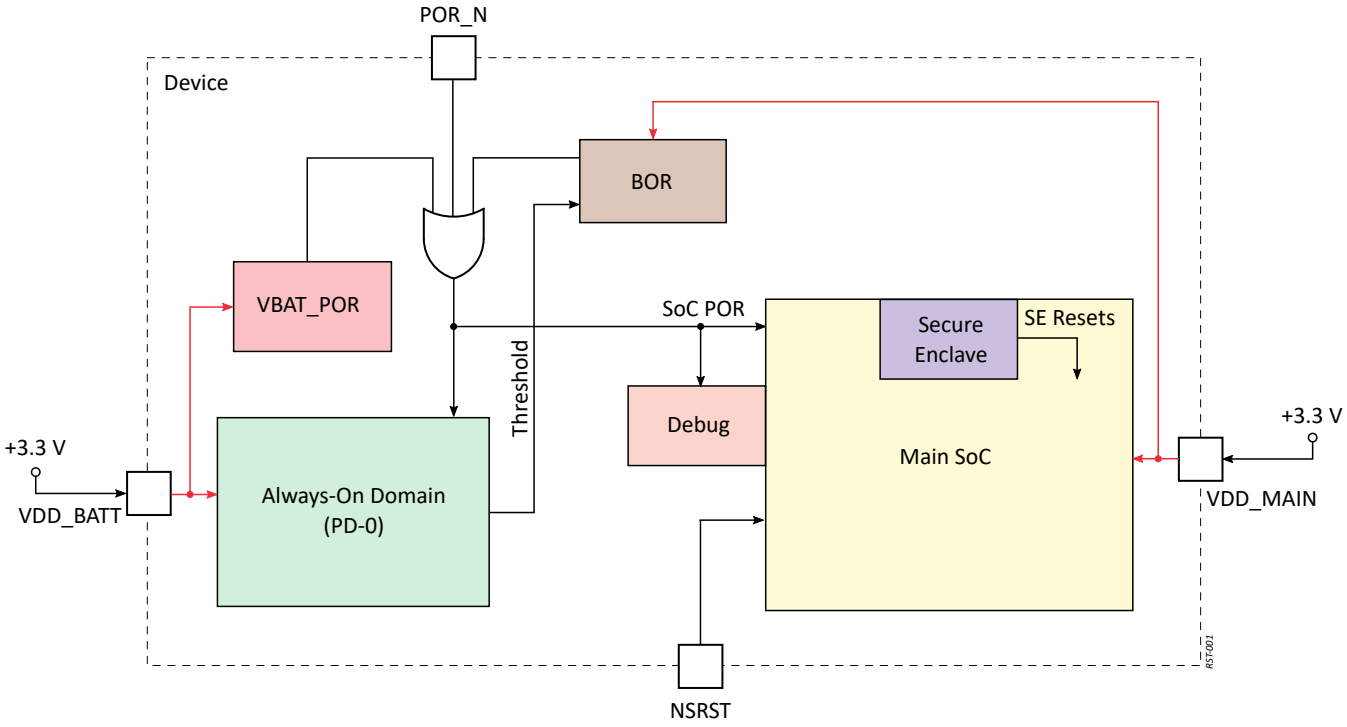


Table 3-6 lists the main reset sources along with their types and functions.

Table 3-6 Device Main Reset Sources

Reset Source	Hardware/Software	Description
POR_N pin (active-low)	HW	System cold reset pin. Asserting this pin is equivalent to turning the device power off. After POR_N is deasserted, the device completes a full power on cycle, which is equivalent to a cold start. No logic or memory retains its state.
NSRST pin (active-low)	HW	System warm reset pin. Typically, an external debugger asserts this reset pin. It resets all logic in the device except for PD-0 Always-On peripherals, debug logic, and the JTAG interface.
VBAT_POR monitor	HW	Fundamental POR. VBAT_POR keeps the entire device in reset during a power-on ramp-up until the device reaches the operational threshold.
BOR monitor	HW and SW	Brown-out reset. BOR assertion is equivalent to turning the device power off. After BOR is deasserted, the device completes a full power on cycle, which is equivalent to a cold start. For applications utilizing the BOR function, the minimum device operating voltage on VDD_MAIN is limited to 1.9 V.

Reset Source	Hardware/Software	Description
Secure Enclave Reset	SW	Warm reset by Secure Enclave. Initializes all logic except for PD-0 Always-On, the debug logic, and the JTAG interface.
SW_HE_RST	SW	High-efficiency subsystem (RTSS-HE) reset. Warm reset by Secure Enclave. RTSS-HE reset reasons are logged to RTSS_HE_RESET register.

Table 3-7 presents Reset signals and provides descriptions to their functions.

Table 3-7 Reset Signal Descriptions

Signal Name	Pin Name	Type	Description
NSRST	P2_2	I	JTAG reset (system reset) active low
POR_N	POR_N	I	Power-On-Reset (cold reset) active low

3.8 Clock Generation and Control

The device includes several clock domains, PLLs, clock dividers, clock multiplexers, oscillators.

The device clock sources are as follows:

- Low-Frequency Resistor-Capacitor (LFRC) oscillator—a low-power, internal RC oscillator powered by VDD_MAIN. This oscillator is used during the power-up sequence, with a typical clock frequency accuracy of 32.7 kHz ±4%.
- Low-Frequency crystal Oscillator (LFXO)—a low-power oscillator that is used with a high-accuracy 32.768 kHz external crystal. This oscillator is powered by VDD_MAIN. It is enabled at power-up and is the typical clock source for LPRTC. The LFXO oscillator input may optionally be configured in bypass mode for connection to an external 32.768 kHz clock source.
- High-Frequency Resistor-Capacitor (HFRC) oscillator—a low-power internal RC oscillator that generates 76.8 MHz. When the LFXO clock source is available, the HFRC oscillator can be trimmed to reach an accuracy of ±2% or better over temperature. The HFRC oscillator is available in all power modes except for STOP mode. This oscillator is used during power-up for rapid initialization and fast start-up.
- High-Frequency crystal Oscillator (HFXO)—a power-optimized oscillator that is used with an external crystal with a frequency of 38.4 MHz. This oscillator is enabled by software after initial device configuration and is typically the source clock for the PLL. The HFXO oscillator input may optionally be configured in bypass mode for connection to an external high-speed clock source/oscillator.

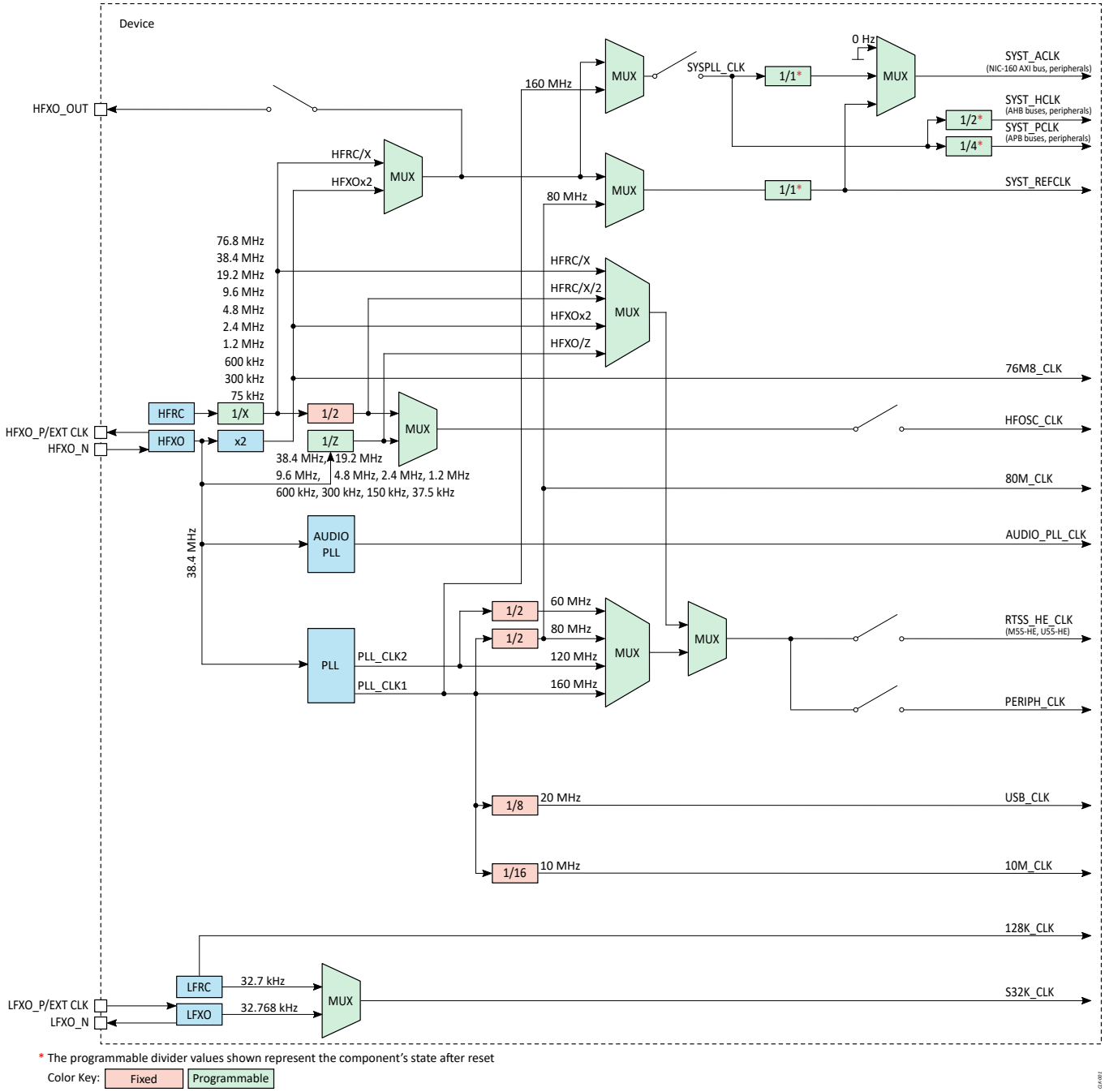
CAUTION

It is not recommended to operate the device without an HFXO or external clock source/oscillator connected to the device. Although the internal clocks can be sourced from the HFRC, an HFXO clock source is required for a proper device startup and when using peripherals requiring a high-accuracy clock (USB, etc.).

- System PLL (Phase-Locked Loop)—a power-optimized, fast-locking clock multiplier with fractional mode. It has a single clock output used to supply most of the device subsystems, modules, and interconnects.
- Audio PLL—a power-optimized, fast-locking clock multiplier with fractional mode. It has a single clock output used to clock the I2S and PDM audio peripherals.

Figure 3-5 provides a high-level overview of the clocking scheme implementation in the device.

Figure 3-5 Device Clocking Scheme Overview



NOTE

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

Table 3-8 presents clock interface signals and provides descriptions to their functions.

Table 3-8 Clock Signal Descriptions

Signal Name	Pin Name	Type	Description
HFXO_OUT_A	P4_2	O	High-frequency clock output to external devices
HFXO_OUT_B	P5_2	O	High-frequency clock output to external devices
HFXO_P	HFXO_P	I	High-frequency oscillator input
HFXO_N	HFXO_N	O	High-frequency oscillator output
LFXO_P	LFXO_P	I	Low-frequency oscillator input
LFXO_N	LFXO_N	O	Low-frequency oscillator output

3.9 Signal Multiplexing and I/O Buffer Configuration

3.9.1 Signal Multiplexing

The device offers a sophisticated signal-to-pin multiplexing scheme. Each I/O pin may be assigned to one of up to eight peripheral signals, and vice versa, a peripheral signal may be routed to up to four I/O pins. This assignment is pseudo-static and must be performed once during boot time.

The multiplexed pins are divided into 8-pin groups, also referred to as 'ports'. A pin identifier 'Pn_i' may be used, where *n* is the port number and *i* is the pin number within that port. A pin may be referenced also with the GPIO peripheral's signal name 'GPIOn_i' because it shares the same numbering convention. For more information on the GPIO peripheral, see Section 3.15 General-Purpose Input/Output Module.

MIPI-DSI, USB PHY pins, and power and ground pins have fixed functions and cannot be multiplexed.

Figure 3-6 shows the P0_0 multiplexing as an example. The Pn_i[PINMUX] register bitfield, where n = i = 0, selects a peripheral signal to be available on P0_0. The multiplexer switches three signals at a time: IN, OUT, and OEN (output enable). OEN could be dynamically driven by the peripheral, for example by the I2C which needs to change the Data pin direction very frequently. For many other peripherals OEN could be static, and for GPIO it is programmable via its Data Direction register. The analog peripherals are not multiplexed between themselves and all three can read P0_0 when [PINMUX] = 7. For more information on configuration registers, refer to the corresponding device series-specific Hardware Reference Manual.

Figure 3-6 I/O Signal Multiplexing (P0_0 Example)

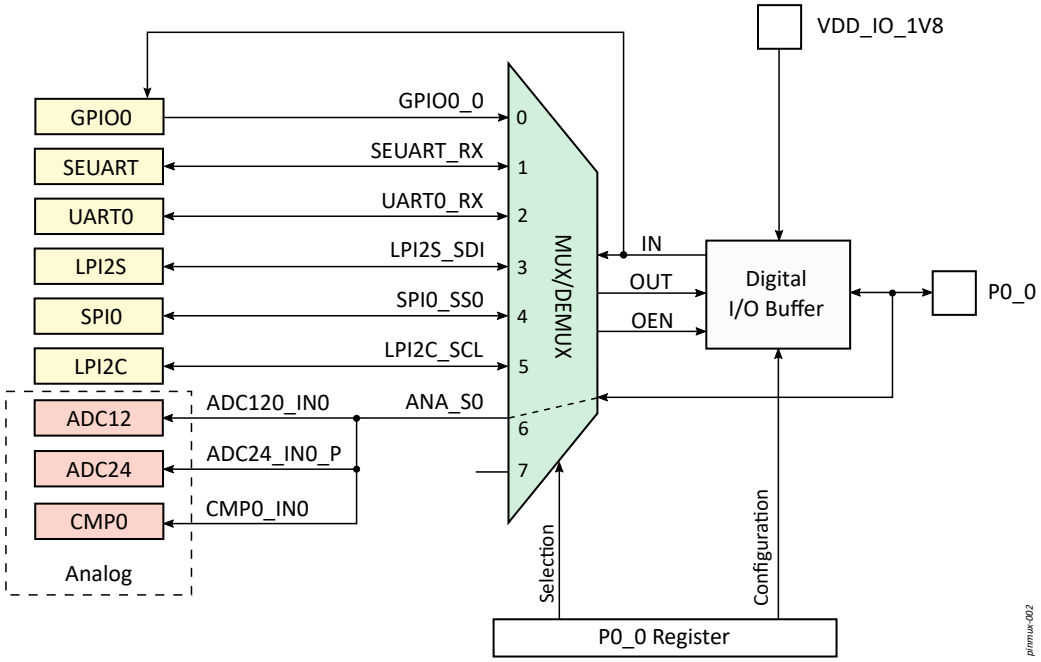
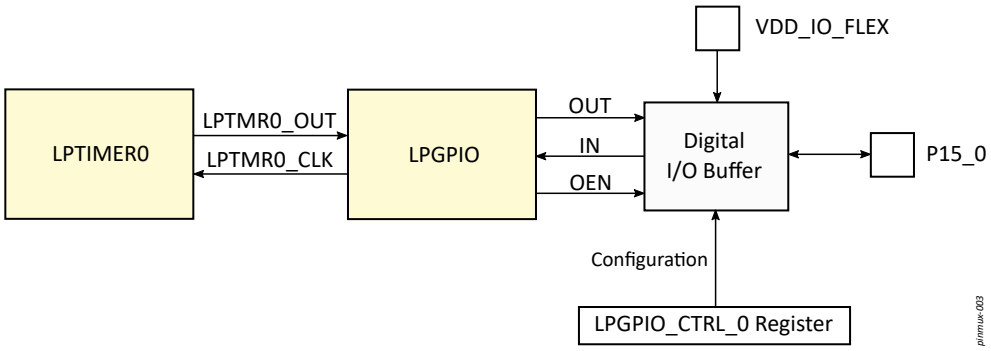


Figure 3-7 shows the LPGPIO pin sharing. Because Port 15 is located in the Always-On domain, here pin sharing is achieved differently. That is, there is no multiplexing as such. In this example, LPTIMER0 gets access to P15_0 via the LPGPIO module. LPGPIO controls the pin direction depending on the value written to its Data Direction register.

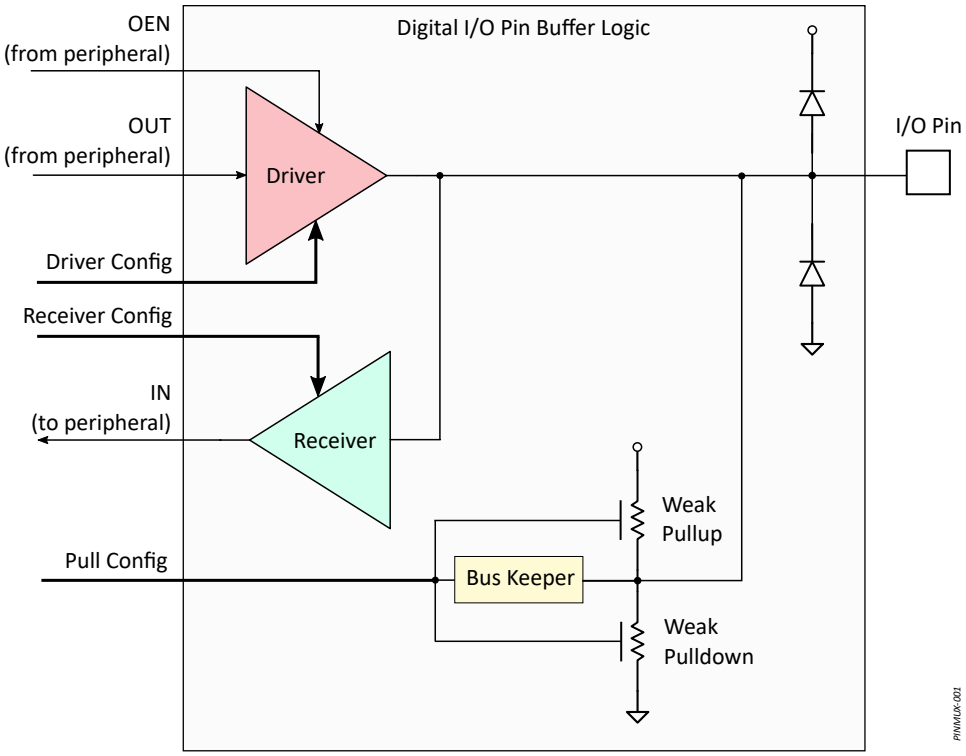
Figure 3-7 LPGPIO/LPTIMER Pin Sharing (P15_0 Example)



3.9.2 I/O Buffer Configuration

Figure 3-8 shows a top-level block diagram of a digital I/O buffer module. I/O buffer consists of configurable output buffer (driver), input buffer (receiver), pull-up/pull-down block, and protective diodes.

Figure 3-8 I/O Buffer Block Diagram



The I/O buffer has the following main features:

- Configurable direction (input, output or both)
- Selectable driver-disabled state:
  - No pull (Hi-Z, floating)
  - Weak pull-up
  - Weak pull-down
  - Bus keeper (keeps the last state seen on the pin)
- Configurable drive strength
- Configurable slew rate
- Output driver can be open drain or push-pull type
- Input may have a Schmitt trigger enabled which adds hysteresis to signal transitions
- Dedicated power rails:
  - VDD_IO_FLEX for the 1.8-V/3.3-V pins (GPIOV_[0], GPIO1[3-7])
  - VDD_IO_1V8 for the 1.8-V pins

The Pn_i registers contain bitfields controlling the following parameters:

- Driver type—[DRV] (open drain or push-pull)
- Output drive strength—[E] (2 mA, 4 mA, 8 mA, or 12 mA)
- Driver disabled state—[P] (Hi-Z, Pull-up, Pull-down, or Bus Keeper)
- Slew rate—[SR] (slow [half-speed] or fast)
- Schmitt trigger enable—[SMT]
- Receiver enable—[REN]

Similar I/O buffer controls exist also for Port 15 in the LPGPIO_CTRL_n[DRIVER] and LPGPIO_CTRL_n [RECEIVER] register bitfields.

NOTE

For more information on I/O buffer configuration registers, refer to sub-sections *PINMUX Registers Guide* and *LPGPIO_CTRL Registers Guide* in Section *Signal Multiplexing and I/O Buffer Configuration* of the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

3.10 Inter-Processor Communication

3.10.1 MHU Overview

The Message Handling Unit (MHU) provides point-to-point communication between the Secure Enclave processor and the Real-Time processor (M55-HE). The MHU is an interrupt-based communication between two processing entities.

The device includes up to 4 unidirectional MHU modules.

Each of the MHU modules supports the following main features:

- Two memory mapped register frames—Sender and Receiver
- Unidirectional communication interface
- Read and write access—32-bit word aligned
- Dual transport channels
- Different transport protocols—Doorbell, Single-Word transfer, and Multi-Word
- Dedicated interrupt lines for the Sender and Receiver

The software responsibilities are:

- To request the Receiver to be powered
- To ensure that the Sender remains powered until the transfer has been finished
- To use Ready to Send protocol to send the transfer

Each processor entity includes only one of the Sender or Receiver frame. To ensure a bi-directional (full-duplex) communication between the entities, two MHUs with reversed Sender and Receiver parts are implemented.

3.11 Memories

3.11.1 MRAM Overview

The MRAM module is a type of non-volatile random-access memory which stores information in magnetic elements.

The MRAM operates at 26.67 MHz clock frequency over 128-bit data bus. The 128-bit (16-byte) word represents the minimum sector size for the MRAM. The smaller granularity offers much better efficiency compared to the legacy flash memory modules. It takes flash memories longer to be programmed/erased due to their much larger sector sizes.

The MRAM module implements a state machine controlling the erase and programming sequence of 16-byte memory blocks. This operation is transparent to the CPU core.

The MRAM controller implements read cache and write buffer mechanism that enables the concurrent read and write operations. This greatly benefits the implementation of multi-core applications that are not

required to coordinate the access to the MRAM. Up to four bus masters can originate concurrent write operations, while the number of concurrent read operations is not limited.

The MRAM supports the following main features:

- Size up to 1.9MB
- High endurance (more than 100 000 erase cycles)
- More than 10 years data retention (at 125 °C junction temperature)
- 16 ECC bits for each 128-bit data word
- 2× 16 bytes read cache to accelerate access to frequently used data and non-16-byte aligned read requests
- Built-in state machine controlling 16-byte program/erase cycle (no need of driver)
- Concurrent write (up to four bus masters) and read operations (no need for synchronization between them)
- DMA write operation with up to 128 bytes in each DMA write cycle data payload

3.11.2 SRAM Overview

The device contains the following types of on-chip SRAM memories:

- User SRAM available for all bus masters:
  - M55-HE TCM: SRAM0 (M55-HE ITCM) and SRAM1 (M55-HE DTCM), with optional retention
- Processor cache memories:
  - M55-HE Level 1 cache
- Utility SRAM
  - Located in Always-On domain

The TCM is an SRAM block providing high-bandwidth and low latency access. The TCM is primarily used by the M55-HE core. Alternatively, it can be shared with other bus masters in the device.

The cache memory is a high-performance SRAM accelerating the CPU access to frequently used instructions and data. The M55-HE processor has Level 1 cache memories dedicated to the M55-HE core.

The device includes the following quantities of SRAM with their performance characteristics:

- User SRAM available to all bus masters:
  - Up to 2MB:
    - Zero wait state read access
    - Up to 0.5MB SRAM0 (M55-HE ITCM), with optional retention
    - Up to 1.5MB SRAM1 (M55-HE DTCM)
- Real-time processor (M55-HE) cache memories:
  - Level 1 Cache: 16KB Instruction and 16KB Data
- Utility SRAM:
  - 4KB in power domain PD-0
  - 100 MHz read/write access
- The contents of SRAM0 and SRAM1 may be optionally retained for context saving during low power modes with the following retention current consumption at 3.3 V in SRAM increments of:
  - 64KB (450 nA), 128KB (900 nA), 256KB (1.8 µA), 512KB (3.6 µA), 1MB (7.2 µA), 2MB (14.4 µA)

NOTE

User SRAM size and availability is device part number dependent. For more information on SRAM blocks enabled for each part number and their sizes, see Section 7 Ordering Information.

3.11.3 TCM Overview

The Tightly Coupled Memory (TCM) is a high-bandwidth and low latency memory. The TCM enables the Cortex-M55 core to perform vector operations with high efficiency and process interrupts with minimum latency. The TCM access time is a single clock cycle with no wait states for reads. The TCM interface is based on Harvard architecture—it has one instruction memory (ITCM0) bus and four data memory (DTCM0/1/2/3) buses, all 32-bit wide.

The M55-HE core can use the ITCM for storing data and can fetch instructions out of the DTCM. In this scenario, the TCM access time is slower and vector operations are not supported.

The Cortex-M55 core has the following TCM configurations:

- M55-HE:
  - Up to 512KB of ITCM and up to 4 × 384KB of DTCM (total of up to 2048KB)
  - 1 × 32-bit ITCM and 4 × 32-bit DTCM memory buses
  - Single-cycle read access at 160 MHz
  - Concurrent share of TCM with the other processing entities via AHB slave port
  - Optional content retention

3.11.4 External Memory Expansion Options

The device provides two options to expand the memory using external devices:

- 1× SDMMC interface
- 1× OSPI interface

The SDMMC interface can be used to access embedded or external memory cards with clock frequency up to 50 MHz. The data bus is up to 8 bits wide. This external memory interface is suitable for expanding the bulk data storage capacity in the form of an external flash-based file system. The SDMMC interface supports legacy 4-bit cards as well.

The OSPI interface can be used to access external flash memory devices. The OSPI supports Double Data Rate (DDR) mode transferring 8-bit data on both edges of the clock signal. The maximum clock frequency is up to 80 MHz, delivering raw DDR bandwidth of up to 160 MB/s.

The OSPI interface could access the memory in two modes—directly (through register read/write operations) or indirectly (through memory-mapped operations). The indirect access supports eXecute-in-Place (XIP) mode which translates the instruction fetch operations to proper address and data read transactions. This way, the external memory devices expand the available non-volatile memory.

The OSPI interface supports legacy Single, Dual, Quad, or Octal SPI flash memory devices.

The OSPI interface also supports the HyperBus protocol in direct and indirect modes. This enables the integration of external Static or Pseudo-Static RAM devices. See operation limitations in Section 3.17.1 Cryptographic OSPI Overview.

The OSPI interface can be attached to a flash or SRAM devices based on the application needs.

The device includes an AES decoder which is implemented in hardware and enables on-the-fly decoding of the external memory content. This allows protecting the OSPI code or the confidentiality of the data stored

in external devices. The decoder effectively adds no latency while maintaining the overall external memory interface bandwidth.

3.11.5 Memory Mapping

Refer to the device series-specific Hardware Reference Manual for details on the memory mapping.

3.12 Interrupts and Events Management

3.12.1 NVIC Overview

The Nested Vectored Interrupt Controller (NVIC) resides in the M55-HE processor, and it is closely integrated with the Cortex-M55 core to achieve low-latency interrupt processing.

The NVIC module supports the following main features:

- Maintaining the current execution priority of the Cortex-M55 processor
- Maintaining the pending and active status of all exceptions that are supported
- Invoking preemption when a pending exception has priority
- Providing wake-up signals to wake up the Cortex-M55 processor from deep sleep mode
- Providing support to the Internal Wakeup Interrupt Controller (IWIC) and External Wakeup Interrupt Controller (EWIC)
- Providing priority and exception information to other processor components
- 480 external interrupts, with 256 priority levels per interrupt

3.12.2 IRQRTR Overview

The shared Interrupt Router (IRQRTR) is intended to route interrupt signals from the device peripherals to all processing entities. It has an input port wired to the interrupt sources and two output ports connected to the Secure Enclave and the Real-Time Processing (M55-HE) interrupt controller.

The router configuration registers define which interrupt sources are enabled and their destination output ports. Once configured, the router can be locked fully or partially so that further changes can be restricted.

The access to the IRQRTR configuration may be constrained based on the device security policy. In this case, the interrupt routing can be indirectly setup by service call to the Secure Enclave.

The IRQRTR supports the following main features:

- Manages up to 427 shared interrupts
- Configures routing of the interrupt signals to up to four processing entities
- Supports configuration access lockdown
- Reports tamper interrupts to the Secure Enclave

3.12.3 EVTRTR Overview

The device integrates a large number of peripherals that can generate events indicating changes in their state, receiving of data or completion of an operation. The Event Router (EVTRTR) is a module that can associate an event originated by one peripheral with an action executed by another.

The function of the EVTRTR is similar to the shared Interrupt Router (IRQRTR), which targets an interrupt controller and ultimately a CPU core. Unlike the IRQRTR, the EVTRTR is connecting the event signal to a peripheral that executes an action without involving any CPU core.

Modules generating such event signals include: GPIO, UTIMER, I2C, SPI, UART, and others. The EVTRTR passes the signals through edge-detection circuits and gating logic before routing them to specific targets.

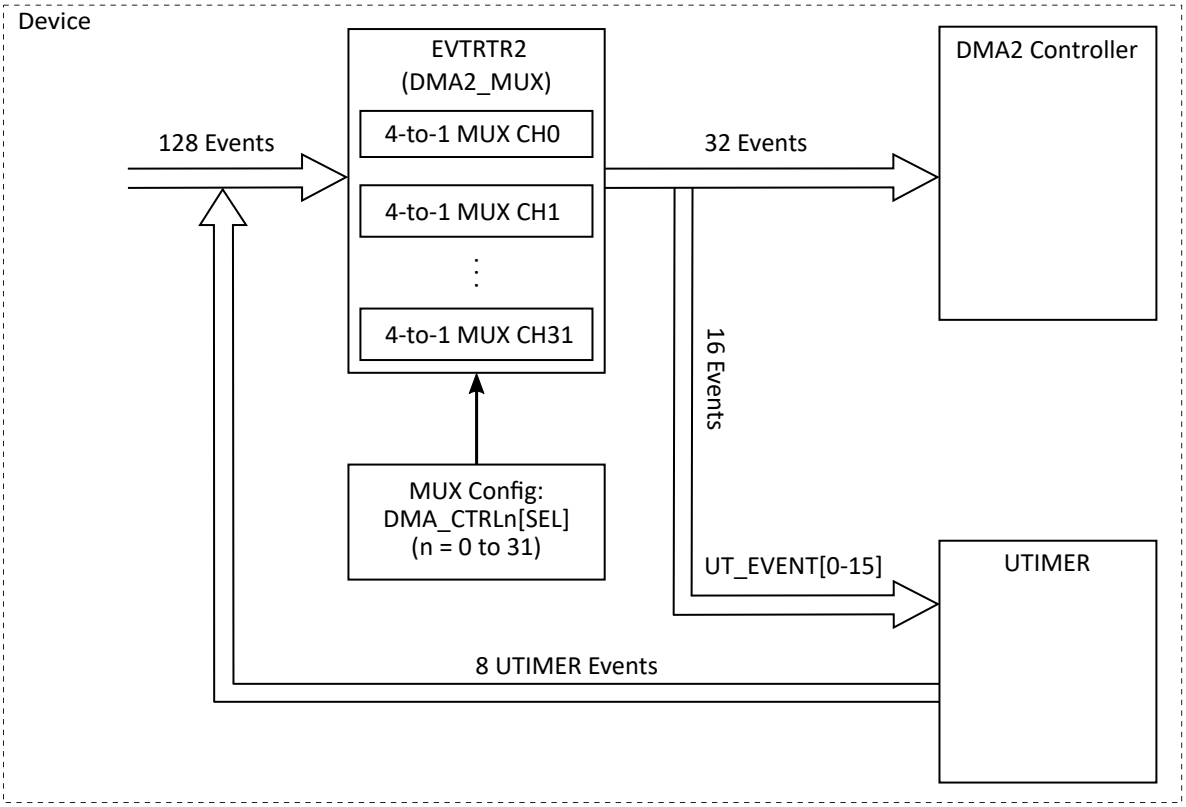
The device includes one Event Router: EVTRTR2, dedicated to DMA2 controller and UTIMER.

EVTRTR2 provides the following main features:

- Software generated events
- Zero wait state for event routing between peripherals in the same clock domain
- Automatic synchronization of events and triggers between peripherals in different clock domains
- DMA channel enable, handshake status and type selection

Figure 3-9 provides a high-level overview of the EVTRTR implementation in the device.

Figure 3-9 EVTRTR Overview



EVTRTR2 is also referred to as DMA2_MUX and expands the available 32 inputs of DMA2 by exposing the DMA channels to 128 different peripheral events via 32 × 4-to-1 multiplexers. The first 16 multiplexed DMA2 requests are also routed as input triggers to the Universal Timer (UTIMER). This mechanism enables the implementation of complex state machines involving the use of peripheral or time-based events that trigger data transfers and/or timer triggers.

3.13 DMA Management

3.13.1 DMA Architecture Overview

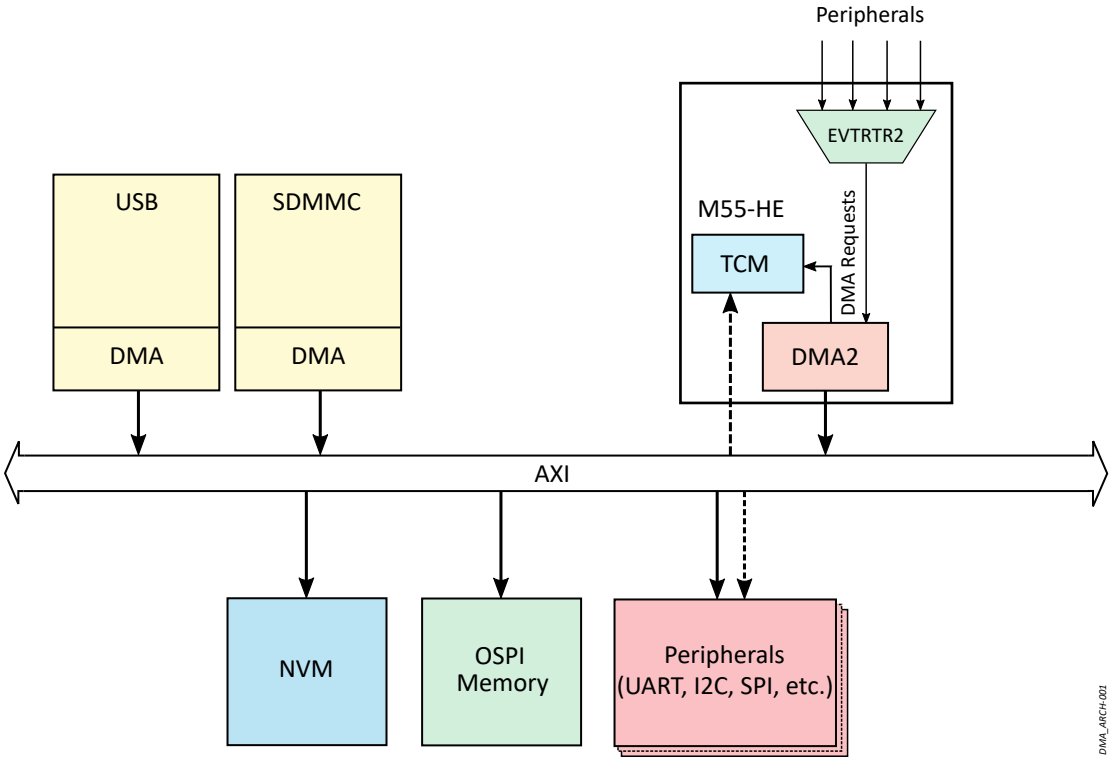
The device features Direct Memory Access (DMA) controllers to offload the CPUs from repeated data transfer tasks. The device has the following DMA controllers:

- USB embedded DMA controller
- SDMMC embedded DMA controller
- DMA2: Dedicated to the RTSS-HE subsystem
  - DMA2 can move data from/to the following peripherals: Low Power (LP) peripherals (such as LPUART, LPSPI, etc.), UART, SPI, OSPI, ADC, CANFD, I2S, I2C, and I3C.

- BOD, LPTIMER, UTIMER, CMP, LPCMP, LPCAM_VSYNC, LPCAM_HSYNC, CDC_VSYNC, CDC_HSYNC, GPIO1, GPIO3, GPIO4, GPIO7, and LPGPIO I/O transitions can trigger DMA requests.

Figure 3-10 gives a high-level overview of the DMA architecture in the device.

Figure 3-10 DMA Architecture



The high-speed interface peripherals (USB and SDMMC) have their own, embedded DMA controllers. They are optimized for the specific needs of these interfaces.

DMA2 is a general-purpose, programmable, multi-channel, and TrustZone-aware DMA controller (DMAC). It has 32 inputs for accepting DMA requests from various device peripherals and triggers (for example, UART Tx and Rx, ADC conversion done, etc). The Event Router positioned in front of the DMA2 controller provides support for DMA handshaking between peripherals and DMAC. Additionally, EVTRTR2 provides 32 × 4-to-1 programmable multiplexers, which expose the 32 DMA2 inputs to 128 possible DMA requests from peripherals, thus providing an increased flexibility. The DMA2 controller supports 8 internal data channels (FIFOs). All channels can perform independently programmed transactions including different data lengths, source and destination addresses, single or burst transfers.

DMA2 is assigned to the M55-HE CPU core. DMA2 resides in the M55-HE domain and shares AXI-bus Stream IDs (and security policy). The DMA2 request interface can generate individual interrupt requests, attached locally to the M55-HE core.

3.13.2 DMA Controllers Overview

The device includes one general-purpose DMA Controller (DMAC):

- DMA2, dedicated to the RTSS-HE

DMAC supports the following main features:

- Flexible instruction set for programming DMA transfers
- Transfer types:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Scatter-gather
- 32 peripheral request interfaces (DMA_Req/DMA_Ack)
- 8 DMA channels (VFIFOs)
- Flagging of various DMA events using 33 interrupt signals
  - 32 interrupts, one per DMA request interface
  - One data abort interrupt
- Dual slave interfaces, secure and non-secure, for accessing registers
- Programmable security state for each DMA channel
- Arm TrustZone technology
- 4 active AXI read transactions
- 4 active AXI write transactions
- 32 deep internal data buffer (MFIFO)
- 4 lines in the instruction cache with 8 words in a line
- 8 deep read instruction queue
- 8 deep write instruction queue
- Request acceptance capability of a peripheral request interface—4 requests

3.14 Timers and Counters

3.14.1 LPTIMER Overview

The 32-bit Low-Power Timer (LPTIMER) module counts down from a programmed value and generates an interrupt when the count reaches zero. Two events can cause the timer to load the initial value from which it counts down. The first event is when the timer is enabled after being reset or disabled, and the second event is when the timer count reaches zero.

The device includes up to two independent LPTIMER modules (“channels”), accessible through a single bus.

Each LPTIMER module supports the following main features:

- 32-bit down counter
- Free-running and user-defined count modes
- Asynchronous event counting
- Individual toggle output with PWM capability
- Individual interrupt output
- Independent clock input that can be connected either to internal clocks or to an external clock source
- LPTIMER1 can be concatenated with LPTIMER0 to form up to a 64-bit timer
- The LPTIMER interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPTIMER. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-9 presents LPTIMER interface signals and provides descriptions to their functions.

Table 3-9 LPTIMER Signal Descriptions

Signal Name	Pin Name	Type	Description
LPTIMER0			
LPTMR0_CLK_IO	P15_0	IO	LPTIMER0_CLK: LPTIMR0 input clock from pin.
			LPTIMER0_OUT: LPTIMER0 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.
LPTIMER1			
LPTMR1_CLK_IO	P15_1	IO	LPTIMER1_CLK: LPTIMR1 input clock from pin.
			LPTIMER1_OUT: LPTIMER1 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled.

3.14.2 UTIMER Overview

The 32-bit high-resolution Universal Timer (UTIMER) typically serves as a standard signal timing generator and a pulse counter. In addition, the UTIMER can also be used to implement a quadrature encoder interface and serve as a Quadrature Encoder Counter (QEC).

The device includes up to four independent QEC-enabled UTIMER modules (“channels”): Channel 0 (UTIMER0) to Channel 3 (UTIMER3).

In measurement mode, each UTIMER channel can capture the timing of internal events or external signal pulse edges.

In counting mode, each channel can serve as a multifunctional counter with two inputs that can be configured to support different counting modes and count external pulses, internal events, or decode quadrature encoder pulse sequences. The input signals are passed through a digital filter to improve the noise immunity of the circuit. The count direction can be configured to depend on the phase difference between two signals (quadrature encoding) or on the level of one of them (pulse and direction encoding). Alternatively, one of the signals can be configured to increment and the other to decrement the timer counter values.

As a signal generator, each UTIMER channel can be configured to produce PWM outputs with independent or complementary polarity and has the following main characteristics:

- Outputs configurable option to automatically insert dead-time suitable for power stages with asymmetric switching characteristics
- Multiple channels can be synchronized to drive three-phase inverters with variety of modulation schemes
- Driving up to 4 three-phase motors at once

Each UTIMER channel supports the following main features:

- Clocked at high-resolution, up to 160 MHz clock with 6.25 ns accuracy when generating a PWM output or when measuring input signal timing characteristics
- Dedicated digital inputs configurable as external synchronization sources or as fault signals that trigger automatic shut-off of the output drivers
- 32-bit wide counters and compare registers
- Double-buffered compare registers to support update of PWM duty cycle to occur upon several events, including at the middle or at the end of a PWM period. When buffer operation is enabled, it can be configured to use single or double stage.
- Up to 2 high-resolution PWM outputs with independent or complimentary polarity
- Support of capturing events placed closely together when the channel is configured as a pulse counter
- Capture and compare modes
- Compare registers dedicated to ADC synchronization—on a match they trigger ADC conversion, thus avoiding a power stage switching noise
- 8 interrupt events—some can be shared among channels to enable the implementation of complex state machines that can operate in a deterministic manner
- Configurable to use two I/O pins as inputs and to drive the two I/O pins
- Decoding quadrature encoder pulse sequence
- Counting in pulse/direction or increment/decrement modes
- Measurement of pulse width, period, or duty cycle
- Digital filter on the input signals for up to 32 peripheral clock cycles
- Generation of interrupts on two compare/match events

Table 3-10 presents UTIMER interface signals and provides descriptions to their functions.

Table 3-10 UTIMER Signal Descriptions

Signal Name	Pin Name	Type	Description
UTIMER0 A/B/C			
UT0_T0_A	P4_0	IO	UTIMER0 input event on channel A / output to driver A
UT0_T0_B	P6_0		
UT0_T0_C	P8_0		
UT0_T1_A	P4_1	IO	UTIMER0 input event on channel B / output to driver B
UT0_T1_B	P6_1		
UT0_T1_C	P8_1		
UTIMER1 A/B/C			
UT1_T0_A	P4_2	IO	UTIMER1 input event on channel A / output to driver A
UT1_T0_B	P6_2		
UT1_T0_C	P8_2		
UT1_T1_A	P4_3	IO	UTIMER1 input event on channel B / output to driver B
UT1_T1_B	P6_3		
UT1_T1_C	P8_3		
UTIMER2 A/B/C			
UT2_T0_A	P4_4	IO	UTIMER2 input event on channel A / output to driver A
UT2_T0_B	P6_4		
UT2_T0_C	P8_4		
UT2_T1_A	P4_5	IO	UTIMER2 input event on channel B / output to driver B
UT2_T1_B	P6_5		
UT2_T1_C	P8_5		
UTIMER3 A/B/C			

Signal Name	Pin Name	Type	Description
UT3_T0_A	P4_6	IO	UTIMER3 input event on channel A / output to driver A
UT3_T0_B	P6_6		
UT3_T0_C	P8_6		
UT3_T1_A	P4_7	IO	UTIMER3 input event on channel B / output to driver B
UT3_T1_B	P6_7		
UT3_T1_C	P8_7		

Table 3-11 presents UTIMER common interface signals and provides descriptions to their functions.

Table 3-11 UTIMER Common Signal Descriptions

Signal Name	Pin Name	Type	Description
Common A/B			
FAULT0_A	P0_4	I	Fault signal 0. Used to trigger automatic shut-off of the output drivers.
FAULT0_B	P2_4		
FAULT1_A	P0_5	I	Fault signal 1. Used to trigger automatic shut-off of the output drivers.
FAULT1_B	P2_5		
FAULT2_A	P0_6	I	Fault signal 2. Used to trigger automatic shut-off of the output drivers.
FAULT2_B	P2_6		
FAULT3_A	P0_7	I	Fault signal 3. Used to trigger automatic shut-off of the output drivers.
FAULT3_B	P2_7		

3.14.3 WDT_RTSS Overview

The Real-Time Subsystem Watchdog Timer module, hereinafter referred to as WDT_RTSS, is a timer based on a 32-bit down-counter. The basic function of the WDT_RTSS is to count for a fixed period, during which it expects to be serviced by the system, indicating normal operation. The WDT_RTSS provides a mechanism to detect errant system behavior and recover from an unknown state by causing reset of the system if the count period elapses without intervention.

The device includes one WDT_RTSS module:

- WDT_HE: Dedicated to the Arm Cortex-M55 High-Efficiency (M55-HE) processor

The WDT_RTSS module supports the following main features:

- 32-bit down-counter
- Counter decrements by one on each positive watchdog clock edge
- Configurable NMI generation upon watch period expiration
- Configurable CPU reset upon watch period expiration

3.14.4 LPRTC Overview

The Low-Power Real-Time Counter (LPRTC) module is a configurable high-range binary counter, which can generate an interrupt on a user-specified interval.

The device includes one LPRTC module located in the PD-0 power domain, allowing it to run even when the device is in the lowest power state and power is present on VDD_MAIN.

The LPRTC module supports the following main features:

- 32.768 kHz typical reference clock
- 32-bit incrementing counter
- 16-bit programmable prescaler

- Interrupt generation upon programmed count match
- Counter wrap mode
- The LPRTC interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPRTC. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

The LPRTC module can be utilized for the following use cases:

- Real-time clock—to keep track of the current time
- Long-term exact chronometer—to keep track of time from now up to 136 years in the future (when clocked with a 1 Hz clock signal)
- Alarm function—to generate an interrupt after a programmed number of cycles
- Long time base counter—when clocked with a kHz range clock signal from either LFXO or LFRC

3.14.5 System Timers Overview

The system timer is composed of one counter and several timer modules. The counter provides count value to the timer modules, which generate interrupts when a certain timer condition is met.

The device includes two system timers – REFCLK_TMR and S32KCLK_TMR. The REFCLK_TMR system timer is clocked by SYST_REFCLK and has four timer modules – REFCLK_CNT_BASE[0-3]. The S32KCLK_TMR system timer is clocked by S32K_CLK and has two timer modules – S32KCLK_CNT_BASE[0-1].

Each system timer supports the following main features:

- Provides a uniform view of system time
- Provides 64-bit up counters and 32-bit down counters
- Has 64-bit wide counter and compare registers
- Supports virtual time by offsetting the real time via dedicated registers
- Can be incremented by larger amounts at a lower frequency (for example, increment by 4 at 4 times lower frequency)
- Has individual interrupt output for each timer module (CNT_BASEn)

3.15 General-Purpose Input/Output Module

The General-Purpose Input/Output (GPIO) module provides means for driving and reading from digital I/O pins when they are not used by other peripheral (like UART, I2C, etc.). GPIO module can be used for tasks like lighting LEDs or reading the state of push-buttons, switches, etc. The GPIO module also offers switch contact debounce and interrupt capabilities.

The device includes up to ten GPIO modules with support of up to 74 I/O pins in total. The I/O signals are distributed as follows:

- GPIO[0-8]: 8 I/O signals each
- LPGPIO: 2 I/O signals

The I/O pins are typically powered by VDD_IO_1V8 with the exception of 6 I/O pins, which are powered by the VDD_IO_FLEX rail that is 1.8 V or 3.3 V.

The GPIO modules are integrated in two power domains:

- Power Domain PD-6: GPIO[0-8]
- Power Domain PD-0 (AON): LPGPIO

Each GPIO module supports the following main features:

- Data register allows driving and reading each GPIO pin individually
- Data Direction register selects pin direction – input or output
- Bit manipulation registers for GPIO pin set, clear, and toggle
- Debounce function driven by the 32-kHz clock for switch/push-button contacts debouncing
- Individual interrupt generation for every pin of GPIO[0-8] and LPGPIO
- Common (combined) interrupt generation for the pin events of LPGPIO
- The LPGPIO interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPGPIO. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-12 presents GPIO interface signals and provides descriptions to their functions.

Table 3-12 GPIO Signal Descriptions

Signal Name	Pin Name	Type	Description
GPIO0			
GPIO0_0	P0_0	IO	General-purpose input/output(1)
GPIO0_1	P0_1	IO	General-purpose input/output(1)
GPIO0_2	P0_2	IO	General-purpose input/output(1)
GPIO0_3	P0_3	IO	General-purpose input/output(1)
GPIO0_4	P0_4	IO	General-purpose input/output(1)
GPIO0_5	P0_5	IO	General-purpose input/output(1)
GPIO0_6	P0_6	IO	General-purpose input/output(1)
GPIO0_7	P0_7	IO	General-purpose input/output(1)
GPIO1			
GPIO1_0	P1_0	IO	General-purpose input/output
GPIO1_1	P1_1	IO	General-purpose input/output
GPIO1_2	P1_2	IO	General-purpose input/output
GPIO1_3	P1_3	IO	General-purpose input/output(3)
GPIO1_4	P1_4	IO	General-purpose input/output(3)
GPIO1_5	P1_5	IO	General-purpose input/output(3)
GPIO1_6	P1_6	IO	General-purpose input/output(3)
GPIO1_7	P1_7	IO	General-purpose input/output(3)
GPIO2			
GPIO2_0	P2_0	IO	General-purpose input/output(1)
GPIO2_1	P2_1	IO	General-purpose input/output(1)
GPIO2_2	P2_2	IO	General-purpose input/output(1)
GPIO2_3	P2_3	IO	General-purpose input/output(2)
GPIO2_4	P2_4	IO	General-purpose input/output(1)

Signal Name	Pin Name	Type	Description
GPIO2_5	P2_5	IO	General-purpose input/output(1)
GPIO2_6	P2_6	IO	General-purpose input/output(1)
GPIO2_7	P2_7	IO	General-purpose input/output(1)
GPIO3			
GPIO3_0	P3_0	IO	General-purpose input/output
GPIO3_1	P3_1	IO	General-purpose input/output
GPIO3_2	P3_2	IO	General-purpose input/output
GPIO3_3	P3_3	IO	General-purpose input/output
GPIO3_4	P3_4	IO	General-purpose input/output
GPIO3_5	P3_5	IO	General-purpose input/output
GPIO3_6	P3_6	IO	General-purpose input/output
GPIO3_7	P3_7	IO	General-purpose input/output
GPIO4			
GPIO4_0	P4_0	IO	General-purpose input/output
GPIO4_1	P4_1	IO	General-purpose input/output
GPIO4_2	P4_2	IO	General-purpose input/output
GPIO4_3	P4_3	IO	General-purpose input/output
GPIO4_4	P4_4	IO	General-purpose input/output
GPIO4_5	P4_5	IO	General-purpose input/output
GPIO4_6	P4_6	IO	General-purpose input/output
GPIO4_7	P4_7	IO	General-purpose input/output
GPIO5			
GPIO5_0	P5_0	IO	General-purpose input/output
GPIO5_1	P5_1	IO	General-purpose input/output
GPIO5_2	P5_2	IO	General-purpose input/output
GPIO5_3	P5_3	IO	General-purpose input/output
GPIO5_4	P5_4	IO	General-purpose input/output
GPIO5_5	P5_5	IO	General-purpose input/output
GPIO5_6	P5_6	IO	General-purpose input/output
GPIO5_7	P5_7	IO	General-purpose input/output
GPIO6			
GPIO6_0	P6_0	IO	General-purpose input/output
GPIO6_1	P6_1	IO	General-purpose input/output
GPIO6_2	P6_2	IO	General-purpose input/output
GPIO6_3	P6_3	IO	General-purpose input/output
GPIO6_4	P6_4	IO	General-purpose input/output
GPIO6_5	P6_5	IO	General-purpose input/output
GPIO6_6	P6_6	IO	General-purpose input/output
GPIO6_7	P6_7	IO	General-purpose input/output
GPIO7			
GPIO7_0	P7_0	IO	General-purpose input/output
GPIO7_1	P7_1	IO	General-purpose input/output
GPIO7_2	P7_2	IO	General-purpose input/output
GPIO7_3	P7_3	IO	General-purpose input/output
GPIO7_4	P7_4	IO	General-purpose input/output

Signal Name	Pin Name	Type	Description
GPIO7_5	P7_5	IO	General-purpose input/output
GPIO7_6	P7_6	IO	General-purpose input/output
GPIO7_7	P7_7	IO	General-purpose input/output
GPIO8			
GPIO8_0	P8_0	IO	General-purpose input/output
GPIO8_1	P8_1	IO	General-purpose input/output
GPIO8_2	P8_2	IO	General-purpose input/output
GPIO8_3	P8_3	IO	General-purpose input/output
GPIO8_4	P8_4	IO	General-purpose input/output
GPIO8_5	P8_5	IO	General-purpose input/output
GPIO8_6	P8_6	IO	General-purpose input/output
GPIO8_7	P8_7	IO	General-purpose input/output
LPGPIO			
GPIOV_0	P15_0	IO	Low-power general-purpose input/output[3]
GPIOV_1	P15_1	IO	Low-power general-purpose input/output

1. Serves also as analog input. See Section 3.20.6 Analog Signals.
2. Serves also as analog input/output. See Section 3.20.6 Analog Signals.
3. Powered by VDD_IO_FLEX supply rail

3.16 Communication Peripherals

3.16.1 CANFD Overview

The Controller Area Network (CANFD) module performs serial communication according to the CAN protocol. The CAN bus interface uses the basic CAN principle and meets all constraints of the CAN Specification 2.0B active. The CANFD module supports both classic CAN and CAN with Flexible Data-rate (FD) specifications.

The device includes up to two CANFD modules.

Each CANFD module supports the following main features:

- CAN specifications:
  - CAN 2.0B (up to 8 bytes payload, verified by Bosch reference model)
  - CAN FD (up to 64 bytes payload, ISO 11898-1:2015 or non-ISO Bosch)
- Free programmable data rates:
  - Data rates up to 10 Mbps
  - CAN FD rates are limited by the transceiver and the clock frequency of the CAN controller
- Programmable baud rate prescaler (1 to 1/256)
- One receive buffer and two transmit buffers—primary transmit buffer (PTB) and secondary transmit buffer (STB):
  - Buffer size: 640 words
  - Number of buffer slots: 16
- 3× independent and programmable internal 29-bit acceptance filters
- Extended features:
  - Single Shot Transmission mode (for PTB and/or for STB)
  - Listen-Only mode
  - Loop Back mode (internal and external)
  - Transceiver Standby mode

- Extended status and error report:
  - Capturing of last occurred Kind Of Error (KOER) and arbitration lost position
  - Programmable Error Warning Limit
- 32-bit synchronous Host controller interfaces
- Configurable interrupt sources
- Dual port memory block for frame buffer
- CiA 603 32-bit timestamping
- Compatible with AUTOSAR
- Optimized for SAE J1939

Table 3-13 presents CANFD interface signals and provides descriptions to their functions.

Table 3-13 CANFD Signal Descriptions

Signal Name	Pin Name	Type	Description
CANFD0 A/B/C			
CAN0_RXD_A	P2_5	I	CANFD0 serial data input (from external CAN transceiver)
CAN0_RXD_B	P5_0		
CAN0_RXD_C	P8_2		
CAN0_TXD_A	P2_4	O	CANFD0 serial data output (to external CAN transceiver)
CAN0_TXD_B	P5_1		
CAN0_TXD_C	P8_3		
CAN0_STBY_A	P0_4	O	CANFD0 transceiver standby mode signal
CAN0_STBY_B	P5_3		
CAN0_STBY_C	P8_4		
CANFD1 A/B			
CAN1_RXD_A	P1_3	I	CANFD1 serial data input (from external CAN transceiver)
CAN1_RXD_B	P8_5		
CAN1_TXD_A	P1_4	O	CANFD1 serial data output (to external CAN transceiver)
CAN1_TXD_B	P8_6		
CAN1_STBY_A	P1_5	O	CANFD1 transceiver standby mode signal
CAN1_STBY_B	P8_7		

3.16.2 CRC Overview

The Cyclic Redundancy Check (CRC) calculation module can produce 8-, 16-, and 32-bit codes for variety of polynomials. This function is used to validate the integrity of a communication packet received or the integrity of a binary image that is an update candidate. This is achieved by computing and comparing the CRC code with the one received after the data packet transmission.

The device includes one CRC module.

The CRC module has the following main features:

- Built-in support for the following CRC algorithms:
  - CRC-8-CCITT
  - CRC-16
  - CRC-16-CCITT
  - CRC-32
  - CRC-32C
- Support of customized polynomials configured by register settings

- 8- or 32-bits of data processed at a time
- Configurable byte and bit swapping of data

3.16.3 I2C Overview

The Inter-Integrated Circuit (I2C) module is a synchronous, master/slave serial communication bus which is suitable for different system control applications.

The device includes:

- Up to two I2C modules in Shared Peripherals
- One Low-Power I2C (LPI2C) slave-only module in the RTSS-HE

The I2C modules support the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)
  - Fast Mode Plus (FM+) mode (up to 1 Mbps)
- Master or slave operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 32-byte deep receive and transmit FIFOs
- Bulk transmit mode
- Interrupt or polled-mode operation
- Bit and byte waiting at all bus speeds
- DMA handshaking interface
- Programmable SDA hold time
- Bus clear feature

The LPI2C module supports the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)
- Slave operation only
- 7-bit addressing only
- Hardcoded slave bus address (0x40)
- 8-byte deep inbound and outbound FIFOs
- Interrupt or polled-mode operation
- The LPI2C interrupt can be used as a wake-up source from STANDBY low-power mode

NOTE

All Low Power peripherals are single-master accessible, including LPI2C. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-14 presents I2C interface signals and provides descriptions to their functions.

Table 3-14 I2C Signal Descriptions

Signal Name	Pin Name	Type	Description
I2C0 A/B/C			

Signal Name	Pin Name	Type	Description
I2C0_SCL_A	P1_7	IO	I2C0 serial clock line. Open-drain output driver, requires external pull-up.
I2C0_SCL_B	P2_4		
I2C0_SCL_C	P7_1		
I2C0_SDA_A	P1_6	IO	I2C0 serial data line. Open-drain output driver, requires external pull-up.
I2C0_SDA_B	P2_5		
I2C0_SDA_C	P7_0		
I2C1 A/B/C			
I2C1_SCL_A	P1_5	IO	I2C1 serial clock line. Open-drain output driver, requires external pull-up.
I2C1_SCL_B	P2_7		
I2C1_SCL_C	P7_3		
I2C1_SDA_A	P1_4	IO	I2C1 serial data line. Open-drain output driver, requires external pull-up.
I2C1_SDA_B	P2_6		
I2C1_SDA_C	P7_2		
LPI2C A/B/C			
LPI2C_SCL_A	P0_0	I	LPI2C serial clock line. Slave-only, requires external pull-up.
LPI2C_SCL_B	P2_1		
LPI2C_SCL_C	P7_4		
LPI2C_SDA_A	P0_1	IO	LPI2C serial data line. Open-drain output driver, requires external pull-up.
LPI2C_SDA_B	P2_3		
LPI2C_SDA_C	P7_5		

3.16.4 I2S Overview

The Inter-IC Sound (I^2S™) is a low pin count, serial bus standard for a stereo audio data link between ADCs, DACs, CODECs, DSPs, and others. As the I^2S only handles the transfer of audio data, the control and sub-coding signals need to be transferred separately using a different bus interface (such as I^2C).

The device includes:

- Up to two I2S modules in Shared Peripherals
- One Low-Power I2S module (LPI2S) in the RTSS-HE

Each I2S module supports the following main features:

- I^2S transmitter and receiver based on the Philips I^2S serial protocol
- One stereo channel for transmitter and one for receiver
- Full duplex communication due to the independence of transmitter and receiver
- Master mode of operation (I2S0 and LPI2S)
- Slave mode of operation (I2S1)
- 76.8 MHz input clock
- 8, 16, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling frequencies
- 16, 24, or 32 clocks word-select cycles (left/right audio channel select)
- 12, 16, 20, 24, and 32 bits of audio data resolution
- FIFO depth of 16 words for each of receiver and transmitter
- Programmable FIFO thresholds
- DMA hardware handshaking interface
- 32-bit APB data bus

NOTE

All Low Power peripherals are single-master accessible, including LPI2S. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-15 presents I2S interface signals and provides descriptions to their functions.

Table 3-15 I2S Signal Descriptions

Signal Name	Pin Name	Type	Description
I2S0 A/B/C			
I2S0_SCLK_A	P1_6	O	I2S0 serial clock
I2S0_SCLK_B	P2_6		
I2S0_SCLK_C	P8_2		
I2S0_SDI_A	P1_4	I	I2S0 serial data input line
I2S0_SDI_B	P2_4		
I2S0_SDI_C	P8_0		
I2S0_SDO_A	P1_5	O	I2S0 serial data output line
I2S0_SDO_B	P2_5		
I2S0_SDO_C	P8_1		
I2S0_WS_A	P1_7	O	I2S0 word select line
I2S0_WS_B	P2_7		
I2S0_WS_C	P8_3		
I2S1 A/B/C			
I2S1_SCLK_SLV_A	P1_3	I	I2S1 serial clock
I2S1_SCLK_SLV_B	P3_2		
I2S1_SCLK_SLV_C	P8_6		
I2S1_SDI_A	P2_0	I	I2S1 serial data input line
I2S1_SDI_B	P3_0		
I2S1_SDI_C	P8_4		
I2S1_SDO_A	P2_1	O	I2S1 serial data output line
I2S1_SDO_B	P3_1		
I2S1_SDO_C	P8_5		
I2S1_WS_SLV_A	P2_3	I	I2S1 word select line
I2S1_WS_SLV_B	P3_3		
I2S1_WS_SLV_C	P8_7		
LPI2S A/B			
LPI2S_SCLK_A	P0_2	O	LPI2S serial clock
LPI2S_SCLK_B	P4_5		
LPI2S_SDI_A	P0_0	I	LPI2S serial data input line
LPI2S_SDI_B	P4_3		
LPI2S_SDO_A	P0_1	O	LPI2S serial data output line
LPI2S_SDO_B	P4_4		
LPI2S_WS_A	P0_3	O	LPI2S word select line
LPI2S_WS_B	P4_6		

3.16.5 I3C Overview

The MIPI Improved Inter-Integrated Circuit (I3C) provides an interface to external I3C devices.

The device includes one I3C module in Shared Peripherals.

The I3C module supports the following main features:

- Secondary Master function
- Data rates:
  - Fast Mode (FM) (up to 400 kbps)
  - Fast Mode Plus (FM+) (up to 1 Mbps)
  - Single Data Rate (SDR) (up to 10 Mbps)
  - High Data Rate—Double Data Rate (HDR-DDR) (up to 20 Mbps)
- Support for legacy I2C devices
- Separate command and data buffers for each of the transfers
- Buffer depths (each location can hold 4 bytes of data):
  - Commands buffer: 8 (16 locations)
  - Response buffer: 8 (8 locations)
  - Transmit and receive data buffers: 64 (64 locations) each
- Up to 2^{16} (65536) write/read bytes with a single command
- Hardware assisted Dynamic Address Assignment (DAA) support
- Hardware assisted device role switching between current master and slave
- Hot-Join support with user controllable filter
- CRC/parity generation and validation
- Broadcast and directed Common Command Code (CCC) transfers
- DMA support through hardware handshake interface
- Autonomous clock stalling
- Device address table for addressing multiple slaves
- Dedicated buffer for capturing information from ENTDAA CCC command
- Detects arbitration loss due to incoming In-Band Interrupt (IBI) and subsequently re-transmits the command
- Use of duty cycle to achieve lower effective speed for SDR transfers to work with slower I3C slaves
- Programmable Serial Data (SDA) transmit hold
- Programmable retry count for transfers that are addressed by slaves
- IBI with 16 locations of IBI status (no IBI payload)
- Defining Byte support for vendor specific broadcast and directed CCC transfers

Table 3-16 presents I3C interface signals and provides descriptions to their functions.

Table 3-16 I3C Signal Descriptions

Signal Name	Pin Name	Type	Description
I3C A/B/C			
I3C_SCL_A	P0_5	IO	I3C serial clock line
I3C_SCL_B	P1_7		
I3C_SCL_C	P8_0		
I3C_SDA_A	P0_6	IO	I3C serial data line
I3C_SDA_B	P1_6		
I3C_SDA_C	P8_1		

3.16.6 PDM Overview

The Pulse Density Modulation (PDM) module provides an interface to Digital Microphones (DMIC). The DMIC signal first gets amplified, and then sampled at a high rate and quantized by a DMIC's internal PDM modulator. The device PDM module provides clock and decodes the received 1-bit PDM stream into 16-bit values in Pulse Code Modulation (PCM) format.

The device includes one Low-Power PDM module (LPPDM) in the RTSS-HE.

The LPPDM module supports the following main features:

- 4× 2-channel PDM microphone inputs for total support of up to 8 PDM channels (mono DMICs)
- Audio signal bandwidth of up to 96 kHz
- DMA controller interface for storing audio samples
- 16-bit PCM output per channel
- Selection between 9 modes of PDM clock frequencies from 512 kHz to 4.8 MHz (oversampling). The mode applies to all channels.
- Microphone sleep mode when at 128 kHz PDM clock
- Independent phase adjustment per channel to allow beam forming
- Independent gain adjustment per channel
- Independent peak detector per channel with programmable thresholds
- Peak detection interrupt per channel producing wake-up event
- Independent programmable DC blocking Infinite Impulse Response (IIR) filter per channel
- Independent programmable Finite Impulse Response (FIR) filter per channel
- FIFO with a capability to store up to 8 PCM samples for each channel for CPU to read
- Programmable FIFO watermark level to generate *data available* interrupt
- FIFO overrun error interrupt

NOTE

All Low Power peripherals are single-master accessible, including LPPDM. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-17 presents LPPDM interface signals and provides descriptions to their functions.

Table 3-17 LPPDM Signal Descriptions

Signal Name	Pin Name	Type	Description
LPPDM A/B/C			
LPPDM_C0_A	P1_1	O	LPPDM clock output 0 to DMIC (shared between channels 0 and 1)
LPPDM_C0_B	P3_0		
LPPDM_C0_C	P5_4		
LPPDM_C1_A	P1_3	O	LPPDM clock output 1 to DMIC (shared between channels 2 and 3)
LPPDM_C1_B	P3_2		
LPPDM_C1_C	P5_5		
LPPDM_C2_A	P1_4	O	LPPDM clock output 2 to DMIC (shared between channels 4 and 5)
LPPDM_C2_B	P3_4		
LPPDM_C2_C	P7_4		
LPPDM_C3_A	P1_6	O	LPPDM clock output 3 to DMIC (shared between channels 6 and 7)

Signal Name	Pin Name	Type	Description
LPPDM_C3_B	P3_6		
LPPDM_C3_C	P7_6		
LPPDM_D0_A	P1_0	I	LPPDM data input 0 from DMIC (shared between channels 0 and 1)
LPPDM_D0_B	P3_1		
LPPDM_D0_C	P5_6		
LPPDM_D1_A	P1_2	I	LPPDM data input 1 from DMIC (shared between channels 2 and 3)
LPPDM_D1_B	P3_3		
LPPDM_D1_C	P5_7		
LPPDM_D2_A	P1_5	I	LPPDM data input 2 from DMIC (shared between channels 4 and 5)
LPPDM_D2_B	P3_5		
LPPDM_D2_C	P7_5		
LPPDM_D3_A	P1_7	I	LPPDM data input 3 from DMIC (shared between channels 6 and 7)
LPPDM_D3_B	P3_7		
LPPDM_D3_C	P7_7		

3.16.7 SPI Overview

The Serial Peripheral Interface (SPI) module is a programmable low pin count, full-duplex master or slave synchronous serial interface.

The device includes:

- Up to three high-speed SPI modules in Shared Peripherals
- Up to two Low-Power SPI modules (LPSPI0 and LPSPI1) in the RTSS-HE, sharing device pins and thus forming a single LPSPI channel

The SPI modules support the following main features:

- 32-bit data bus width for AHB interface (SPI modules) and APB interface (LPSPI modules)
- Standard SPI mode
- Up to three slave select lines for the SPI modules, one slave select line for the LPSPI
- Multi-master contention detection
- Programmable delay on the sample time of received serial data bit for the high-speed SPI modules only (when programmed in Master mode)
- Separate Transmit and Receive FIFO buffers:
  - Buffer width of 32 bits
  - Buffer depth of 16 words
- DMA requests
- Combined interrupt lines and active high-level interrupts
- Operation modes:
  - Serial Master or Slave modes for the high-speed SPI modules
  - Master mode only for LPSPI0, and Slave mode only for LPSPI1
- Programmable frame formats:
  - Motorola Serial Peripheral Interface
  - Texas Instruments Synchronous Serial Protocol (SSP)
  - National Semiconductor Microwire
- Programmable data transfer clock bit rate for dynamic control of the serial bit rate
- Programmable data item size (4 to 32 bits) for each data transfer

NOTE

All Low Power peripherals are single-master accessible, including LPSPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-18 presents SPI interface signals and provides descriptions to their functions.

Table 3-18 SPI Signal Descriptions

Signal Name	Pin Name	Type	Description
SPI0 A/B/C			
SPI0_SCLK_A	P1_2	IO	SPI0 serial clock (driven by master)
SPI0_SCLK_B	P5_2		
SPI0_SCLK_C	P8_0		
SPI0_SS0_A	P0_0	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI0_SS0_B	P5_3		
SPI0_SS0_C	P8_1		
SPI0_SS1_A	P0_1	O	SPI0 slave select 1 (driven by master)
SPI0_SS1_B	P5_4		
SPI0_SS1_C	P8_2		
SPI0_SS2_A	P0_2	O	SPI0 slave select 2 (driven by master)
SPI0_SS2_B	P5_5		
SPI0_SS2_C	P8_3		
SPI0_MISO_A	P1_0	IO	SPI0 master in slave out
SPI0_MISO_B	P5_0		
SPI0_MISO_C	P7_6		
SPI0_MOSI_A	P1_1	IO	SPI0 master out slave in
SPI0_MOSI_B	P5_1		
SPI0_MOSI_C	P7_7		
SPI1 A/B/C			
SPI1_SCLK_A	P3_6	IO	SPI1 serial clock (driven by master)
SPI1_SCLK_B	P6_3		
SPI1_SCLK_C	P8_6		
SPI1_SS0_A	P0_3	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI1_SS0_B	P6_4		
SPI1_SS0_C	P8_7		
SPI1_SS1_A	P0_4	O	SPI1 slave select 1 (driven by master)
SPI1_SS1_B	P6_5		
SPI1_SS2_A	P0_5	O	SPI1 slave select 2 (driven by master)
SPI1_SS2_B	P6_6		
SPI1_MISO_A	P3_4	IO	SPI1 master in slave out
SPI1_MISO_B	P6_1		
SPI1_MISO_C	P8_4		
SPI1_MOSI_A	P3_5	IO	SPI1 master out slave in
SPI1_MOSI_B	P6_2		
SPI1_MOSI_C	P8_5		

Signal Name	Pin Name	Type	Description
SPI2 A/B/C			
SPI2_SCLK_A	P3_2	IO	SPI2 serial clock (driven by master)
SPI2_SCLK_B	P7_2		
SPI2_SS0_A	P3_3	IO	In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master.
SPI2_SS0_B	P7_3		
SPI2_SS1_A	P4_0	O	SPI2 slave select 1 (driven by master)
SPI2_SS1_B	P7_4	O	SPI2 slave select 1 (driven by master)
SPI2_SS2_A	P4_1	O	SPI2 slave select 2 (driven by master)
SPI2_SS2_B	P7_5	O	SPI2 slave select 2 (driven by master)
SPI2_SS2_C	P6_7	O	SPI2 slave select 2 (driven by master)
SPI2_MISO_A	P3_0	IO	SPI2 master in slave out
SPI2_MISO_B	P7_0		
SPI2_MOSI_A	P3_1	IO	SPI2 master out slave in
SPI2_MOSI_B	P7_1		
LPSPI0/1 A/B			
LPSPI_SCLK_A	P1_5	IO	LPSPI0/1 serial clock (driven by master)
LPSPI_SCLK_B	P4_4		
LPSPI_MISO_A	P1_3	IO	LPSPI0/1 master in slave out
LPSPI_MISO_B	P5_6		
LPSPI_MOSI_A	P1_4	IO	LPSPI0/1 master out slave in
LPSPI_MOSI_B	P5_7		
LPSPI_SS_A	P2_0	IO	LPSPI0/1 slave select (driven by master)
LPSPI_SS_B	P6_0		

3.16.8 UART Overview

The Universal Asynchronous Receiver/Transmitter (UART) module implements asynchronous serial communication interface based on standard Non-Return-to-Zero (NRZ) frame format.

The device includes:

- Up to six UART modules in Shared Peripherals
- One Low-Power UART module (LPUART) in the RTSS-HE
- One UART module in the SESS (SEUART)—not accessible by user application

The UART modules are integrated in the following power domains:

- Power Domain PD-6: UART[0-5]
- Power Domain PD-2: LPUART
- Power Domain PD-5: SEUART

Each UART module supports the following main features:

- Full duplex operation
- Programmable baud rates up to 2.5 Mbps with a fractional baud rate divisor
- Interrupt driven or DMA controlled data transfer
- Auto flow control compatible with 16750 devices
- Configurable character length—5, 6, 7, 8 or 9 bits
- Optional parity bit—Even, Odd, Stick
- Number of stop bits—1, 1.5, 2 bits
- Line break generation and detection

- CTS/RTS signals for hardware flow control
- Drive enable output for RS485 interface support on UART[4-5] only
- Transmit (Tx) and Receive (Rx) FIFO depth of 32 characters
- Loopback mode for test and troubleshooting
- False start bit detection
- Compatible with the industry standard 16550 devices
- The LPUART interrupt can be used as a wake-up source from STANDBY low-power mode

NOTE

All Low Power peripherals are single-master accessible, including LPUART. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-19 presents UART interface signals and provides descriptions to their functions.

Table 3-19 UART Signal Descriptions

Signal Name	Pin Name	Type	Description
UART0 A/B/C			
UART0_RX_A	P0_0	I	UART0 serial data input
UART0_RX_B	P4_0		
UART0_RX_C	P8_0		
UART0_TX_A	P0_1	O	UART0 serial data output
UART0_TX_B	P4_1		
UART0_TX_C	P8_1		
UART0_CTS_A	P0_2	I	UART0 clear to send
UART0_CTS_B	P6_6		
UART0_RTS_A	P0_3	O	UART0 request to send
UART0_RTS_B	P6_7		
UART1 A/B/C			
UART1_RX_A	P0_4	I	UART1 serial data input
UART1_RX_B	P5_0		
UART1_RX_C	P8_2		
UART1_TX_A	P0_5	O	UART1 serial data output
UART1_TX_B	P5_1		
UART1_TX_C	P8_3		
UART1_CTS_A	P0_6	I	UART1 clear to send
UART1_CTS_B	P5_6		
UART1_RTS_A	P0_7	O	UART1 request to send
UART1_RTS_B	P5_7		
UART2 A/B/C			
UART2_RX_A	P1_6	I	UART2 serial data input
UART2_RX_B	P5_2		
UART2_RX_C	P8_4		
UART2_TX_A	P1_7	O	UART2 serial data output
UART2_TX_B	P5_3		

Signal Name	Pin Name	Type	Description
UART2_TX_C	P8_5		
UART2_CTS_A	P6_2	I	UART2 clear to send
UART2_CTS_B	P6_4		
UART2_RTS_A	P6_3	O	UART2 request to send
UART2_RTS_B	P6_5		
UART3 A/B/C			
UART3_RX_A	P2_4	I	UART3 serial data input
UART3_RX_B	P3_2		
UART3_RX_C	P8_6		
UART3_TX_A	P2_5	O	UART3 serial data output
UART3_TX_B	P3_3		
UART3_TX_C	P8_7		
UART3_CTS_A	P5_4	I	UART3 clear to send
UART3_CTS_B	P7_4		
UART3_RTS_A	P5_5	O	UART3 request to send
UART3_RTS_B	P7_5		
UART4 A/B			
UART4_RX_A	P2_6	I	UART4 serial data input
UART4_RX_B	P3_6		
UART4_TX_A	P2_7	O	UART4 serial data output
UART4_TX_B	P3_7		
UART4_DE_A	P4_2	O	UART4 RS485 driver enable
UART4_DE_B	P6_0		
UART5 A/B			
UART5_RX_A	P3_0	I	UART5 serial data input
UART5_RX_B	P7_6		
UART5_TX_A	P3_1	O	UART5 serial data output
UART5_TX_B	P7_7		
UART5_DE_A	P6_1	O	UART5 RS485 driver enable
LPUART A/B			
LPUART_RX_A	P2_0	I	LPUART serial data input
LPUART_RX_B	P7_0		
LPUART_TX_A	P2_1	O	LPUART serial data output
LPUART_TX_B	P7_1		
LPUART_CTS_A	P2_3	I	LPUART clear to send
LPUART_CTS_B	P7_2		
LPUART_RTS_A	P1_3	O	LPUART request to send
LPUART_RTS_B	P7_3		
SEUART A/B/C			
SEUART_RX_A	P0_0	I	SEUART serial data input
SEUART_RX_B	P8_2		
SEUART_RX_C	P7_6		
SEUART_TX_A	P0_1	O	SEUART serial data output
SEUART_TX_B	P8_3		
SEUART_TX_C	P7_7		

3.16.9 USB Overview

The Universal Serial Bus (USB) provides an expandable, bi-directional, hot-pluggable, serial interface that allows to plug different peripherals into a USB port and have them automatically configured and ready to use. USB host and devices use memory FIFO buffers to implement data endpoints used to accept or send data from and to its endpoint counterpart.

The device includes one USB module. The USB module consists of an xHCI USB2.0 Dual-Role Device (DRD) controller, a FIFO RAM, and an on-chip PHY.

The USB module supports the following main features:

- Compliant with USB Specification 2.0
- Eight bi-directional endpoints including the bi-directional control endpoint 0, or 16 uni-directional endpoints
- Same programming model for Low-Speed (LS) (1.5 Mbit/s, host mode only), Full-Speed (FS) (12 Mbit/s), and High-Speed (HS) (480 Mbit/s) bit rates
- Internal DMA controller
- Power-saving features (clock gating)
- Link Power Management (LPM) protocol
- Hardware-controlled LPM support in Host mode
- Single 2001 × 64-bit RAM, accommodating registers, descriptor cache, Rx buffers and Tx prefetch
  - Dynamic FIFO memory allocation for endpoints
- Keep-alive feature in LS mode and (micro-)SOFs in FS and HS modes
- (micro-)SOFs (Start-of-Frame)
- Software-controlled standard USB commands (USB SETUP commands detected and forwarded to application for decoding)
- Hardware-controlled USB bus level and packet level error handling
- Low CPU utilization needs
  - Driver involved only in setting up transfers and high-level error recovery
  - Hardware handles data packing and routing to a specific pipe
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- On-chip PHY via an USB 2.0 Transceiver Macrocell Interface (UTMI+)

Table 3-20 presents USB interface signals and provides descriptions to their functions.

Table 3-20 USB Signal Descriptions

Signal Name	Pin Name	Type	Description
USB_DP	USB_DP	IO	USB 2.0 differential data (positive)
USB_DM	USB_DM	IO	USB 2.0 differential data (negative)
USB_VBUS	USB_VBUS	A	USB V_{BUS}-sense input
USB_REXT	USB_REXT	P	External calibration resistor (200 Ω ±1%) to GND

3.17 External Memory Interfaces

3.17.1 Cryptographic OSPI Overview

The cryptographic OSPI implementation in the device consists of the Octal Serial Peripheral Interface (OSPI) module and the ancillary Advanced Encryption Standard (AES) engine.

The OSPI is an intelligent peripheral offering various memory expansion options. The OSPI can work either in a direct access mode to directly read and write data to the external SPI memory, or in a decryption mode where the incoming data is decrypted on-the-fly via the AES engine.

The device includes one OSPI module, assisted by a dedicated AES engine for the cryptographic operations.

The OSPI module supports the following main features:

- Single, Dual, Quad, or Octal SPI Master mode operation
- Up to 80 MHz clock for up to 80 MB/s Single Data Rate (SDR) and 160 MB/s Dual Data Rate (DDR) support
- HyperBus protocol support for integration of HyperRAM™ modules
- Programmable instruction length, address length, wait cycles and data frame size
- Programmable option to skip address and instruction phase
- Read data strobe support in DDR mode for higher frequencies
- Support of Motorola Serial Peripheral Interface protocol
- DMA controller interface
- Programmable delay on the sample time of Received Serial Data (RXD) bit compensating routing delays
- Programmable frame size of each data transfer from 4 to 32 bits
- 128 words deep Rx and Tx FIFO buffers
- Execute-in-Place (XIP) support for read and write transfers—translates memory access requests to SPI transactions for code memory expansion. This mode supports the following main features:
  - Programmable instruction length and address length in XIP mode
  - Data frame size mapping directly from AHB transfers
  - Fixed data frame size for all the transfers
  - Continuous transfer mode for read transactions
  - Data mask support
  - Configurable data pre-fetch during XIP read transaction
  - Concurrent XIP and non-XIP transactions
  - Automatic slave select (SS) line control based on the target memory address within the OSPI allocated space in the system memory map
- eXpanded SPI (xSPI) with all the command formats as described in JEDEC xSPI version 1.0
- Two xSPI command modes:
  - 1S-1S-1S—one IO signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
  - 8D-8D-8D—eight IO signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.

The AES engine supports the following main features:

- On-the-fly decryption, transparent for the OSPI read transactions from external memory
- Electronic Codebook (ECB) mode of operation
- 128-bit long AES keys
- Secure setup and lockup of the decryption keys by the Secure Enclave at boot time

NOTE

There are operational limitations that should be considered when using the OSPI interface. Please refer to section Cryptographic OSPI Overview in the device series-specific Hardware Reference Manual for further details.

Table 3-21 presents OSPI interface signals and provides descriptions to their functions.

Table 3-21 OSPI Signal Descriptions

Signal Name	Pin Name	Type	Description
OSPI Data Bus A/B/C			
OSPI0_D0_A	P3_0	IO	OSPI data input/output 0 in enhanced SPI modes. Data output (MOSI) in standard SPI mode.
OSPI0_D0_B	P5_0		
OSPI0_D0_C	P6_0		
OSPI0_D1_A	P3_1	IO	OSPI data input/output 1 in enhanced SPI modes. Data input (MISO) in standard SPI mode.
OSPI0_D1_B	P5_1		
OSPI0_D1_C	P6_1		
OSPI0_D2_A	P3_2	IO	OSPI data 2
OSPI0_D2_B	P5_2		
OSPI0_D2_C	P6_2		
OSPI0_D3_A	P3_3	IO	OSPI data 3
OSPI0_D3_B	P5_3		
OSPI0_D3_C	P6_3		
OSPI0_D4_A	P3_4	IO	OSPI data 4
OSPI0_D4_B	P5_4		
OSPI0_D4_C	P6_4		
OSPI0_D5_A	P3_5	IO	OSPI data 5
OSPI0_D5_B	P5_5		
OSPI0_D5_C	P6_5		
OSPI0_D6_A	P3_6	IO	OSPI data 6
OSPI0_D6_B	P5_6		
OSPI0_D6_C	P6_6		
OSPI0_D7_A	P3_7	IO	OSPI data 7
OSPI0_D7_B	P5_7		
OSPI0_D7_C	P6_7		
OSPI Clock, Slave Select, Data Strobe A/B/C			
OSPI0_SCLKN_A	P4_0	O	OSPI serial clock (negative)
OSPI0_SCLKN_B	P4_6		
OSPI0_SCLKN_C	P7_1		
OSPI0_SCLK_A	P4_2	O	OSPI serial clock
OSPI0_SCLK_B	P4_7		
OSPI0_SCLK_C	P7_0		
OSPI0_RXDS_A	P4_1	IO	OSPI read data strobe (RXDS) when input. Data mask (TXD_DM) when output.
OSPI0_RXDS_B	P4_5		
OSPI0_RXDS_C	P2_3		

Signal Name	Pin Name	Type	Description
OSPI0_SS0_A	P0_2	O	OSPI slave select 0(1)
OSPI0_SS0_B	P2_0		
OSPI0_SS0_C	P7_2		
OSPI0_SS1_A	P0_3	O	OSPI slave select 1(1)
OSPI0_SS1_B	P2_1		
OSPI0_SS1_C	P7_3		

1. In XIP mode of operation, the slave select signals are automatically controlled based on the target memory address within the OSPI allocated space in the system memory map.

3.17.2 SDMMC Overview

The Secure Digital / MultiMediaCard (SDMMC) module provides an interface to embedded MultiMediaCard (eMMC™), Secure Digital® (SD®) card, and SD Input/Output (SDIO). The communication between the SDMMC module and eMMC/SD/SDIO device is performed according to the eMMC/SD/SDIO protocol.

The device includes one SDMMC module.

The SDMMC module supports the following main features:

- SD card interface:
  - 4-bit data bus
  - Complaint with SD Host Controller Standard Specification v4.20
  - Complaint with SD Physical Layer Specification v6.00
  - Backward compatible with earlier SD card specifications
  - UHS-I mode
  - Speed modes:
    - Default-Speed (DS)
    - High-Speed (HS)
    - SDR12
    - SDR25
- SDIO interface:
  - 4-bit data bus
  - Complaint with SD Specifications Part E1 SDIO Specification Version 4.10
  - SDIO read wait
  - SDIO card interrupts in both 1-bit and 4-bit modes
  - Wake-up on card interrupt
- eMMC interface:
  - 4-bit/8-bit data bus
  - Complaint with JEDEC eMMC 5.1 Specification (JESD84-B51)
  - Backward compatible with earlier eMMC specifications
  - Speed legacy modes:
    - High Speed SDR
- 32-bit slave AHB and 64-bit master AXI interface
- Data transfer types for SD and eMMC:
  - CPU
  - SDMA
  - ADMA2
  - ADMA3
- Clocking:
  - Supports independent clocks for the host controller, slave interface, and master interface
  - Supports gating of host controller base clock, if host controller is inactive

- Supports context aware functional clock gates
- Interrupt outputs:
  - Combined and separate interrupt outputs
  - Interrupt enabling and masking
- Data buffering:
  - Automatic packing/unpacking of data to fit buffer width

Table 3-22 presents SDMMC interface signals and provides descriptions to their functions.

Table 3-22 SDMMC Signal Descriptions

Signal Name	Pin Name	Type	Description
SDMMC Data Bus A/B			
SD_D0_A	P4_0	IO	SDMMC data line 0
SD_D0_B	P6_0		
SD_D1_A	P4_1	IO	SDMMC data line 1
SD_D1_B	P6_1		
SD_D2_A	P4_2	IO	SDMMC data line 2
SD_D2_B	P6_2		
SD_D3_A	P4_3	IO	SDMMC data line 3
SD_D3_B	P6_3		
SD_D4_A	P4_4	IO	SDMMC data line 4
SD_D4_B	P6_4		
SD_D5_A	P4_5	IO	SDMMC data line 5
SD_D5_B	P6_5		
SD_D6_A	P4_6	IO	SDMMC data line 6
SD_D6_B	P6_6		
SD_D7_A	P4_7	IO	SDMMC data line 7
SD_D7_B	P6_7		
SDIO Command, Clock, Reset A/B/C			
SD_CMD_A	P3_4	IO	SDMMC command/response line
SD_CMD_B	P2_6		
SD_CMD_C	P8_0		
SD_CLK_A	P3_5	O	SDMMC host to card clock line
SD_CLK_B	P2_7		
SD_CLK_C	P8_1		
SD_RST_A	P1_5	O	SDMMC reset line
SD_RST_B	P3_7		
SD_RST_C	P8_2		

3.18 Camera Interfaces

3.18.1 CPI Overview

The digital Camera Parallel Interface (CPI) enables pixel data reception from external CMOS sensors and camera modules. The data transfer rate is limited by the maximum supported pixel clock and data bus width.

The device includes:

- One Low-Power CPI (LPCPI) controller in the RTSS-HE
  - The LPCPI receives parallel data from an external camera sensor (up to 8-bit data bus)

- The LPCPI outputs the processed data on 64-bit AXI port to system memory

The LPCPI controller supports the following main features:

- Up to 60 MHz pixel clock
- Up to 8-bit data bus width
- Programmable polarity for the pixel clock, horizontal and vertical synchronization signals
- Single frame capture or continuous video frames capture
- Pixel clock output to external camera sensor

The LPCPI controller supports the following specific features:

- External camera sensor source:
  - Data modes: 1-, 2-, 4-, and 8-bit
  - Programmable MSB/LSB selection
  - Transfer 10-bit pixel encoding over 8-bit wide data bus

NOTE

All Low Power peripherals are single-master accessible, including LPCPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-23 presents LPCPI interface signals and provides descriptions to their functions.

Table 3-23 LPCPI Signal Descriptions

Signal Name	Pin Name	Type	Description
LPCPI Data Bus A/B			
LPCAM_D0_A	P4_0	I	LPCPI pixel data from external camera sensor bit [0]
LPCAM_D0_B	P7_0		
LPCAM_D1_A	P4_1	I	LPCPI pixel data from external camera sensor bit [1]
LPCAM_D1_B	P7_1		
LPCAM_D2_A	P4_2	I	LPCPI pixel data from external camera sensor bit [2]
LPCAM_D2_B	P7_2		
LPCAM_D3_A	P4_3	I	LPCPI pixel data from external camera sensor bit [3]
LPCAM_D3_B	P7_3		
LPCAM_D4_A	P4_4	I	LPCPI pixel data from external camera sensor bit [4]
LPCAM_D4_B	P7_4		
LPCAM_D5_A	P4_5	I	LPCPI pixel data from external camera sensor bit [5]
LPCAM_D5_B	P7_5		
LPCAM_D6_A	P4_6	I	LPCPI pixel data from external camera sensor bit [6]
LPCAM_D6_B	P7_6		
LPCAM_D7_A	P4_7	I	LPCPI pixel data from external camera sensor bit [7]
LPCAM_D7_B	P7_7		
LPCPI Clock and Sync A/B/C			
LPCAM_HSYNC_A	P3_5	I	LPCPI line valid from external camera sensor
LPCAM_HSYNC_B	P2_0		
LPCAM_HSYNC_C	P8_5		
LPCAM_VSYNC_A	P3_4	I	LPCPI vertical synchronization from external camera sensor

Signal Name	Pin Name	Type	Description
LPCAM_VSYNC_B	P0_6		
LPCAM_VSYNC_C	P8_4		
LPCAM_PCLK_A	P3_6	I	LPCPI pixel clock from external camera sensor
LPCAM_PCLK_B	P2_1		
LPCAM_PCLK_C	P8_6		
LPCAM_XVCLK_A	P3_7	O	LPCPI pixel clock to external camera sensor
LPCAM_XVCLK_B	P2_3		
LPCAM_XVCLK_C	P8_7		

3.19 Display Interfaces

3.19.1 DPI Controller Overview

The Display Parallel Interface (DPI) provides a 24-bit RGB data bus either directly to LCD and TFT panels with a resolution of up to WXGA (1280 × 800) or to the MIPI DSI Controller. In addition to the 24 data lines, the interface includes pixel clock up to 50 MHz, horizontal and vertical synchronization pulses, and data enable signals with configurable polarity.

The device includes a single Configurable DPI Controller (CDC).

The CDC supports the following main features:

- Configurable resolution and refresh rate
- Two display layers
- Programmable background color
- Color Look-Up Table (CLUT) with 256 × 24-bit entries per layer for indexed pixel formats
- Flexible blending between the layers using alpha value (pixel alpha or constant alpha)
- Color keying: defining transparent color for pixel formats without alpha channel
- Windowing: blending a programmable rectangular area of one layer into the other
- Gamma correction
- Dithering (2 bits per color component): providing softer color transitions for displays with less color depth
- Multiple input pixel formats selectable per layer:
  - ARGB8888, RGBA8888, RGB888, RGB565, ARGB1555, ARGB4444
  - AL44 (4-bit alpha + 4-bit luminance) and L8 (8-bit luminance)
- RGB888 output pixel format
- Master Bus Interface (MBI): 64-bit AXI interface used for pixel data transfer
- Slave Bus Interface (SBI): 32-bit APB interface used for configuration

Table 3-24 presents DPI interface signals and provides descriptions to their functions.

Table 3-24 DPI Signal Descriptions

Signal Name	Pin Name	Type	Description
DPI Data Bus A			
CDC_D0_A	P5_0	O	DPI RGB pixel data output bit B[0]
CDC_D1_A	P5_1	O	DPI RGB pixel data output bit B[1]
CDC_D2_A	P5_2	O	DPI RGB pixel data output bit B[2]
CDC_D3_A	P5_3	O	DPI RGB pixel data output bit B[3]
CDC_D4_A	P5_4	O	DPI RGB pixel data output bit B[4]
CDC_D5_A	P5_5	O	DPI RGB pixel data output bit B[5]

Signal Name	Pin Name	Type	Description
CDC_D6_A	P5_6	O	DPI RGB pixel data output bit B[6]
CDC_D7_A	P5_7	O	DPI RGB pixel data output bit B[7]
CDC_D8_A	P6_0	O	DPI RGB pixel data output bit G[0]
CDC_D9_A	P6_1	O	DPI RGB pixel data output bit G[1]
CDC_D10_A	P6_2	O	DPI RGB pixel data output bit G[2]
CDC_D11_A	P6_3	O	DPI RGB pixel data output bit G[3]
CDC_D12_A	P6_4	O	DPI RGB pixel data output bit G[4]
CDC_D13_A	P6_5	O	DPI RGB pixel data output bit G[5]
CDC_D14_A	P6_6	O	DPI RGB pixel data output bit G[6]
CDC_D15_A	P6_7	O	DPI RGB pixel data output bit G[7]
CDC_D16_A	P7_0	O	DPI RGB pixel data output bit R[0]
CDC_D17_A	P7_1	O	DPI RGB pixel data output bit R[1]
CDC_D18_A	P7_2	O	DPI RGB pixel data output bit R[2]
CDC_D19_A	P7_3	O	DPI RGB pixel data output bit R[3]
CDC_D20_A	P7_4	O	DPI RGB pixel data output bit R[4]
CDC_D21_A	P7_5	O	DPI RGB pixel data output bit R[5]
CDC_D22_A	P7_6	O	DPI RGB pixel data output bit R[6]
CDC_D23_A	P7_7	O	DPI RGB pixel data output bit R[7]
DPI Clock and Sync A/B			
CDC_DE_A	P1_5	O	DPI pixel data enable
CDC_DE_B	P3_3		
CDC_PCLK_A	P1_4	O	DPI pixel clock
CDC_PCLK_B	P3_2		
CDC_HSYNC_A	P1_6	O	DPI horizontal synchronization
CDC_HSYNC_B	P3_0		
CDC_VSYNC_A	P1_7	O	DPI vertical synchronization
CDC_VSYNC_B	P3_1		

3.19.2 DSI Overview

The MIPI Display Serial Interface (DSI) facilitates the communication and data transfer to a MIPI DSI compliant display panel. The interface is realized through a MIPI DSI host controller that implements the protocol functions defined in the MIPI DSI Specification, and a MIPI D-PHY module acting as the physical layer.

The device includes a single DSI implementation.

The DSI supports the following main features:

- Conformity to MIPI standards:
  - MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.2—16 June 2014
  - MIPI Alliance Standard for Display Pixel Interface v2.00 (DPI-2)—15 September 2005
  - MIPI Alliance Specification for Stereoscopic Display Formats (SDF) v1.0—22 November 2011
  - MIPI Alliance Specification for D-PHY v1.2, 01 August 2014
- PPI between the DSI host controller and the D-PHY transmitter
- One D-PHY TX data lane
- Up to 2.5 Gbps throughput per lane
- Bidirectional communication and escape mode support through data lane 0
- End of Transmission Packet (EoTp)

- ECC and checksum capabilities
- Fault recovery schemes
- Stereoscopic (3D) image data transmission
- Video mode only
- Configurable MIPI Display Pixel Interface (DPI) to system level that provides:
  - Data transfer in Video mode:
    - Real-time pixel stream
    - Shut Down Peripheral and Color Mode commands
  - 24-bit RGB color coding
  - Programmable polarity of all DPI interface signals
  - The maximum resolution and frame rate are limited by the pixel clock and the available DSI physical link bandwidth (defined by the number of lanes and the maximum speed per lane)
- Slave interface used for the transmission of generic commands
- Independently programmable virtual channel ID for the DPI and slave interfaces
- DPI payload FIFO with 1024 × 32-bit slots depth
- Generic command FIFO with 16 × 32-bit slots depth
- Generic payload FIFO with 128 × 32-bit slots depth
- Generic read FIFO with 32 × 32-bit slots depth
- Video mode pattern generator with the following capabilities:
  - Vertical and horizontal color bar generation without DPI stimuli
  - PHY Bit-Error Ratio (BER) pattern without DPI stimuli

The DSI does not support the following features:

- Command mode
- VESA® Display Stream Compression (DSC) standard

Table 3-25 presents MIPI DSI interface signals and provides descriptions to their functions.

Table 3-25 MIPI DSI Signal Descriptions

Signal Name	Pin Name	Type	Description
MIPIDSI_0_P	MIPIDSI_0_P	IO	DSI D-PHY Tx differential data lane 0 (positive)
MIPIDSI_0_N	MIPIDSI_0_N	IO	DSI D-PHY Tx differential data lane 0 (negative)
MIPIDSI_C_P	MIPIDSI_C_P	O	DSI D-PHY Tx differential clock lane (positive)
MIPIDSI_C_N	MIPIDSI_C_N	O	DSI D-PHY Tx differential clock lane (negative)
MIPI_REXT	MIPI_REXT	P	DSI D-PHY Tx external reference resistor (200 Ω, ±1%) connection

3.20 Analog Peripherals

3.20.1 ADC Overview

The Analog-to-Digital Converter (ADC) modules are 12-bit/24-bit, multi-input units used for analog signals conversion into digital values.

The device includes two ADC12 modules and one ADC24 module.

ADC12 modules support the following main features:

- 12-bit Successive Approximation Register (SAR) ADC
- Conversion rate of up to 1.25 MSPS

- 6 external inputs and one internal input:
  - 6 external pins may be configured to 6 single-ended or 3 differential inputs
  - One input from the on-chip temperature sensor (TSENS) (valid for ADC120 only)

ADC24 supports the following main features:

- 24-bit Sigma-Delta ADC
- Conversion rate of up to 16 kSPS
- 4 external differential inputs

ADC12 and ADC24 common features:

- Programmable gain instrumentation amplifier (up to 38 dB gain)
- On-chip offset calibration and factory calibrated gain error
- Widely programmable sample time
- Hardware averaging option (up to 256 samples) for enhanced Signal-to-Noise Ratio (SNR)
  - ADC12 must use hardware averaging at all times, with a minimum of two samples per average
- Flexible digital user interface:
  - Programmable input scan modes:
    - Single-shot or continuous conversions
    - A sequencer can be programmed to loop over a selection of inputs
  - Conversions can be triggered also externally by UTIMER events
  - Conversion results can be stored into sample registers and to SRAM via DMA
  - Hardware data shift:
    - 1 to 12 bits left shift
    - 1 to 12 bits right shift (up to 8 bits for the averaging function plus 4 bits more)
  - Threshold and window detection options. A comparator logic can generate interrupts when an input signal passes programmable thresholds
- Designed for low power operation:
  - ADC sample rate is selectable via a clock divider
  - ADC power consumption decreases as sample rate decreases
- The ADC12, ADC24, as well as other analog peripherals, are powered from a dedicated internal 1.8-V LDO

For information on ADC interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.2 DAC12 Overview

The Digital-to-Analog Converter (DAC12) module converts 12-bit digital values into analog voltage signals. The analog output range is between 0 V and 1.8 V in LP mode.

The device includes one DAC12 module.

The DAC12 module supports the following main features:

- Up to 1 kHz conversion rate at 12-bit resolution
- Accepts unsigned binary or two’s complement signed digital data
- Programmable output current up to 1.5 mA
- Programmable load capacitance compensation
- Internal 1.8-V voltage reference
- Excellent high-frequency Power Supply Rejection Ratio (PSRR)
- Maximum current output up to 1.5 mA
- Software-selectable low-power (LP) or high-performance (HP) modes
  - HP mode handles larger resistive load at the expense of higher power consumption
  - LP mode handles slow sample rate and light resistive load for power savings

For information on DAC interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.3 CMP Overview

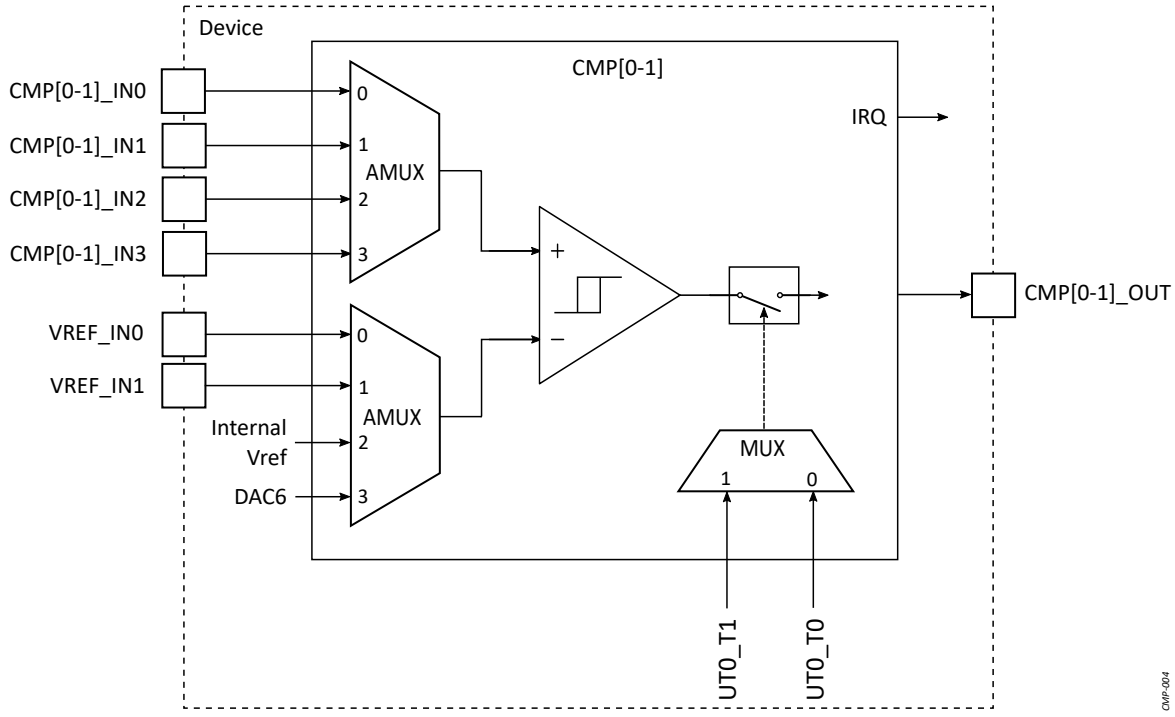
The High-Speed Comparator (CMP) module is a rail-to-rail, multi-input, analog comparator with programmable reference voltage and hysteresis.

The device includes up to two CMP modules.

Each CMP module supports the following main features:

- Reference voltage from DAC6, internal Vref, or external pins
- Programmable hysteresis
- Windowing (gating) driven by one of four events from UTIMER
- Comparator result inverter
- Configurable number of taps for filtering
- Interrupt generation after filtering
- Response time: < 5 ns
- Power supply from internal 1.8-V LDO (LDO-5)

Figure 3-11 CMP Overview



For information on CMP interface signals and their descriptions, see Section 3.20.6 Analog Signals.

Table 3-26 presents the CMP digital outputs.

Table 3-26 CMP Signal Descriptions

Signal Name	Pin Name	Type	Description
CMP Outputs A/B/C			
CMP0_OUT_A	P3_4	O	CMP0 comparison result output
CMP0_OUT_B	P4_3		
CMP0_OUT_C	P8_0		
CMP1_OUT_A	P3_5	O	CMP1 comparison result output

Signal Name	Pin Name	Type	Description
CMP1_OUT_B	P4_7		
CMP1_OUT_C	P8_1		

3.20.4 LPCMP Overview

The Low-Power Comparator (LPCMP) module is a low power, rail-to-rail, analog comparator with selectable reference voltage and hysteresis.

The device includes a single LPCMP module located in the PD0 domain.

The LPCMP supports the following main features:

- Up to four external pins for voltage monitoring
- Voltage reference from:
  - Internal AON 0.8-V voltage reference or
  - External VREF pins
- Programmable hysteresis
- Power supply from VDD_IO_1V8 pin
- Response time: < 10 µs
- The LPCMP interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

NOTE

All Low Power peripherals are single-master accessible, including LPCMP. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

For information on LPCMP interface signals and their descriptions, see Section 3.20.6 Analog Signals.

3.20.5 TSENS Overview

The Temperature Sensor (TSENS) generates a voltage V_{TEMP} that varies incrementally with the silicon die's temperature.

The TSENS is connected internally to input channel 6 of ADC120. The ADC module can convert the sensor output voltage into a digital value. The real temperature can be translated using *temperature.h* C header file available in the Alif Ensemble CMSIS pack.

The sensor provides good linearity and accuracy of better than 2.4 °C. Additional calibration can be applied to improve accuracy.

3.20.6 Analog Signals

Table 3-27 shows how the analog signals are mapped simultaneously to functions of the analog modules. Each signal can be used by more than one module at a time.

Table 3-27 Analog Signal Functions Mapping

Signal Name	Function by Module				
	ADC12	ADC24	DAC	CMP	LPCMP
ANA_S0	ADC120_IN0	ADC24_IN0_P		CMP0_IN0	
ANA_S1	ADC120_IN1	ADC24_IN1_P		CMP1_IN0	

Signal Name	Function by Module				
	ADC12	ADC24	DAC	CMP	LPCMP
ANA_S2	ADC120_IN2	ADC24_IN2_P		CMP0_IN2	
ANA_S3	ADC120_IN3	ADC24_IN3_P		CMP1_IN2	
ANA_S4	ADC120_IN4	ADC24_IN0_N		CMP0_IN3	
ANA_S5	ADC120_IN5	ADC24_IN1_N		CMP1_IN3	
ANA_S6	ADC121_IN0	ADC24_IN2_N		CMP0_IN1	
ANA_S7	ADC121_IN1	ADC24_IN3_N		CMP1_IN1	
ANA_S8				VREF_IN0	
ANA_S9				VREF_IN1	
ANA_S10					VREF_IN2
ANA_S11			DAC12_0_OUT		
ANA_S12	ADC121_IN2				LPCMP_IN0
ANA_S13	ADC121_IN3				LPCMP_IN1
ANA_S14	ADC121_IN4				LPCMP_IN2
ANA_S15	ADC121_IN5				LPCMP_IN3

Table 3-28 presents the analog signals with the respective mapping to the analog modules and provides descriptions to their functions.

Table 3-28 Analog Signal Descriptions

Signal Name	Pin Name	Type	Description
ANA_S0	P0_0	A	ADC120_IN0 (ADC120 input 0) ADC24_IN0_P (ADC24 differential input 0 positive) CMP0_IN0 (CMP0 input 0)
ANA_S1	P0_1	A	ADC120_IN1 (ADC120 input 1) ADC24_IN1_P (ADC24 differential input 1 positive) CMP1_IN0 (CMP1 input 0)
ANA_S2	P0_2	A	ADC120_IN2 (ADC120 input 2) ADC24_IN2_P (ADC24 differential input 2 positive) CMP0_IN2 (CMP0 input 2)
ANA_S3	P0_3	A	ADC120_IN3 (ADC120 input 3) ADC24_IN3_P (ADC24 differential input 3 positive) CMP1_IN2 (CMP0 input 2)
ANA_S4	P0_4	A	ADC120_IN4 (ADC120 input 4) ADC24_IN0_N (ADC24 differential input 0 negative) CMP0_IN3 (CMP0 input 3)
ANA_S5	P0_5	A	ADC120_IN5 (ADC120 input 5) ADC24_IN1_N (ADC24 differential input 1 negative) CMP1_IN3 (CMP1 input 3)
ANA_S6	P0_6	A	ADC121_IN0 (ADC121 input 0) ADC24_IN2_N (ADC24 differential input 2 negative) CMP0_IN1 (CMP0 input 1)
ANA_S7	P0_7	A	ADC121_IN1 (ADC121 input 1) ADC24_IN3_N (ADC24 differential input 3 negative) CMP1_IN1 (CMP1 input 1)
ANA_S8	P2_0	A	VREF_IN0 (CMP0-CMP1 and LPCMP reference voltage input 0)
ANA_S9	P2_1	A	VREF_IN1 (CMP0-CMP1 and LPCMP reference voltage input 1)

Signal Name	Pin Name	Type	Description
ANA_S10	P2_2	A	VREF_IN2 (LPCMP reference voltage input 2)
ANA_S11	P2_3	A	DAC12_0_OUT (DAC12 output)
ANA_S12	P2_4	A	ADC121_IN2 (ADC121 input 2) LPCMP_IN0 (LPCMP input 0)
ANA_S13	P2_5	A	ADC121_IN3 (ADC121 input 3) LPCMP_IN1 (LPCMP input 1)
ANA_S14	P2_6	A	ADC121_IN4 (ADC121 input 4) LPCMP_IN2 (LPCMP input 2)
ANA_S15	P2_7	A	ADC121_IN5 (ADC121 input 5) LPCMP_IN3 (LPCMP input 3)

3.21 Debug Infrastructure

To support the debug of multiple cores running simultaneously, the device provides an extensive debug infrastructure, compliant with the Arm® Debug Interface Architecture Specification ADIv6.0. The debug features include:

- JTAG debug support
- Serial Wire Debug (SWD) support
- External debug of SE or RTSS-HE by an off-chip debugger
- Debug through power down for RTSS-HE
- Debug from reset for all systems
- Support for single or multi-system debug
- Trace and cross trigger capabilities

Table 3-29 presents JTAG interface signals and provides descriptions to their functions.

Table 3-29 JTAG Signal Descriptions

Signal Name	Pin Name	Type	Description
JTAG			
JTAG_TCK	P0_7	I	JTAG test clock input
JTAG_TMS	P1_0	I	JTAG test mode select input
JTAG_TDI	P1_1	I	JTAG test data input
JTAG_TDO	P1_2	O	JTAG test data output
JTAG_TDATA0	P4_4	O	JTAG trace data output 0
JTAG_TDATA1	P4_5	O	JTAG trace data output 1
JTAG_TDATA2	P4_6	O	JTAG trace data output 2
JTAG_TDATA3	P4_7	O	JTAG trace data output 3
JTAG_TRACECLK	P4_3	O	JTAG trace clock output

NOTE

Code execution tracing during debug stores the resulting trace data in on-chip SRAM that can be read out of the device for formatting and post-analysis.

4 Pin Assignments

4.1 Pin Location per Package Type

4.1.1 WLCSP120 Package Pin Location Assignment

Figure 4-1 presents a simplified diagram of the WLCSP120 package pin locations.

Figure 4-1 WLCSP120 Pin Location Assignment Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A		GPIO6_2		GPIO7_0		VSS		GPIO4_5		HFXO_N		VSS
B	MIPIDSI_C_P		GPIO6_6		GPIO1_2		VDD_IO_1V8		GPIO7_2		VDD_TRX_0V8	
C		MIPIDSI_0_P		USB_DP		VDD_USB_3V3		GPIO4_6		HFXO_P		N.C.
D	MIPIDSI_C_N		GPIO6_3		USB_DM		VSS		VSS		VSS	
E		MIPIDSI_0_N		GPIO6_5		USB_VBUS		GPIO4_7		VDD_LNAPA_0V8		N.C.
F	VDD_MIPI_1V8		VSS		GPIO1_1		VDD_CORE_0V8		VDD_SX_0V8		VSS	
G		VDD_MIPI_0V8		MIPI_REXT		USB_REXT		GPIO7_1		N.C.		GPIO3_1
H	GPIO5_5		GPIO5_6		GPIO6_4		GPIO6_7		GPIO3_0		GPIO3_2	
J		GPIO5_4		GPIO5_7		GPIO1_0		GPIO4_4		GPIO3_3		VDD_CORE_0V8
K	GPIO5_0		VDD_CORE_0V8		GPIO5_3		GPIO6_1		GPIO7_4		VSS	
L		VSS		GPIO0_7		GPIO5_2		GPIO6_0		GPIO3_4		VDD_IO_1V8
M	VDD_IO_1V8		GPIO0_6		GPIO0_5		GPIO5_1		GPIO7_3		GPIO3_5	
N		GPIO0_4		N.C.		GPIO0_2		GPIO2_5		GPIO3_6		GPIO4_0
P	GPIO0_3		GPIO0_1		GPIO2_0		GPIO2_6		GPIO4_1		GPIO3_7	
R		GPIO0_0		VDD_MAIN		GPIO2_1		GPIO4_2		GPIO4_3		GPIO7_5
T	VREF_P		VSS_ANA		POR_N		GPIO2_7		GPIO7_6		GPIO7_7	
U		VREG_LP_1V8		VREG_DIG_1V8		GPIO2_2		GPIO15_0		VDD_IO_FLEX		GPIO1_3
V	VDD_BUCK		VREG_CORE_0V8		LFXO_N		VDD_IO_1V8		GPIO1_6		GPIO1_5	
W		VSW		VREG_AON		GPIO2_4		GPIO15_1		VSS		VSS
Y	VSS_BUCK		LFXO_P		GPIO2_3		VDD_CORE_0V8		GPIO1_7		GPIO1_4	

For detailed information about package outlines, thermal characteristics, and markings, see Section 6.2.1 WLCSP120 Package Information.

4.1.2 FBGA120 Package Pin Location Assignment

Figure 4-2 presents a simplified diagram of the FBGA120 package pin locations.

Figure 4-2 FBGA120 Pin Location Assignment Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VDD_SX_0V8	HFXO_N	HFXO_P	GPIO7_2	GPIO7_1	GPIO4_4	USB_VBUS	USB_DP	VDD_USB_3V3	GPIO6_3	GPIO6_2	MIPIDSI_0_P	MIPIDSI_0_N
B	VDD_TRX_0V8	VSS	GPIO7_4	GPIO7_3	GPIO4_6	GPIO4_5	GPIO7_5	USB_DM	USB_REXT	GPIO6_4	GPIO6_1	MIPIDSI_C_P	MIPIDSI_C_N
C	N.C.	N.C.										VSS	VDD_MIPI_0V8
D	VSS	VSS		GPIO3_5	GPIO1_2	GPIO4_7	GPIO1_1	GPIO1_0	GPIO7_0	GPIO6_7		MIPI_REXT	GPIO5_7
E	VDD_LNAPA_0V8	GPIO3_0		GPIO3_1						GPIO6_6		GPIO6_0	GPIO5_5
F	N.C.	GPIO3_2		GPIO4_2		GPIO4_3	VDD_CORE_0V8	VDD_IO_1V8		GPIO6_5		GPIO5_6	GPIO5_2
G	VSS	GPIO3_3		GPIO7_6		GPIO8_4	VSS			GPIO5_4		GPIO5_3	GPIO5_1
H	GPIO3_7	GPIO3_4		GPIO8_1		GPIO0_4	VSS	GPIO0_6		GPIO0_5		GPIO5_0	GPIO0_0
J	GPIO4_1	GPIO3_6		GPIO0_7						POR_N		GPIO0_2	GPIO0_1
K	GPIO8_0	GPIO4_0		GPIO1_4	VDD_IO_FLEX	GPIOV_1	GPIO2_1	GPIO0_3	GPIO2_0	VREG_AON		N.C.	VREF_P
L	GPIO8_2	GPIO7_7										VDD_MAIN	VDD_BUCK
M	GPIO8_5	GPIO8_6	GPIO8_3	GPIO1_5	GPIO1_7	GPIO2_7	GPIO2_5	GPIO2_2	LFXO_N	VREG_DIG_1V8	VSS	VSS_ANA	VSW
N	GPIO8_7	GPIO1_3	VDD_CORE_0V8	GPIO1_6	GPIOV_0	GPIO2_6	GPIO2_4	GPIO2_3	LFXO_P	VREG_MIPI_1V8	VREG_CORE_0V8	VREG_LP_1V8	VSS_BUCK

For detailed information about package outlines, thermal characteristics, and markings, see Section 6.2.2 FBGA120 Package Information.

4.2 Pin Function Options by Location

Table 4-1 describes the pin functions available as multiplexed on each pin.

NOTE

A peripheral I/O signal can be routed to up to four different pins. In such cases, a suffix _A, _B, _C, or _D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set or Pin Group.

There are no restrictions on the combination of signals from different pin groups (A, B, C, or D). However, it is user's responsibility to make sure that each peripheral I/O signal is routed to only one pin at a time through the pin multiplexing options.

Table 4-1 Pin Function Options by Location

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_0	H13	R2	GPIO0_0	IO	0	P0_0	LVCMOS ANALOG	VDD_IO_1V8
			SEUART_RX_A[a]	I	1			
			UART0_RX_A	I	2			
			LPI2S_SDI_A	I	3			
			SPI0_SS0_A	IO	4			
			LPI2C_SCL_A	I	5			
			ANA_S0	A	6			
P0_1	J13	P3	GPIO0_1	IO	0	P0_1	LVCMOS ANALOG	VDD_IO_1V8
			SEUART_TX_A[a]	O	1			
			UART0_TX_A	O	2			
			LPI2S_SDO_A	O	3			
			SPI0_SS1_A	O	4			
			LPI2C_SDA_A	IO	5			
			ANA_S1	A	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_2	J12	N6	GPIO0_2	IO	0	P0_2	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS0_A	O	2			
			UART0_CTS_A	I	3			
			LPI2S_SCLK_A	O	4			
			SPI0_SS2_A	O	5			
			ANA_S2	A	6			
P0_3	K8	P1	GPIO0_3	IO	0	P0_3	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS1_A	O	2			
			UART0_RTS_A	O	3			
			LPI2S_WS_A	O	4			
			SPI1_SS0_A	IO	5			
			ANA_S3	A	6			
P0_4	H6	N2	GPIO0_4	IO	0	P0_4	LVCMOS ANALOG	VDD_IO_1V8
			UART1_RX_A	I	2			
			SPI1_SS1_A	O	3			
			FAULT0_A	I	4			
			CAN0_STBY_A	O	5			
			ANA_S4	A	6			
P0_5	H10	M5	GPIO0_5	IO	0	P0_5	LVCMOS ANALOG	VDD_IO_1V8
			UART1_TX_A	O	2			
			SPI1_SS2_A	O	3			
			FAULT1_A	I	4			
			I3C_SCL_A	IO	5			
			ANA_S5	A	6			
P0_6	H8	M3	GPIO0_6	IO	0	P0_6	LVCMOS ANALOG	VDD_IO_1V8
			UART1_CTS_A	I	2			
			FAULT2_A	I	3			
			LPCAM_VSYNC_B	I	4			
			I3C_SDA_A	IO	5			
			ANA_S6	A	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P0_7	J4	L4	GPIO0_7	IO	0	P0_7	LVCMOS ANALOG	VDD_IO_1V8
			JTAG_TCK[a]	I	1			
			UART1_RTS_A	O	2			
			FAULT3_A	I	3			
			ANA_S7	A	4			
P1_0	D8	J6	GPIO1_0	IO	0	P1_0	LVCMOS	VDD_IO_1V8
			JTAG_TMS[a]	I	1			
			LPPDM_D0_A	I	2			
			SPI0_MISO_A	IO	3			
P1_1	D7	F5	GPIO1_1	IO	0	P1_1	LVCMOS	VDD_IO_1V8
			JTAG_TDI[a]	I	1			
			LPPDM_C0_A	O	2			
			SPI0_MOSI_A	IO	3			
P1_2	D5	B5	GPIO1_2	IO	0	P1_2	LVCMOS	VDD_IO_1V8
			JTAG_TDO[a]	O	1			
			LPPDM_D1_A	I	2			
			SPI0_SCLK_A	IO	3			
P1_3	N2	U12	GPIO1_3	IO	0	P1_3	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPUART_RTS_A	O	1			
			LPPDM_C1_A	O	2			
			I2S1_SCLK_SLV_A	I	3			
			LPSPI_MISO_A	IO	4			
			CAN1_RXD_A	I	5			
P1_4	K4	Y11	GPIO1_4	IO	0	P1_4	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPPDM_C2_A	O	1			
			I2S0_SDI_A	I	2			
			LPSPI_MOSI_A	IO	3			
			I2C1_SDA_A	IO	4			
			CDC_PCLK_A	O	5			
			CAN1_TXD_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P1_5	M4	V11	GPIO1_5	IO	0	P1_5	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPPDM_D2_A	I	1			
			I2S0_SDO_A	O	2			
			LPSPI_SCLK_A	IO	3			
			I2C1_SCL_A	IO	4			
			SD_RST_A	O	5			
			CDC_DE_A	O	6			
			CAN1_STBY_A	O	7			
P1_6	N4	V9	GPIO1_6	IO	0	P1_6	Dual Voltage LVCMOS	VDD_IO_FLEX
			UART2_RX_A	I	1			
			LPPDM_C3_A	O	2			
			I2S0_SCLK_A	O	3			
			I2C0_SDA_A	IO	4			
			CDC_HSYNC_A	O	5			
			I3C_SDA_B	IO	6			
P1_7	M5	Y9	GPIO1_7	IO	0	P1_7	Dual Voltage LVCMOS	VDD_IO_FLEX
			UART2_TX_A	O	1			
			LPPDM_D3_A	I	2			
			I2S0_WS_A	O	3			
			I2C0_SCL_A	IO	4			
			CDC_VSYNC_A	O	5			
			I3C_SCL_B	IO	6			
P2_0	K9	P5	GPIO2_0	IO	0	P2_0	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS0_B	O	1			
			LPUART_RX_A	I	2			
			I2S1_SDI_A	I	3			
			LPSPI_SS_A	IO	4			
			LPCAM_HSYNC_B	I	5			
			ANA_S8	A	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P2_1	K7	R6	GPIO2_1	IO	0	P2_1	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_SS1_B	O	1			
			LPUART_TX_A	O	2			
			I2S1_SDO_A	O	3			
			LPI2C_SCL_B	I	4			
			LPCAM_PCLK_B	I	5			
			ANA_S9	A	6			
P2_2	M8	U6	GPIO2_2	IO	0	P2_2	LVCMOS ANALOG	VDD_IO_1V8
			NSRST[a]	I	1			
			ANA_S10	A	2			
P2_3	N8	Y5	GPIO2_3	IO	0	P2_3	LVCMOS ANALOG	VDD_IO_1V8
			OSPI0_RXDS_C	IO	1			
			LPUART_CTS_A	I	2			
			I2S1_WS_SLV_A	O	3			
			LPI2C_SDA_B	IO	4			
			LPCAM_XVCLK_B	O	5			
			ANA_S11	A	6			
P2_4	N7	W6	GPIO2_4	IO	0	P2_4	LVCMOS ANALOG	VDD_IO_1V8
			UART3_RX_A	I	1			
			I2S0_SDI_B	I	2			
			I2C0_SCL_B	IO	3			
			FAULT0_B	I	4			
			CAN0_TXD_A	O	5			
			ANA_S12	A	6			
P2_5	M7	N8	GPIO2_5	IO	0	P2_5	LVCMOS ANALOG	VDD_IO_1V8
			UART3_TX_A	O	1			
			I2S0_SDO_B	O	2			
			I2C0_SDA_B	IO	3			
			FAULT1_B	I	4			
			CAN0_RXD_A	I	5			
			ANA_S13	A	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P2_6	N6	P7	GPIO2_6	IO	0	P2_6	LVCMOS ANALOG	VDD_IO_1V8
			UART4_RX_A	I	1			
			I2S0_SCLK_B	O	2			
			I2C1_SDA_B	IO	3			
			FAULT2_B	I	4			
			SD_CMD_B	IO	5			
			ANA_S14	A	6			
P2_7	M6	T7	GPIO2_7	IO	0	P2_7	LVCMOS ANALOG	VDD_IO_1V8
			UART4_TX_A	O	1			
			I2S0_WS_B	O	2			
			I2C1_SCL_B	IO	3			
			FAULT3_B	I	4			
			SD_CLK_B	O	5			
			ANA_S15	A	6			
P3_0	E2	H9	GPIO3_0	IO	0	P3_0	LVCMOS	VDD_IO_1V8
			OSPI0_D0_A	IO	1			
			UART5_RX_A	I	2			
			LPPDM_C0_B	O	3			
			I2S1_SDI_B	I	4			
			SPI2_MISO_A	IO	5			
			CDC_HSYNC_B	O	6			
P3_1	E4	G12	GPIO3_1	IO	0	P3_1	LVCMOS	VDD_IO_1V8
			OSPI0_D1_A	IO	1			
			UART5_TX_A	O	2			
			LPPDM_D0_B	I	3			
			I2S1_SDO_B	O	4			
			SPI2_MOSI_A	IO	5			
			CDC_VSYNC_B	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P3_2	F2	H11	GPIO3_2	IO	0	P3_2	LVCMOS	VDD_IO_1V8
			OSPI0_D2_A	IO	1			
			UART3_RX_B	I	2			
			LPPDM_C1_B	O	3			
			I2S1_SCLK_SLV_B	I	4			
			SPI2_SCLK_A	IO	5			
			CDC_PCLK_B	O	6			
P3_3	G2	J10	GPIO3_3	IO	0	P3_3	LVCMOS	VDD_IO_1V8
			OSPI0_D3_A	IO	1			
			UART3_TX_B	O	2			
			LPPDM_D1_B	I	3			
			I2S1_WS_SLV_B	O	4			
			SPI2_SS0_A	IO	5			
			CDC_DE_B	O	6			
P3_4	H2	L10	GPIO3_4	IO	0	P3_4	LVCMOS	VDD_IO_1V8
			OSPI0_D4_A	IO	1			
			LPPDM_C2_B	O	2			
			SPI1_MISO_A	IO	3			
			LPCAM_VSYNC_A	I	4			
			SD_CMD_A	IO	5			
			CMP0_OUT_A	O	6			
P3_5	D4	M11	GPIO3_5	IO	0	P3_5	LVCMOS	VDD_IO_1V8
			OSPI0_D5_A	IO	1			
			LPPDM_D2_B	I	2			
			SPI1_MOSI_A	IO	3			
			LPCAM_HSYNC_A	I	4			
			SD_CLK_A	O	5			
			CMP1_OUT_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P3_6	J2	N10	GPIO3_6	IO	0	P3_6	LVCMOS	VDD_IO_1V8
			OSPI0_D6_A	IO	1			
			UART4_RX_B	I	2			
			LPPDM_C3_B	O	3			
			SPI1_SCLK_A	IO	4			
			LPCAM_PCLK_A	I	5			
P3_7	H1	P11	GPIO3_7	IO	0	P3_7	LVCMOS	VDD_IO_1V8
			OSPI0_D7_A	IO	1			
			UART4_TX_B	O	2			
			LPPDM_D3_B	I	3			
			LPCAM_XVCLK_A	O	4			
			SD_RST_B	O	5			
P4_0	K2	N12	GPIO4_0	IO	0	P4_0	LVCMOS	VDD_IO_1V8
			OSPI0_SCLKN_A	O	1			
			UART0_RX_B	I	2			
			SPI2_SS1_A	O	3			
			UT0_T0_A	IO	4			
			LPCAM_D0_A	I	5			
			SD_D0_A	IO	6			
P4_1	J1	P9	GPIO4_1	IO	0	P4_1	LVCMOS	VDD_IO_1V8
			OSPI0_RXDS_A	IO	1			
			UART0_TX_B	O	2			
			SPI2_SS2_A	O	3			
			UT0_T1_A	IO	4			
			LPCAM_D1_A	I	5			
			SD_D1_A	IO	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P4_2	F4	R8	GPIO4_2	IO	0	P4_2	LVCMOS	VDD_IO_1V8
			HFXO_OUT_A	O	1			
			OSPI0_SCLK_A	O	2			
			UART4_DE_A	O	3			
			UT1_T0_A	IO	4			
			LPCAM_D2_A	I	5			
			SD_D2_A	IO	6			
P4_3	F6	R10	GPIO4_3	IO	0	P4_3	LVCMOS	VDD_IO_1V8
			JTAG_TRACECLK	O	1			
			LPI2S_SDI_B	I	2			
			UT1_T1_A	IO	3			
			LPCAM_D3_A	I	4			
			SD_D3_A	IO	5			
			CMP0_OUT_B	O	6			
P4_4	A6	J8	GPIO4_4	IO	0	P4_4	LVCMOS	VDD_IO_1V8
			JTAG_TDATA0	O	1			
			LPI2S_SDO_B	O	2			
			LPSPI_SCLK_B	IO	3			
			UT2_T0_A	IO	4			
			LPCAM_D4_A	I	5			
			SD_D4_A	IO	6			
P4_5	B6	A8	GPIO4_5	IO	0	P4_5	LVCMOS	VDD_IO_1V8
			JTAG_TDATA1	O	1			
			OSPI0_RXDS_B	IO	2			
			LPI2S_SCLK_B	O	3			
			UT2_T1_A	IO	4			
			LPCAM_D5_A	I	5			
			SD_D5_A	IO	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P4_6	B5	C8	GPIO4_6	IO	0	P4_6	LVCMOS	VDD_IO_1V8
			JTAG_TDATA2	O	1			
			OSPI0_SCLKN_B	O	2			
			LPI2S_WS_B	O	3			
			UT3_T0_A	IO	4			
			LPCAM_D6_A	I	5			
			SD_D6_A	IO	6			
P4_7	D6	E8	GPIO4_7	IO	0	P4_7	LVCMOS	VDD_IO_1V8
			JTAG_TDATA3	O	1			
			OSPI0_SCLK_B	O	2			
			UT3_T1_A	IO	3			
			LPCAM_D7_A	I	4			
			SD_D7_A	IO	5			
			CMP1_OUT_B	O	6			
P5_0	H12	K1	GPIO5_0	IO	0	P5_0	LVCMOS	VDD_IO_1V8
			OSPI0_D0_B	IO	1			
			UART1_RX_B	I	2			
			SPI0_MISO_B	IO	3			
			CDC_D0_A	O	4			
			CAN0_RXD_B	I	5			
P5_1	G13	M7	GPIO5_1	IO	0	P5_1	LVCMOS	VDD_IO_1V8
			OSPI0_D1_B	IO	1			
			UART1_TX_B	O	2			
			SPI0_MOSI_B	IO	3			
			CDC_D1_A	O	4			
			CAN0_TXD_B	O	5			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P5_2	F13	L6	GPIO5_2	IO	0	P5_2	LVCMOS	VDD_IO_1V8
			HFXO_OUT_B	O	1			
			OSPI0_D2_B	IO	2			
			UART2_RX_B	I	3			
			SPI0_SCLK_B	IO	4			
			CDC_D2_A	O	5			
P5_3	G12	K5	GPIO5_3	IO	0	P5_3	LVCMOS	VDD_IO_1V8
			OSPI0_D3_B	IO	1			
			UART2_TX_B	O	2			
			SPI0_SS0_B	IO	3			
			CDC_D3_A	O	4			
			CAN0_STBY_B	O	5			
P5_4	G10	J2	GPIO5_4	IO	0	P5_4	LVCMOS	VDD_IO_1V8
			OSPI0_D4_B	IO	1			
			UART3_CTS_A	I	2			
			LPPDM_C0_C	O	3			
			SPI0_SS1_B	O	4			
			CDC_D4_A	O	5			
P5_5	E13	H1	GPIO5_5	IO	0	P5_5	LVCMOS	VDD_IO_1V8
			OSPI0_D5_B	IO	1			
			UART3_RTS_A	O	2			
			LPPDM_C1_C	O	3			
			SPI0_SS2_B	O	4			
			CDC_D5_A	O	5			
P5_6	F12	H3	GPIO5_6	IO	0	P5_6	LVCMOS	VDD_IO_1V8
			OSPI0_D6_B	IO	1			
			UART1_CTS_B	I	2			
			LPPDM_D0_C	I	3			
			LPSPI_MISO_B	IO	4			
			CDC_D6_A	O	5			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P5_7	D13	J4	GPIO5_7	IO	0	P5_7	LVCMOS	VDD_IO_1V8
			OSPI0_D7_B	IO	1			
			UART1_RTS_B	O	2			
			LPPDM_D1_C	I	3			
			LPSPI_MOSI_B	IO	4			
			CDC_D7_A	O	5			
P6_0	E12	L8	GPIO6_0	IO	0	P6_0	LVCMOS	VDD_IO_1V8
			OSPI0_D0_C	IO	1			
			UART4_DE_B	O	2			
			LPSPI_SS_B	IO	3			
			UT0_T0_B	IO	4			
			SD_D0_B	IO	5			
			CDC_D8_A	O	6			
P6_1	B11	K7	GPIO6_1	IO	0	P6_1	LVCMOS	VDD_IO_1V8
			OSPI0_D1_C	IO	1			
			UART5_DE_A	O	2			
			SPI1_MISO_B	IO	3			
			UT0_T1_B	IO	4			
			SD_D1_B	IO	5			
			CDC_D9_A	O	6			
P6_2	A11	A2	GPIO6_2	IO	0	P6_2	LVCMOS	VDD_IO_1V8
			OSPI0_D2_C	IO	1			
			UART2_CTS_A	I	2			
			SPI1_MOSI_B	IO	3			
			UT1_T0_B	IO	4			
			SD_D2_B	IO	5			
			CDC_D10_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P6_3	A10	D3	GPIO6_3	IO	0	P6_3	LVCMOS	VDD_IO_1V8
			OSPI0_D3_C	IO	1			
			UART2_RTS_A	O	2			
			SPI1_SCLK_B	IO	3			
			UT1_T1_B	IO	4			
			SD_D3_B	IO	5			
			CDC_D11_A	O	6			
P6_4	B10	H5	GPIO6_4	IO	0	P6_4	LVCMOS	VDD_IO_1V8
			OSPI0_D4_C	IO	1			
			UART2_CTS_B	I	2			
			SPI1_SS0_B	IO	3			
			UT2_T0_B	IO	4			
			SD_D4_B	IO	5			
			CDC_D12_A	O	6			
P6_5	F10	E4	GPIO6_5	IO	0	P6_5	LVCMOS	VDD_IO_1V8
			OSPI0_D5_C	IO	1			
			UART2_RTS_B	O	2			
			SPI1_SS1_B	O	3			
			UT2_T1_B	IO	4			
			SD_D5_B	IO	5			
			CDC_D13_A	O	6			
P6_6	E10	B3	GPIO6_6	IO	0	P6_6	LVCMOS	VDD_IO_1V8
			OSPI0_D6_C	IO	1			
			UART0_CTS_B	I	2			
			SPI1_SS2_B	O	3			
			UT3_T0_B	IO	4			
			SD_D6_B	IO	5			
			CDC_D14_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P6_7	D10	H7	GPIO6_7	IO	0	P6_7	LVCMOS	VDD_IO_1V8
			OSPI0_D7_C	IO	1			
			UART0_RTS_B	O	2			
			SPI2_SS2_C	O	3			
			UT3_T1_B	IO	4			
			SD_D7_B	IO	5			
			CDC_D15_A	O	6			
P7_0	D9	A4	GPIO7_0	IO	0	P7_0	LVCMOS	VDD_IO_1V8
			OSPI0_SCLK_C	O	1			
			LPUART_RX_B	I	2			
			SPI2_MISO_B	IO	3			
			I2C0_SDA_C	IO	4			
			LPCAM_D0_B	I	5			
			CDC_D16_A	O	6			
P7_1	A5	G8	GPIO7_1	IO	0	P7_1	LVCMOS	VDD_IO_1V8
			OSPI0_SCLKN_C	O	1			
			LPUART_TX_B	O	2			
			SPI2_MOSI_B	IO	3			
			I2C0_SCL_C	IO	4			
			LPCAM_D1_B	I	5			
			CDC_D17_A	O	6			
P7_2	A4	B9	GPIO7_2	IO	0	P7_2	LVCMOS	VDD_IO_1V8
			OSPI0_SS0_C	O	1			
			LPUART_CTS_B	I	2			
			SPI2_SCLK_B	IO	3			
			I2C1_SDA_C	IO	4			
			LPCAM_D2_B	I	5			
			CDC_D18_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P7_3	B4	M9	GPIO7_3	IO	0	P7_3	LVCMOS	VDD_IO_1V8
			OSPI0_SS1_C	O	1			
			LPUART_RTS_B	O	2			
			SPI2_SS0_B	IO	3			
			I2C1_SCL_C	IO	4			
			LPCAM_D3_B	I	5			
			CDC_D19_A	O	6			
P7_4	B3	K9	GPIO7_4	IO	0	P7_4	LVCMOS	VDD_IO_1V8
			UART3_CTS_B	I	1			
			LPPDM_C2_C	O	2			
			SPI2_SS1_B	O	3			
			LPI2C_SCL_C	I	4			
			LPCAM_D4_B	I	5			
			CDC_D20_A	O	6			
P7_5	B7	R12	GPIO7_5	IO	0	P7_5	LVCMOS	VDD_IO_1V8
			UART3_RTS_B	O	1			
			LPPDM_D2_C	I	2			
			SPI2_SS2_B	O	3			
			LPI2C_SDA_C	IO	4			
			LPCAM_D5_B	I	5			
			CDC_D21_A	O	6			
P7_6	G4	T9	GPIO7_6	IO	0	P7_6	LVCMOS	VDD_IO_1V8
			SEUART_RX_C	I	1			
			UART5_RX_B	I	2			
			LPPDM_C3_C	O	3			
			SPI0_MISO_C	IO	4			
			LPCAM_D6_B	I	5			
			CDC_D22_A	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P7_7	L2	T11	GPIO7_7	IO	0	P7_7	LVCMOS	VDD_IO_1V8
			SEUART_TX_C	O	1			
			UART5_TX_B	O	2			
			LPPDM_D3_C	I	3			
			SPI0_MOSI_C	IO	4			
			LPCAM_D7_B	I	5			
			CDC_D23_A	O	6			
P8_0	K1		GPIO8_0	IO	0	P8_0	LVCMOS	VDD_IO_1V8
			UART0_RX_C	I	1			
			I2S0_SDI_C	I	2			
			SPI0_SCLK_C	IO	3			
			UT0_T0_C	IO	4			
			SD_CMD_C	IO	5			
			I3C_SCL_C	IO	6			
			CMP0_OUT_C	O	7			
P8_1	H4		GPIO8_1	IO	0	P8_1	LVCMOS	VDD_IO_1V8
			UART0_TX_C	O	1			
			I2S0_SDO_C	O	2			
			SPI0_SS0_C	IO	3			
			UT0_T1_C	IO	4			
			SD_CLK_C	O	5			
			I3C_SDA_C	IO	6			
			CMP1_OUT_C	O	7			
P8_2	L1		GPIO8_2	IO	0	P8_2	LVCMOS	VDD_IO_1V8
			SEUART_RX_B	I	1			
			UART1_RX_C	I	2			
			I2S0_SCLK_C	O	3			
			SPI0_SS1_C	O	4			
			UT1_T0_C	IO	5			
			SD_RST_C	O	6			
			CAN0_RXD_C	I	7			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P8_3	M3		GPIO8_3	IO	0	P8_3	LVCMOS	VDD_IO_1V8
			SEUART_TX_B	O	1			
			UART1_TX_C	O	2			
			I2S0_WS_C	O	3			
			SPI0_SS2_C	O	4			
			UT1_T1_C	IO	5			
			CAN0_TXD_C	O	6			
P8_4	G6		GPIO8_4	IO	0	P8_4	LVCMOS	VDD_IO_1V8
			UART2_RX_C	I	1			
			I2S1_SDI_C	I	2			
			SPI1_MISO_C	IO	3			
			UT2_T0_C	IO	4			
			LPCAM_VSYNC_C	I	5			
			CAN0_STBY_C	O	6			
P8_5	M1		GPIO8_5	IO	0	P8_5	LVCMOS	VDD_IO_1V8
			UART2_TX_C	O	1			
			I2S1_SDO_C	O	2			
			SPI1_MOSI_C	IO	3			
			UT2_T1_C	IO	4			
			LPCAM_HSYNC_C	I	5			
			CAN1_RXD_B	I	6			
P8_6	M2		GPIO8_6	IO	0	P8_6	LVCMOS	VDD_IO_1V8
			UART3_RX_C	I	1			
			I2S1_SCLK_SLV_C	I	2			
			SPI1_SCLK_C	IO	3			
			UT3_T0_C	IO	4			
			LPCAM_PCLK_C	I	5			
			CAN1_TXD_B	O	6			

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
P8_7	N1		GPIO8_7	IO	0	P8_7	LVCMOS	VDD_IO_1V8
			UART3_TX_C	O	1			
			I2S1_WS_SLV_C	O	2			
			SPI1_SS0_C	IO	3			
			UT3_T1_C	IO	4			
			LPCAM_XVCLK_C	O	5			
			CAN1_STBY_B	O	6			
P15_0	N5	U8	GPIOV_0	IO		LPGPIO_CTRL_0	Dual Voltage LVCMOS	VDD_IO_FLEX
			LPTMR0_CLK_IO	IO				
P15_1	K6	W8	GPIOV_1	IO		LPGPIO_CTRL_1	LVCMOS	VDD_IO_1V8
			LPTMR1_CLK_IO	IO				
N.C.	C1, C2, F1, K12	G10, N4, C12, E12	N.C.	N.C.				
POR_N	J10	T5	POR_N	I			LVCMOS	VDD_IO_1V8
VREF_P	K13	T1	VREF_P	A				
HFXO_P	A3	C10	HFXO_P	I			LVCMOS	VDD_IO_1V8
HFXO_N	A2	A10	HFXO_N	O			LVCMOS	VDD_IO_1V8
LFXO_P	N9	Y3	LFXO_P	I			LVCMOS	VDD_IO_1V8
LFXO_N	M9	V5	LFXO_N	O			LVCMOS	VDD_IO_1V8
VSW	M13	W2	VSW	PWR				
VREG_AON	K10	W4	VREG_AON	PWR				
VREG_LP_1V8	N12	U2	VREG_LP_1V8	PWR				
VREG_DIG_1V8	M10	U4	VREG_DIG_1V8	PWR				
VREG_CORE_0V8	N11	V3	VREG_CORE_0V8	PWR				
VREG_MIPI_1V8	N10		VREG_MIPI_1V8	PWR				
VSS	B2, C12, D1, D2, G1, G7, H7, M11	A6, A12, D7, D9, D11, F3, F11, K11, L2, W10, W12	VSS	GND				
VSS_ANA	M12	T3	VSS_ANA	GND				
VSS_BUCK	N13	Y1	VSS_BUCK	GND				

Pin Name (1)	FBGA120 Pin Location (2)	WLCSP120 Pin Location (2)	Signal Name (3)	Pin Type (4)	Multiplexing Number (5)	Configuration Register (6)	Buffer Type (7)	Power Rail (8)
VDD_SX_0V8	A1	F9	VDD_SX_0V8	PWR				
VDD_TRX_0V8	B1	B11	VDD_TRX_0V8	PWR				
VDD_MAIN	L12	R4	VDD_MAIN	PWR				
VDD_BUCK	L13	V1	VDD_BUCK	PWR				
VDD_IO_FLEX	K5	U10	VDD_IO_FLEX	PWR				
VDD_IO_1V8	F8	B7, L12, M1, V7	VDD_IO_1V8	PWR				
VDD_CORE_0V8	F7, N3	F7, J12, K3, Y7	VDD_CORE_0V8	PWR				
VDD_MIPI_0V8	C13	G2	VDD_MIPI_0V8	PWR				
VDD_MIPI_1V8		F1	VDD_MIPI_1V8	PWR				
MIPI_REXT	D12	G4	MIPI_REXT	P			DSIPHY	VDD_MIPI_0V8
MIPIDSI_0_P	A12	C2	MIPIDSI_0_P	IO			DSIPHY	VDD_MIPI_0V8
MIPIDSI_0_N	A13	E2	MIPIDSI_0_N	IO			DSIPHY	VDD_MIPI_0V8
MIPIDSI_C_P	B12	B1	MIPIDSI_C_P	O			DSIPHY	VDD_MIPI_0V8
MIPIDSI_C_N	B13	D1	MIPIDSI_C_N	O			DSIPHY	VDD_MIPI_0V8
VDD_USB_3V3	A9	C6	VDD_USB_3V3	PWR				
USB_REXT	B9	G6	USB_REXT	P			USBPHY	VDD_USB_3V3
USB_DP	A8	C4	USB_DP	IO			USBPHY	VDD_USB_3V3
USB_DM	B8	D5	USB_DM	IO			USBPHY	VDD_USB_3V3
USB_VBUS	A7	E6	USB_VBUS	A			USBPHY	VDD_USB_3V3
VDD_LNAPA_0V8	E1	E10	VDD_LNAPA_0V8	PWR				

a. Default mode after reset.

The list below describes the column headers:

1. **Pin Name**—Name of the pin. Px_y pins have several functions (mux modes) to select from. The functions of other pins are fixed.
2. **Pin Location**—Pad or ball number of the corresponding device package. An empty cell means that a ball does not exist on the package.
3. **Signal Name**—Signal(s) that can be routed to the particular pin. If a signal is routable to more than one pin, a suffix _A, _B, _C, or _D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set.
4. **Pin Type**—Pin designation (for the multiplexed pins, it depends on the selected mux mode):
   - A—Analog
   - I—Digital Input
   - O—Digital Output
   - IO—Digital Bi-directional (Input/Output)
   - R—Radio frequency

- P—Passive
- PWR—Power
- GND—Ground
- N/A—Not Available. This ball does not exist on the package.
- N.C.—No Connect

5. **Multiplexing Number**—Function number used in the pin configuration registers:
   - 0 is the GPIO function
   - 1 through 7 are possible alternative functions
   - An empty box means Not Applicable
6. **Configuration Register**—Associated pin control register. For more information, see Section 3.9 Signal Multiplexing and I/O Buffer Configuration.
7. **Buffer Type**—Associated I/O buffer type, if applicable:
   - LVCMOS—1.8-V Low-Voltage CMOS digital I/O buffer
   - Dual-Voltage (Flex) LVCMOS—1.8-V and 3.3-V LVCMOS digital I/O buffer
   - Analog—Analog input or output
   - RF—Radio Frequency input or output
   - USBPHY—HS USB data bus PHY and I/Os
   - DSIPHY—MIPI DSI display PHY and I/Os
8. **Power Rail**—I/O buffer power supply, if applicable.

4.3 Pin Function Multiplexing

Table 4-2 describes the pin functions multiplexing options.

Table 4-2 Pin Function Multiplexing

Pin Name	0	1	2	3	4	5	6	7
P0_0	GPIO0_0	SEUART_RX_A	UART0_RX_A	LPI2S_SDI_A	SPI0_SS0_A	LPI2C_SCL_A	ANA_S0	
P0_1	GPIO0_1	SEUART_TX_A	UART0_TX_A	LPI2S_SDO_A	SPI0_SS1_A	LPI2C_SDA_A	ANA_S1	
P0_2	GPIO0_2	RESERVED	OSPI0_SS0_A	UART0_CTS_A	LPI2S_SCLK_A	SPI0_SS2_A	ANA_S2	
P0_3	GPIO0_3	RESERVED	OSPI0_SS1_A	UART0_RTS_A	LPI2S_WS_A	SPI1_SS0_A	ANA_S3	
P0_4	GPIO0_4	RESERVED	UART1_RX_A	SPI1_SS1_A	FAULT0_A	CAN0_STBY_A	ANA_S4	
P0_5	GPIO0_5	RESERVED	UART1_TX_A	SPI1_SS2_A	FAULT1_A	I3C_SCL_A	ANA_S5	
P0_6	GPIO0_6	RESERVED	UART1_CTS_A	FAULT2_A	LPCAM_VSYNC_B	I3C_SDA_A	ANA_S6	
P0_7	GPIO0_7	JTAG_TCK	UART1_RTS_A	FAULT3_A	ANA_S7			
P1_0	GPIO1_0	JTAG_TMS	LPPDM_D0_A	SPI0_MISO_A				
P1_1	GPIO1_1	JTAG_TDI	LPPDM_C0_A	SPI0_MOSI_A				
P1_2	GPIO1_2	JTAG_TDO	LPPDM_D1_A	SPI0_SCLK_A				
P1_3	GPIO1_3	LPUART_RTS_A	LPPDM_C1_A	I2S1_SCLK_SLV_A	LPSPI_MISO_A	CAN1_RXD_A		
P1_4	GPIO1_4	LPPDM_C2_A	I2S0_SDI_A	LPSPI_MOSI_A	I2C1_SDA_A	CDC_PCLK_A	CAN1_TXD_A	
P1_5	GPIO1_5	LPPDM_D2_A	I2S0_SDO_A	LPSPI_SCLK_A	I2C1_SCL_A	SD_RST_A	CDC_DE_A	CAN1_STBY_A
P1_6	GPIO1_6	UART2_RX_A	LPPDM_C3_A	I2S0_SCLK_A	I2C0_SDA_A	CDC_HSYNC_A	I3C_SDA_B	
P1_7	GPIO1_7	UART2_TX_A	LPPDM_D3_A	I2S0_WS_A	I2C0_SCL_A	CDC_VSYNC_A	I3C_SCL_B	
P2_0	GPIO2_0	OSPI0_SS0_B	LPUART_RX_A	I2S1_SDI_A	LPSPI_SS_A	LPCAM_HSYNC_B	ANA_S8	
P2_1	GPIO2_1	OSPI0_SS1_B	LPUART_TX_A	I2S1_SDO_A	LPI2C_SCL_B	LPCAM_PCLK_B	ANA_S9	
P2_2	GPIO2_2	NSRST	ANA_S10					
P2_3	GPIO2_3	OSPI0_RXDS_C	LPUART_CTS_A	I2S1_WS_SLV_A	LPI2C_SDA_B	LPCAM_XVCLK_B	ANA_S11	
P2_4	GPIO2_4	UART3_RX_A	I2S0_SDI_B	I2C0_SCL_B	FAULT0_B	CAN0_TXD_A	ANA_S12	
P2_5	GPIO2_5	UART3_TX_A	I2S0_SDO_B	I2C0_SDA_B	FAULT1_B	CAN0_RXD_A	ANA_S13	
P2_6	GPIO2_6	UART4_RX_A	I2S0_SCLK_B	I2C1_SDA_B	FAULT2_B	SD_CMD_B	ANA_S14	
P2_7	GPIO2_7	UART4_TX_A	I2S0_WS_B	I2C1_SCL_B	FAULT3_B	SD_CLK_B	ANA_S15	
P3_0	GPIO3_0	OSPI0_D0_A	UART5_RX_A	LPPDM_C0_B	I2S1_SDI_B	SPI2_MISO_A	CDC_HSYNC_B	
P3_1	GPIO3_1	OSPI0_D1_A	UART5_TX_A	LPPDM_D0_B	I2S1_SDO_B	SPI2_MOSI_A	CDC_VSYNC_B	
P3_2	GPIO3_2	OSPI0_D2_A	UART3_RX_B	LPPDM_C1_B	I2S1_SCLK_SLV_B	SPI2_SCLK_A	CDC_PCLK_B	
P3_3	GPIO3_3	OSPI0_D3_A	UART3_TX_B	LPPDM_D1_B	I2S1_WS_SLV_B	SPI2_SS0_A	CDC_DE_B	

Pin Name	0	1	2	3	4	5	6	7
P3_4	GPIO3_4	OSPI0_D4_A	LPPDM_C2_B	SPI1_MISO_A	LPCAM_VSYNC_A	SD_CMD_A	CMP0_OUT_A	
P3_5	GPIO3_5	OSPI0_D5_A	LPPDM_D2_B	SPI1_MOSI_A	LPCAM_HSYNC_A	SD_CLK_A	CMP1_OUT_A	
P3_6	GPIO3_6	OSPI0_D6_A	UART4_RX_B	LPPDM_C3_B	SPI1_SCLK_A	LPCAM_PCLK_A		
P3_7	GPIO3_7	OSPI0_D7_A	UART4_TX_B	LPPDM_D3_B	LPCAM_XVCLK_A	SD_RST_B		
P4_0	GPIO4_0	OSPI0_SCLKN_A	UART0_RX_B	SPI2_SS1_A	UT0_T0_A	LPCAM_D0_A	SD_D0_A	
P4_1	GPIO4_1	OSPI0_RXDS_A	UART0_TX_B	SPI2_SS2_A	UT0_T1_A	LPCAM_D1_A	SD_D1_A	
P4_2	GPIO4_2	HFXO_OUT_A	OSPI0_SCLK_A	UART4_DE_A	UT1_T0_A	LPCAM_D2_A	SD_D2_A	
P4_3	GPIO4_3	JTAG_TRACECLK	LPI2S_SDI_B	UT1_T1_A	LPCAM_D3_A	SD_D3_A	CMP0_OUT_B	
P4_4	GPIO4_4	JTAG_TDATA0	LPI2S_SDO_B	LPSPI_SCLK_B	UT2_T0_A	LPCAM_D4_A	SD_D4_A	
P4_5	GPIO4_5	JTAG_TDATA1	OSPI0_RXDS_B	LPI2S_SCLK_B	UT2_T1_A	LPCAM_D5_A	SD_D5_A	
P4_6	GPIO4_6	JTAG_TDATA2	OSPI0_SCLKN_B	LPI2S_WS_B	UT3_T0_A	LPCAM_D6_A	SD_D6_A	
P4_7	GPIO4_7	JTAG_TDATA3	OSPI0_SCLK_B	UT3_T1_A	LPCAM_D7_A	SD_D7_A	CMP1_OUT_B	
P5_0	GPIO5_0	OSPI0_D0_B	UART1_RX_B	SPI0_MISO_B	CDC_D0_A	CAN0_RXD_B		
P5_1	GPIO5_1	OSPI0_D1_B	UART1_TX_B	SPI0_MOSI_B	CDC_D1_A	CAN0_TXD_B		
P5_2	GPIO5_2	HFXO_OUT_B	OSPI0_D2_B	UART2_RX_B	SPI0_SCLK_B	CDC_D2_A		
P5_3	GPIO5_3	OSPI0_D3_B	UART2_TX_B	SPI0_SS0_B	CDC_D3_A	CAN0_STBY_B		
P5_4	GPIO5_4	OSPI0_D4_B	UART3_CTS_A	LPPDM_C0_C	SPI0_SS1_B	CDC_D4_A		
P5_5	GPIO5_5	OSPI0_D5_B	UART3_RTS_A	LPPDM_C1_C	SPI0_SS2_B	CDC_D5_A		
P5_6	GPIO5_6	OSPI0_D6_B	UART1_CTS_B	LPPDM_D0_C	LPSPI_MISO_B	CDC_D6_A		
P5_7	GPIO5_7	OSPI0_D7_B	UART1_RTS_B	LPPDM_D1_C	LPSPI_MOSI_B	CDC_D7_A		
P6_0	GPIO6_0	OSPI0_D0_C	UART4_DE_B	LPSPI_SS_B	UT0_T0_B	SD_D0_B	CDC_D8_A	
P6_1	GPIO6_1	OSPI0_D1_C	UART5_DE_A	SPI1_MISO_B	UT0_T1_B	SD_D1_B	CDC_D9_A	
P6_2	GPIO6_2	OSPI0_D2_C	UART2_CTS_A	SPI1_MOSI_B	UT1_T0_B	SD_D2_B	CDC_D10_A	
P6_3	GPIO6_3	OSPI0_D3_C	UART2_RTS_A	SPI1_SCLK_B	UT1_T1_B	SD_D3_B	CDC_D11_A	
P6_4	GPIO6_4	OSPI0_D4_C	UART2_CTS_B	SPI1_SS0_B	UT2_T0_B	SD_D4_B	CDC_D12_A	
P6_5	GPIO6_5	OSPI0_D5_C	UART2_RTS_B	SPI1_SS1_B	UT2_T1_B	SD_D5_B	CDC_D13_A	
P6_6	GPIO6_6	OSPI0_D6_C	UART0_CTS_B	SPI1_SS2_B	UT3_T0_B	SD_D6_B	CDC_D14_A	
P6_7	GPIO6_7	OSPI0_D7_C	UART0_RTS_B	SPI2_SS2_C	UT3_T1_B	SD_D7_B	CDC_D15_A	
P7_0	GPIO7_0	OSPI0_SCLK_C	LPUART_RX_B	SPI2_MISO_B	I2C0_SDA_C	LPCAM_D0_B	CDC_D16_A	
P7_1	GPIO7_1	OSPI0_SCLKN_C	LPUART_TX_B	SPI2_MOSI_B	I2C0_SCL_C	LPCAM_D1_B	CDC_D17_A	
P7_2	GPIO7_2	OSPI0_SS0_C	LPUART_CTS_B	SPI2_SCLK_B	I2C1_SDA_C	LPCAM_D2_B	CDC_D18_A	
P7_3	GPIO7_3	OSPI0_SS1_C	LPUART_RTS_B	SPI2_SS0_B	I2C1_SCL_C	LPCAM_D3_B	CDC_D19_A	
P7_4	GPIO7_4	UART3_CTS_B	LPPDM_C2_C	SPI2_SS1_B	LPI2C_SCL_C	LPCAM_D4_B	CDC_D20_A	

Pin Name	0	1	2	3	4	5	6	7
P7_5	GPIO7_5	UART3_RTS_B	LPPDM_D2_C	SPI2_SS2_B	LPI2C_SDA_C	LPCAM_D5_B	CDC_D21_A	
P7_6	GPIO7_6	SEUART_RX_C	UART5_RX_B	LPPDM_C3_C	SPI0_MISO_C	LPCAM_D6_B	CDC_D22_A	
P7_7	GPIO7_7	SEUART_TX_C	UART5_TX_B	LPPDM_D3_C	SPI0_MOSI_C	LPCAM_D7_B	CDC_D23_A	
P8_0	GPIO8_0	UART0_RX_C	I2S0_SDI_C	SPI0_SCLK_C	UT0_T0_C	SD_CMD_C	I3C_SCL_C	CMP0_OUT_C
P8_1	GPIO8_1	UART0_TX_C	I2S0_SDO_C	SPI0_SS0_C	UT0_T1_C	SD_CLK_C	I3C_SDA_C	CMP1_OUT_C
P8_2	GPIO8_2	SEUART_RX_B	UART1_RX_C	I2S0_SCLK_C	SPI0_SS1_C	UT1_T0_C	SD_RST_C	CAN0_RXD_C
P8_3	GPIO8_3	SEUART_TX_B	UART1_TX_C	I2S0_WS_C	SPI0_SS2_C	UT1_T1_C	CAN0_TXD_C	
P8_4	GPIO8_4	UART2_RX_C	I2S1_SDI_C	SPI1_MISO_C	UT2_T0_C	LPCAM_VSYNC_C	CAN0_STBY_C	
P8_5	GPIO8_5	UART2_TX_C	I2S1_SDO_C	SPI1_MOSI_C	UT2_T1_C	LPCAM_HSYNC_C	CAN1_RXD_B	
P8_6	GPIO8_6	UART3_RX_C	I2S1_SCLK_SLV_C	SPI1_SCLK_C	UT3_T0_C	LPCAM_PCLK_C	CAN1_TXD_B	
P8_7	GPIO8_7	UART3_TX_C	I2S1_WS_SLV_C	SPI1_SS0_C	UT3_T1_C	LPCAM_XVCLK_C	CAN1_STBY_B	

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above the values listed under Table 5-1 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Parameter		Condition	Min	Max	Unit
Chip power inputs	VDD_MAIN		-0.3	5.0	V
	VDD_IO_FLEX	1.8-V mode	-0.3	1.98	V
		3.3-V mode	-0.3	3.63	V
	VDD_BUCK		-0.3	5.0	V
Input/Output voltage range (1.8 V IOs)			0.3	1.98	V
Maximum junction temperature			-40	150	°C

5.1.1 Maximum Supply Current

Table 5-2 summarizes maximum current consumption ratings at power terminals of the device.

Table 5-2 Maximum Supply Current

Parameter		Condition	Max	Unit
I_{VDD_ALL}	Supply current into all power pins		600	mA
I_{VSS_ALL}	Supply current out of all ground pin(s)		1000	mA
I_{VDD_MAIN}	Supply current rating for the VDD_MAIN pins		10	mA
$I_{VDDIO_1.8V}$	Supply current rating for the VDD_IO_1V8 pins		500	mA
$I_{VDDIO_3.3V}$	Supply current rating for the VDD_IO_FLEX pins		200	mA
I_{1V8_IO}	Current sunk, sourced by any 1.8 V I/O pin		65	mA
I_{3V6_IO}	Current sunk, sourced by any 3.6 V I/O pin		35	mA
I_{IO_ALL}	Current sunk, sourced by all pins (I/O and control)		700	mA

5.1.2 Maximum Performance Ratings

Table 5-3 lists the maximum performance per module on this device.

Table 5-3 Maximum Performance Ratings

Parameter		Max	Unit
Interconnect APB bus	SYST_PCLK	40	MHz
Interconnect AHB bus	SYST_HCLK	80	MHz
Interconnect AXI bus	SYST_ACLK	160	MHz
High-Efficiency Arm Cortex-M55	M55-HE	160	MHz
Ethos-U55 Neural Processing Units	NPU-HE	160	MHz
D/AVE 2D Graphics Processing Unit	GPU2D	160	MHz
Controller Area Network	CANFD	10	Mbps

Parameter		Max	Unit
Inter-Integrated Circuit	I2C	1.0	Mbps
	LPI2C	400	kbps
Inter-IC Sound	I2S(1)	192	kHz
	LPI2S(1)	192	kHz
MIPI Improved Inter-Integrated Circuit	I3C	20	Mbps
Pulse Density Modulator	LPPDM	4.8	MHz
Serial Peripheral Interface	SPI	40	MHz
	LPSPI	20	MHz
Universal Asynchronous Receiver/Transmitter	UART	2.5	Mbps
	LPUART	2.5	Mbps
Universal Serial Bus	USB	480	Mbps
Octal SPI	OSPI	80	MHz
Memory Card Controller	SD Card	40	MHz
	eMMC	40	MHz
	SDIO	40	MHz
Camera Parallel Interface	LPCPI	60	MHz
Display Parallel Interface	DPI	50	MHz
MIPI Display Serial Interface	DSI	2.5	Gbps/lane
Analog-to-Digital Converters	ADC12	1.25	MSPS
	ADC24	16	kSPS
Digital-to-Analog Converters	DAC12	1	kHz

1. Sampling frequency

5.2 Operating Conditions

5.2.1 General Operating Conditions

Table 5-4 presents recommended operating conditions over free-air temperature range (unless otherwise noted).

Table 5-4 General Operating Conditions

Parameter			Min	Typ	Max	Unit
VDD_MAIN[1][2]	Main power supply		1.71		4.8	V
VDD_BUCK	Internal DC-DC converter power input		1.75		4.8	V
VDD_USB_3V3	USB power input		3.0	3.3	3.6	V
VDD_IO_FLEX	GPIO flex pads (1.8 V - 3.3 V) power input	1.8-V mode[3]	1.62	1.8	1.98	V
		3.3-V mode	3.0	3.3	4.5	V
VDD_IO_1V8	GPIO standard pads (1.8 V) power input		1.08	1.8	1.98	V
VREG_DIG_1V8[4]	Internal 1.8 V regulator output		1.7	1.8	1.9	V
VREG_AON[5]	Internal voltage supply – output of internal Always-On 0.8 V LDO regulator		0.76	0.825	0.9	V
VREG_LP_1V8[6]	Internal voltage supply – output of internal low-power LDO regulator		N/A	N/A	N/A	V
VREF_P	External positive voltage reference input for ADC and DAC		1.2	1.8	1.9	V
VSS_BUCK	DC-DC converter ground			0		V
VSS_ANA	Analog ground			0		V
VSS	Digital ground			0		V
t_a	Operating ambient temperature range	Industrial (high)	-40		105	°C
t_j	Operating junction temperature range	Industrial (high)	-40		125	°C

1. When an external reset supervisor device is used, and VDD_MAIN is less than 1.8 V, it is important that the supply voltage to the supervisor device does not dip during start-up and trigger the supervisor device.
2. BOR and BOD functions not supported below 1.9 V.
3. VDD_IO_FLEX should be connected to VDD_IO_1V8 when 1.8-V mode is used.
4. VREG_DIG_1V8 must be bypassed to ground through a 1-µF capacitor in series with a 10 Ω resistor.
5. VREG_AON must be bypassed to ground through a 1-µF capacitor in series with a 1.0 kΩ resistor.
6. VREG_LP_1V8 must be bypassed to ground through a 1-µF capacitor.

CAUTION

The decoupling for VREG_AON and VREG_DIG_1V8 pins must be present on the PCB or otherwise the device may be at risk for damage.

NOTE

An external brownout supervisor must be connected to VDD_MAIN/VDD_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65 V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Refer to the Alif Application Note AAPN0040, *PCB Layout Guidelines for Ensemble E1C MCUs*, for more details and detailed information about power decoupling for all power pins.

For use of the device with external reference for VREF_P please contact an Alif representative.

5.2.2 Device Power Modes

5.2.2.1 Power Modes Case Definition

NOTE

Specifications shown in Table 5-5 Power Modes Case Definition are preliminary and subject to change after the device characterization.

Table 5-5 provides status of each module during different power modes of the device.

Table 5-5 Power Modes Case Definition

Power Mode		Voltage Regulation	MRAM	SRAM			Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption at 3.3 V		Wake Time to Reach GO Mode	
				TCM SRAM	M55-HE TCM	Utility					Typ	Units	Typ	Units
GO Modes														
GO_1	M55-HE running CoreMark at 160 MHz. NPU running convolution MAC workload.	DC-DC	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	12.5 78	mA µA/MHz	N/A	
GO_2	Only M55-HE running CoreMark at 160 MHz, cache disabled. No NPU is enabled.										7.3[3] 45	mA µA/MHz		
GO_3			OFF	OFF				All OFF			4.3[3] 26	mA µA/MHz		
GO_4	Only M55-HE running CoreMark at 76.8 MHz, cache disabled. No NPU is enabled.						HFRC				2.2 29	mA µA/MHz		
GO_5	M55-HE running										650	µA		

Power Mode		Voltage Regulation	MRAM	SRAM			Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption at 3.3 V		Wake Time to Reach GO Mode	
				TCM SRAM	M55-HE TCM	Utility					Typ	Units	Typ	Units
	CoreMark at 19.2 MHz. No NPU is enabled.										34	µA/MHz		
READY Modes														
RDY_1	M55-HE in WFI[2] at 160 MHz.	DC-DC	OFF	OFF	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	6.0	mA	< 100	ns
RDY_2	M55-HE in WFI at 76.8 MHz.						HFRC	All OFF			1.5	mA	< 200	
IDLE Modes														
IDLE_1	CPU and NPU cores powered off. 38.4 MHz clock.	DC-DC	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral [1]	2.8	mA	2 to 4	µs
IDLE_2	CPU and NPU cores powered off. 600 kHz clock.						HFRC				1600	µA		
STANDBY Modes														
STBY_1	CPU and NPU cores powered off. HFRC ready.	DC-DC	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPI2C Slave + STOP Mode peripherals	Any interrupt from a powered peripheral	40	µA	5	µs
STOP Modes														
STOP_1	STOP_2 plus 256KB of M55-HE TCM SRAM retained.	LDO	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, LPCMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral	2.6	µA	1.0	ms
STOP_2	STOP_3 plus 4KB Utility SRAM retained.				OFF						800	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, LPCMP, and LPGPIO active.					OFF					750	nA		
STOP_4	STOP_5 plus LPRTC running from								LPRTC + LPGPIO ON		700	nA		

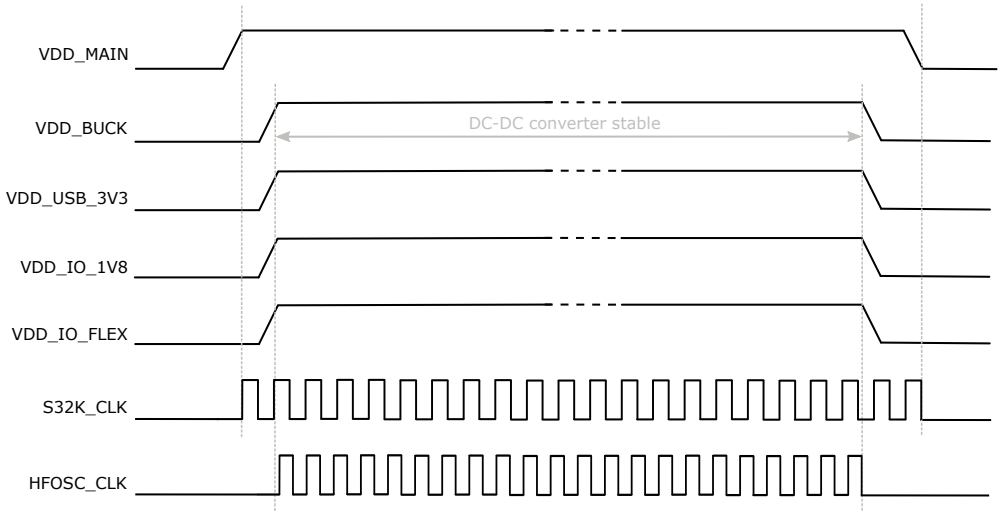
Power Mode		Voltage Regulation	MRAM	SRAM			Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption at 3.3 V		Wake Time to Reach GO Mode	
				TCM SRAM	M55-HE TCM	Utility					Typ	Units	Typ	Units
	32.768 kHz LFXO.													
STOP_5	32.7 kHz LFRC running, all other functions off.						LFRC		LPGPIO ON		600	nA		
TCM	Adder current for optional retention of ITCM SRAM0 and DTCM SRAM1 contents available in any Power Mode	DC-DC or LDO	N/A	64KB ITCM SRAM0 + 0KB DTCM SRAM1 Retained			N/A				450	nA	N/A	
				64KB ITCM SRAM0 + 64KB DTCM SRAM1 Retained							900	nA		
				128KB ITCM SRAM0 + 128KB DTCM SRAM1 Retained							1.8	µA		
				256KB ITCM SRAM0 + 256KB DTCM SRAM1 Retained							3.6	µA		
				512KB ITCM SRAM0 + 512KB DTCM SRAM1 Retained							7.2	µA		
				512KB ITCM SRAM0 + 1536KB DTCM SRAM1 Retained							14.4	µA		
SERAM	Adder current for optional retention of Secure Enclave SRAM contents available in any Power Mode	DC-DC or LDO	N/A	128KB Secure Enclave SRAM Retained			N/A				900	nA	N/A	
I/O Domain Adder for STOP in all cases.		N/A									STOP Mode current adder $I_{VDD_IO_1V8}$ when VDD_IO_1V8 = 1.8 V		N/A	
											200	nA		
Cold boot time from Power-On Reset		N/A											99	ms
Power Mode Entry													**Time**	
Time to enter STOP Mode		N/A											1.0	ms

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down. Only EWIC-connected interrupts can wake the CPU while the CPU core is powered off.
2. WFI: Wait for Interrupt.
3. At ACLK = 80 MHz, HCLK = 80 MHz, PCLK = 40 MHz.

5.2.3 Power Sequence

Figure 5-1 shows the power-up and power-down sequencing of the device.

Figure 5-1 Power-Up/Power-Down Sequencing



The following restrictions and considerations apply to Figure 5-1 Power-Up/Power-Down Sequencing:

- The power supply ramp-up time (10% to 90%) must be between 1 µs and 1 ms.
- During power-up phase, VDD_MAIN power supply must come up at the same time or before the other supplies. All other power supplies can come up in any order.
- During power-down phase, VDD_MAIN power supply must come down at the same time or after the other supplies. All other power supplies can come down in any order.
- The low-frequency S32K_CLK comes up after VDD_MAIN.
- The high-frequency HFOSC_CLK comes up after the internal DC-DC converter is stable.

NOTE

Inputs to the device (for example, NSRST, POR_N, SEUART_RX) must not be floating after power up.

An external brownout supervisor must be connected to VDD_MAIN/VDD_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65 V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Refer to the Alif Application Note AAPN0040, *PCB Layout Guidelines for Ensemble E1C MCUs*, for more details and detailed information about power decoupling for all power pins.

5.2.4 Reference Voltage Characteristics, VREF_P as an Output

Table 5-6 presents reference voltage characteristics when VREF_P is used as an output for other devices to use as a precision voltage reference.

Table 5-6 Reference Voltage Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{REFP_OUT}	Voltage reference output		1.7	1.8	1.9	V
TRIM	Trim step resolution			6	7	mV
C_{LOAD}	Load capacitor		0.8	1		µF
ESR	Equivalent series resistor of C_{LOAD}				0.2	Ω
I_{LOAD}	Static load current				10	mA
I_{LINE_REG}	Line regulation			100	400	ppm/V
T_{Coeff}	Temperature coefficient			50		ppm/°C
PSRR	Power supply rejection ratio	DC	40	60		dB
		100 kHz	20	30		dB
t_{START}	Start-up time				100	µs
$I_{DDA(VREFP_OUT)}$	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA		200	250	µA
		I_{LOAD} = 1 mA		1.2		mA

5.2.5 Electrical Sensitivity Characteristics

Table 5-7 presents Electrostatic Discharge (ESD) characteristics of the device.

Table 5-7 ESD Characteristics

Parameter		Conditions	Package	Value	Unit
ESD_{HBM}	All pins except for ones listed in(1)	ESD Human Body Model (HBM)	WLCSP/FBGA	±2000	V
ESD_{CDM}	All pins	ESD Charged Device Model (CDM)	WLCSP/FBGA	±250	V

1. ESD_{HBM} for HFXO_P, HFXO_N, LFXO_P, and LFXO_N pins: ±1000 V

Table 5-8 presents latch-up characteristics of the device.

Table 5-8 Latch-up Characteristics

Parameter		Conditions	Value	Unit
I_{LU}	Latch-Up current level	Per JEDEC JESD 78	±100	mA

5.3 Clock Characteristics

5.3.1 External Clock Source Characteristics

Table 5-9 presents the HFXO external clock source characteristics.

Table 5-9 External HFXO Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency		38.4		MHz
C_{CS}	On chip shunt capacitance (programmable by SE only)	4		20	pF
I_{CC}	Current consumption at 3.3 V		80		µA
t_j	Period jitter			1	ps
t_s	Start-up time		200		µs
t_{acr}	Frequency accuracy		set by XTAL		ppm

Parameter		Min	Typ	Max	Unit
ESR	Equivalent Series Resistance			< 100	Ω

Table 5-10 presents the LFXO external clock source characteristics.

Table 5-10 External LFXO Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency		32.768		kHz
C_{CS}	On chip shunt capacitance (programmable)	2		18	pF
I_{CC}	Current consumption at 3 V		150		nA
t_s	Start-up time		0.1	1	s
t_{acr}	Frequency accuracy		set by XTAL		ppm

5.3.2 Internal Clock Source Characteristics

Table 5-11 presents the HFRC internal clock source characteristics.

Table 5-11 Internal HFRC Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Uncalibrated frequency at 25 °C	65	76.8	88.8	MHz
f_{cs}	Calibration step		0.768		MHz
t_s	Start-up time		0.5	1	µs
t_j	Frequency variation over temperature and voltage	-2		2	%
I_{CC}	Current consumption		1.1		µA
t_{pj}	RMS period jitter		42		ps

Table 5-12 presents the LFRC internal clock source characteristics.

Table 5-12 Internal LFRC Clock Source Characteristics

Parameter		Min	Typ	Max	Unit
f_c	Frequency at 25 °C		32.7		kHz
t_j	Frequency variation over temperature and voltage	-4		4	%

5.3.3 PLL Characteristics

Table 5-13 presents the PLL characteristics.

Table 5-13 PLL Characteristics

Parameter		Min	Typ	Max	Unit
f_{C_IN}	Input clock frequency		38.4		MHz
f_{C_OUT}	Output clock frequency		480		MHz
t_{SET}	Settling time		20		µs
f_{DC}	Output clock duty cycle		50		%
$t_{j(CLK)}$	Output clock jitter (period jitter)			2	ps
I_{CC}	Current consumption at 3.3 V supply		0.11		mA

Parameter		Min	Typ	Max	Unit
$I_{CC(PWR-DWN)}$	Power-down current consumption			0.1	µA

5.3.4 Audio PLL Characteristics

Table 5-14 presents the Audio PLL characteristics.

Table 5-14 Audio PLL Characteristics

Parameter		Min	Typ	Max	Unit
f_{C_IN}	Input clock frequency (HFXO only)		38.4		MHz
f_{C_OUT}	Output clock frequency		76.8		MHz
t_{SET}	Settling time		20		µs
f_{DC}	Output clock duty cycle		50		%
$t_{j(CLK)}$	Output clock jitter (period jitter)			2	ps
I_{CC}	Current consumption at 3.3 V supply		0.11		mA
$I_{CC(PWR-DWN)}$	Power-down current consumption			0.1	µA

5.4 Memory Characteristics

Table 5-15 presents MRAM characteristics.

Table 5-15 MRAM Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
I_{MRAM}	MRAM current consumption	3.3 V device supply. 25 °C ambient temperature.	Write		30		mA
			Read		10		mA
			Power down		50		µA
N_{MRAMR}	Number of read cycles					Unlimited	Cycles
N_{MRAME}	Number of erase cycles					100000	Cycles
$t_{MRAMW16}$	Write time, non-DMA	Write operation, 16 bytes (minimum number of bytes that can be written in one write operation)			TBD		µs
		Effective write time and rate			TBD		µs
					TBD		MB/s
$t_{MRAMWDMA}$	Write time, DMA	DMA write operation, 128 bytes (maximum DMA cycle payload)			TBD		µs
		Effective write time and rate			TBD		ns
					TBD		MB/s
$t_{MRAMR16}$	Read time	Read operation, 16 bytes		TBD		TBD	ns
				TBD		TBD	MB/s

Table 5-16 presents SRAM throughput characteristics.

Table 5-16 SRAM Throughput Characteristics

Memory Block	Transaction Data Width (Bytes)	Achievable Read Throughput (MB/s) Read Originating from:	Achievable Write Throughput (MB/s) Write Originating from:
		M55-HE at 160 MHz	M55-HE at 160 MHz
SRAM0	4	TBD	TBD
SRAM1	8	TBD	TBD

NOTE

User SRAM size and availability is device part number dependent. For more information on SRAM block enabled for each part number and their size, see Section 7 Ordering Information.

5.5 I/O Buffer Characteristics

5.5.1 I/O Parameter Test Conditions

Unless otherwise specified, typical values are taken at t_a = 25 °C and typical supply voltages as specified in Table 5-4 General Operating Conditions. Where statistical variation is relevant and unless otherwise specified, typical values represent parts at the mean of the distribution.

Unless otherwise specified the minimum and maximum values are taken across the full temperature and voltage range. Where statistical variation is relevant and unless otherwise specified, minimum and maximum values represent parts that are three standard deviations away from the mean of the distribution.

All values are based on laboratory characterization.

5.5.2 LVCMOS DC Specifications

Table 5-17 presents the LVCMOS I/O DC specifications.

Table 5-17 LVCMOS DC Specifications (1.8 V Logic)

Parameter		Min	Typ	Max	Unit
Input					
V_{IH}	Input logic high voltage	0.65 × VDD_IO_1V8		VDD_IO_1V8 + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDD_IO_1V8	V
R_{pu}	Input pull-up resistance		50		kΩ
R_{pd}	Input pull-down resistance		50		kΩ
Output					
$V_{OH(DC)}$	DC Output logic high voltage	VDD_IO_1V8 - 0.4			V
$V_{OL(DC)}$	DC Output logic low voltage			0.4	V
I_{OL}	Output drive current (programmable)			2, 4, 8, or 12	mA

5.5.3 Dual-Voltage (Flex) LVCMOS DC Specifications

Table 5-18 presents the dual-voltage (Flex) LVCMOS I/O DC specifications.

Table 5-18 Dual-Voltage (Flex) LVCMOS DC Specifications (1.8 V / 3.3 V Logic)

Parameter		Min	Typ	Max	Unit
Input					
V_{IH}	Input logic high voltage	0.65 × VDD_IO_FLEX (1)		VDD_IO_FLEX(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDD_IO_FLEX (1)	V
R_{pu}	Input pull-up resistance		50		kΩ
R_{pd}	Input pull-down resistance		50		kΩ
Output					
$V_{OH(DC)}$	DC Output logic high voltage	VDD_IO_FLEX(1) - 0.4			V
$V_{OL(DC)}$	DC Output logic low voltage			0.4	V
I_{OL}	Output drive current (programmable)			2, 4, 8, or 12	mA

1. The voltage supply can be 1.8 V or 3.3 V.

5.5.4 MIPI DSI DC Specifications

The DSI interface (DSIPHY port type) electrical characteristics are compliant with MIPI Alliance Specification for D-PHY v1.2.

5.5.5 USB DC Specifications

The USB interface (USBPHY port type) electrical characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

5.6 Analog Peripherals Characteristics

5.6.1 ADC Characteristics

Table 5-19 presents the ADC12 electrical characteristics.

Table 5-19 ADC12 Electrical Characteristics

Parameter		Conditions			Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V from external 3.3 V supply (DC-DC)				12		Bits
f_s	Operational speed				312		5000	kHz
E_G	Gain error (calibrated)					6.1		LSB
E_O	Offset error					0.41		LSB
E_L	Integral nonlinearity						3	LSB
E_D	Differential nonlinearity						2	LSB
ENOB	Effective number of	Internal ADC voltage	Single-ended	1.25 MSPS (2.5 MHz, Ave(1) = 2)		9.25		Bits

Parameter		Conditions			Min	Typ	Max	Unit
	bits	reference = 1.8 V		0.5 MSPS (1 MHz, Ave = 2)		9.65		
				1.0 MSPS (5 MHz, Ave = 4)		10.00		
				0.625 MSPS (2.5 MHz, Ave = 4)		10.00		
				0.25 MSPS (1 MHz, Ave = 4)		10.15		
		Ambient temperature = 25 °C	Differential	1.25 MSPS (2.5 MHz, Ave = 2)		10.25		
				0.5 MSPS (1 MHz, Ave = 2)		10.50		
				1.0 MSPS (5 MHz, Ave = 4)		11.00		
				0.625 MSPS (2.5 MHz, Ave = 4)		11.00		
				0.25 MSPS (1 MHz, Ave = 4)		11.25		
SNR	Signal-to-noise ratio		Single-ended	1.25 MSPS (2.5 MHz, Ave = 2)		58.8		dB
			Differential			64.8		
T_{HD}	Total harmonic distortion		Single-ended	1.25 MSPS (2.5 MHz, Ave = 2)		-63.3		dB
			Differential			-68.8		
I_{DDA}	Current consumption		f_S = 5 MHz			0.50	0.80	mA
			f_S = 2.5 MHz			0.30	0.47	

1. Ave: Averaging factor

Table 5-20 presents the ADC24 electrical characteristics.

Table 5-20 ADC24 Electrical Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V provided by on-die DC-DC with external 3.3 V supply			24		Bits
f_S	Sampling rate			1		16	kSPS
E_G	Gain error				1.5		% of FSR
E_O	Offset error				50		µV
T_{HD}	Total harmonic distortion	Internal ADC voltage reference = 1.8 V	1 kSPS		-80		dB
			16 kSPS		-74		
SNR	Signal to noise ratio	Differential mode, PGA off Ambient temperature = 25 °C	1 kSPS		106		dB
			16 kSPS		93.5		
I_{DDA}	Current consumption				0.45	1.0	mA
V_{CM}	Common Mode			200		1600	mV

5.6.2 DAC12 Characteristics

Table 5-21 presents the DAC12 electrical characteristics.

Table 5-21 DAC12 Electrical Characteristics

Parameter		Conditions		Min	Typ	Max	Unit
RES	Resolution	Internal ADC voltage supply = 1.8 V provided by on-die DC-DC with external 3.3 V supply Internal ADC voltage reference = 1.8 V Ambient temperature = 25 °C			12		Bits
f_c	Conversion rate					1.0	kHz
I_{OUT}	Output drive current		High-performance mode			1.5	mA
E_G	Gain error		High-performance mode		1.5		% of FSR
			Low-power mode		1.5		
E_{Off}	Offset error		High-performance mode		0.14		% of FSR
			Low-power mode		0.01		
I_{DDA}	Current consumption		High-performance mode		2.0		mA
			Low-power mode		150		µA
INL	Integral nonlinearity		High-performance mode	-2		3.2	LSB
			Low-power mode	-1.5		2.6	
DNL	Differential nonlinearity		High-performance mode	-2.2		1.5	LSB
			Low-power mode	-1.1		1.8	

5.6.3 CMP Characteristics

Table 5-22 presents the high-speed comparator electrical characteristics.

Table 5-22 CMP Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{IN}	Comparator input voltage range		-0.3		VDD(1) + 0.3	V
V_{OFFSET_IN}	Input offset	Full common mode range			20	mV
I_{CC}	Current consumption	High-speed mode			200	µA
V_{HYS}	Hysteresis	0.7 V ≤ Vin ≤ VDD(1) - 0.7 V	5		30	mV
I_{bias}	Comparator input bias current				10	nA
t_{RES}	Response time	High-speed mode			5	ns

1. Power supply from LDO-5. For more information on configuration, refer to the CMP_COMP_REG2[ANA_PERIPH_LDO_CONT] register field in the corresponding series-specific Hardware Reference Manual.

5.6.4 LPCMP Characteristics

Table 5-23 presents the low power comparator electrical characteristics.

Table 5-23 LPCMP Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage (from VDD_IO_1V8)		1.62	1.8	1.98	V
V_{IN}	Comparator input voltage range		-0.3		V_{DDA} + 0.3	V
V_{OFFSET_IN}	Input offset	Full common mode range			20	mV
I_{CC}	Current consumption	Low power mode			20	µA
V_{HYS}	Hysteresis	0.7 V ≤ Vin ≤ V_{DDA}–0.7 V	5		30	mV
I_{bias}	Comparator input bias current				10	nA
t_{RES}	Response time	Low power mode			10	µs

5.7 Timing Characteristics

5.7.1 Timing Test Conditions

Table 5-24 shows general description of used symbols, adopted standards, terminology, and test process. Unless otherwise specified, all timing parameters are characterized assuming load capacitance of 10 pF.

Table 5-24 Timing Test Conditions

Parameter	Description
f_{op}	Operating frequency
t_c	Cycle time (period)
t_d	Delay time
t_{dsbl}	Disable time
t_{en}	Enable time
t_h	Hold time
t_s	Setup time
t_{tr}	Transition time
t_v	Valid time
t_{pd}	Pulse duration
t_F	Fall time
t_R	Rise time
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{REF}	Reference voltage
t_{RES}	Timer resolution time
RES	Timer resolution
$t_{P_COUNTER}$	Counter clock period
t_{MAX_COUNT}	Maximum possible count
$f_{(baud)}$	Maximum programmable baud rate
$t_{(BUF)}$	Bus free time
start	Start bit
C_b	Capacitive load
Dc	Duty cycle
JIT	Jitter
t_{CAS}	Clock after START condition
t_{CBT}	Clock before STOP condition
t_{CASr}	Clock after repeated START
t_{CBSr}	Clock before repeated START
$t_{MMovrLAP}$	Current master to secondary master overlap time during hand off
t_{MMLOCK}	Time internal where new master not driving SDA low
t_{BAC}	Bus available condition
T_{BIC}	Bus idle condition

5.7.2 Timers and Counters

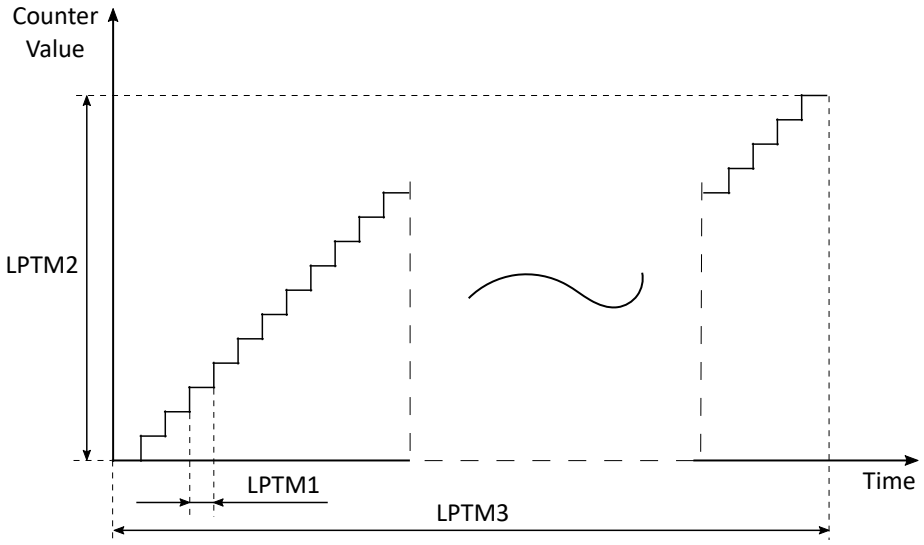
5.7.2.1 LPTIMER Timing Characteristics

Table 5-25 and Figure 5-2 present the LPTIMER timing characteristics.

Table 5-25 LPTIMER Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
Condition: f_{LPTIM_CLK} = 128 kHz (see Table 5-12 Internal LFRC Clock Source Characteristics)						
LPTM1	t_{RES}	Timer resolution time		7.8		µs
LPTM2	$t_{P_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
LPTM3	t_{MAX_COUNT}	Maximum possible count per timer			32000	s
Condition: f_{LPTIM_CLK} = 32.768 kHz (see Table 5-10 External LFXO Clock Source Characteristics)						
LPTM1	t_{RES}	Timer resolution time		30.5		µs
LPTM2	$t_{P_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
LPTM3	t_{MAX_COUNT}	Maximum possible count per timer			120000	s

Figure 5-2 LPTIMER Timing Diagram



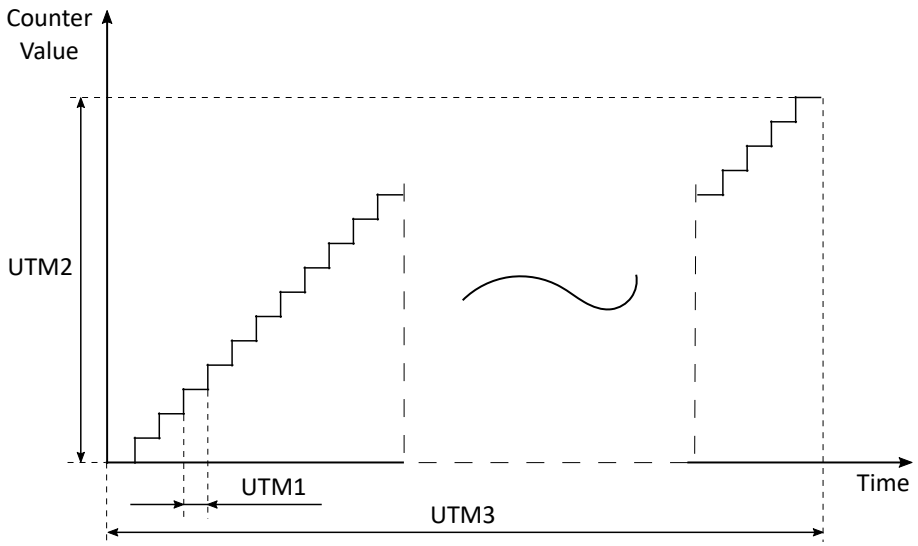
5.7.2.2 UTIMER Timing Characteristics

Table 5-26 and Figure 5-3 present the UTIMER timing characteristics.

Table 5-26 UTIMER Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
Condition: f_{UTIM_CLK} = 160 MHz						
UTM1	t_{RES}	Timer resolution time		6.25		ns
UTM2	$t_{P_COUNTER}$	Cycle time counter	1		2^{32} - 1	counts
UTM3	t_{PERIOD}	Timer period	12.5×10^{-9}		26.84	s

Figure 5-3 UTIMER Timing Diagram



5.7.3 Communication Peripherals

5.7.3.1 CANFD Timing Characteristics

Table 5-27 presents the CANFD timing characteristics.

Table 5-27 CANFD Timing Characteristics

No	Parameter		Min	Max	Unit
CAN1	$f_{(baud)}$	Maximum programmable baud rate		10	Mbps
CAN2	$t_{d_shift_TX}$	Delay time, transmit shift register to Tx pin		10	ns
CAN3	$t_{d_RX_shift}$	Delay time, Rx pin to receive shift register		30	ns

5.7.3.2 I2C Timing Characteristics

Table 5-28 and Figure 5-4 present the I2C timing characteristics.

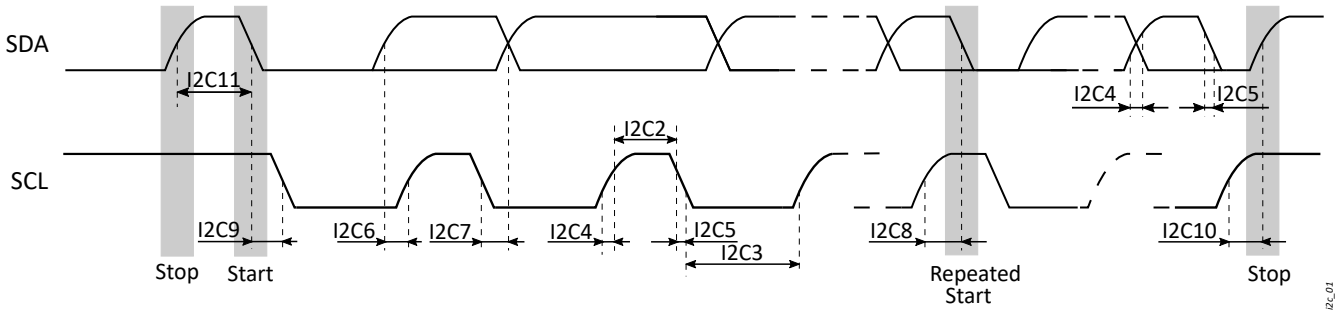
Table 5-28 I2C Timing Characteristics

No	Parameter		SS		FS		FM+		Unit
			Min	Max	Min	Max	Min	Max	
	t_{c_SCL}	Cycle time	10		2.5		1		µs
I2C2	t_{pd_SCL-H}	Pulse duration, SCL high		0.450		1.320		0.500	µs
I2C3	t_{pd_SCL-L}	Pulse duration, SCL low		0.450		1.320		0.500	µs
I2C4	$t_{R_SDA_SCL}$	Rise time of SDA and SCL signals	20	300	20	300	20	120	ns
I2C5	$t_{F_SDA_SCL}$	Fall time of SDA and SCL signals	See table note(1)	300	See table note(1)	300	See table note(1)	120	ns
I2C6	$t_{s_SDA_SCL}$	Setup time, SDA to SCL		0.1		0.1		0.1	µs
I2C7	$t_{h_SDA_SCL}$	Hold time, SDA to SCL							µs
I2C8	$t_{s_SCL_start}$	Setup time, SCL to repeated START condition		0.6		0.26		0.26	µs
I2C9	$t_{h_start_SCL}$	Hold time, START condition to SCL		0.6		0.26		0.26	µs

No	Parameter		SS		FS		FM+		Unit
			Min	Max	Min	Max	Min	Max	
I2C10	$t_{h_SCL_stop}$	Setup time, SCL to STOP condition		0.6		0.26		0.26	µs
I2C11	$t_{BUF_start_stop}$	Bus free time between STOP and START condition		1.3		0.5		0.5	µs
	C_{b_bus}	Capacitive load for each bus line		50		50		50	pF

1. 20 × (VDD_IO_1V8 ÷ 5.5 V)
2. Supported only by I2C modules

Figure 5-4 I2C Timing Diagram



5.7.3.3 I2S Timing Characteristics

Table 5-29, Figure 5-5, and Figure 5-6 present the I2S timing characteristics.

Table 5-29 I2S Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
	f_{op_SCK}	Operation frequency, SCK (serial clock)	2.27	2.5	2.78	MHz
I2S3	t_{c_SCK}	Cycle time, SCK (serial clock)	440	400	360	ns
I2S4	t_{pd_SCK-H}	Pulse duration, SCK high	160			ns
I2S5	t_{pd_SCK-L}	Pulse duration, SCK low	160			ns
I2S6	$t_{d_SCK_WS}$	Delay time, SCK output low to WS valid			$0.8 \times t_{c_SCK}$	ns
I2S7	$t_{d_SCK_SDOUT}$	Delay time, SCK output low to SDOUT valid			$0.8 \times t_{c_SCK}$	ns
I2S8	$t_{s_SDIN_master}$	Setup time, SDIN master mode	60			ns
I2S9	$t_{s_SDIN_slave}$	Setup time, SDIN slave mode	60			ns
I2S10	$t_{h_SDIN_master}$	Hold time, SDIN master mode	100			ns
I2S11	$t_{h_SDIN_slave}$	Hold time, SDIN slave mode	0			ns

Figure 5-5 I2S Master Mode Timing Diagram

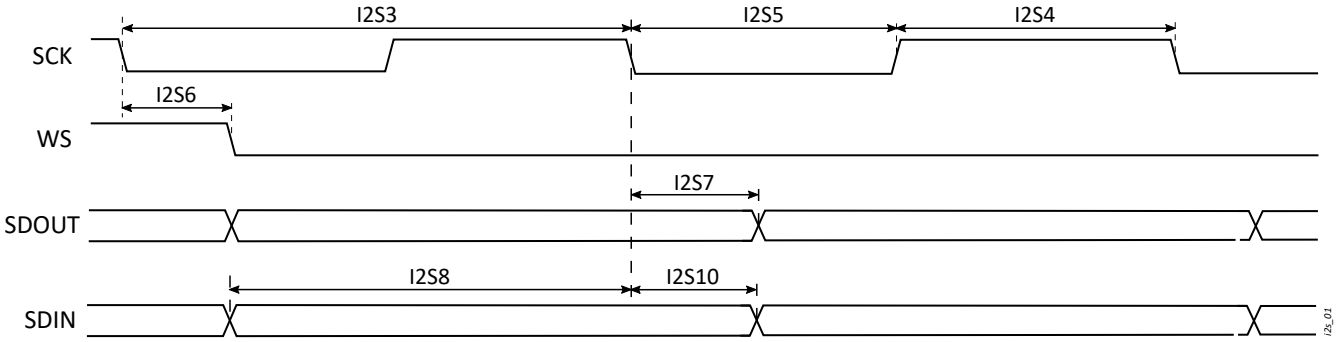
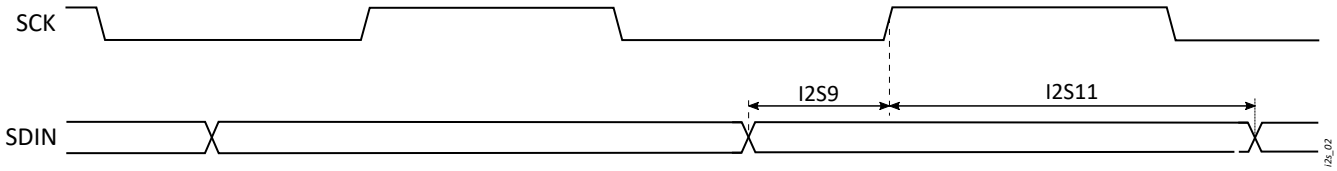


Figure 5-6 I2S Slave Mode Timing Diagram



5.7.3.4 I3C Timing Characteristics

Table 5-30, Table 5-31, Figure 5-7, and Figure 5-8 present the I3C timing characteristics.

Table 5-30 I3C Open Drain Timing Characteristics

No	Parameter		Mode	Min	Max	Unit
I3C1	t_{pd_SCL-L}	Pulse duration, SCL low	Master	200		ns
I3C2	t_{pd_SCL-H}	Pulse duration, SCL high	Master	200		ns
I3C3	t_{F_SDA}	Fall time, SDA	Master		11	ns
I3C4	t_{s_SDA-OD}	Setup time, SDA open drain	Master	3		ns
I3C5	t_{CAS}	Clock after START condition	Master	38.4		ns
I3C6	t_{CBT}	Clock before STOP condition	Master	19.2		ns
I3C7	$t_{MMovrLAP}$	Current master to secondary master overlap time during hand off	Master	212		ns
I3C8	t_{BAC}	Bus available condition	Master	1000		ns
I3C9	T_{BIC}	Bus idle condition	Master	200000		ns
I3C10	t_{MMLOCK}	Time internal where new master not driving SDA Low	Master	1000		ns

Table 5-31 I3C Push-Pull Timing Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
I3C1	t_c	Cycle time, SCL	Master	100000	77.52	ns
I3C2	t_{pd_SCL-L}	Pulse duration, SCL low	Master	32		ns
I3C4	t_{pd_SCL-H}	Pulse duration, SCL high	Master	32		ns
I3C5	$t_{d_SCL_SDA}$	Delay time, SCL to SDA out	Master		12	ns
I3C6	t_{R_SCL}	Rise time, SCL	Master		12	ns
I3C7	t_{F_SCL}	Fall time, SCL	Master		12	ns
I3C8	th_SDA	Hold time, SDA	Master in push-pull	15		ns

NO.	PARAMETER		MODE	MIN	MAX	UNIT
I3C9	ts_SDA	Setup time, SDA	Master in push-pull	15		ns
I3C10	t_{CASr}	Clock after repeated START	Master	19.2		ns
I3C11	t_{CBSr}	Clock before repeated START	Master	19.2		ns
	C_b	Capacitive load per bus line (SDA/SCL)	Master, Slave	50		pf

Figure 5-7 I3C Open Drain Timing Diagram

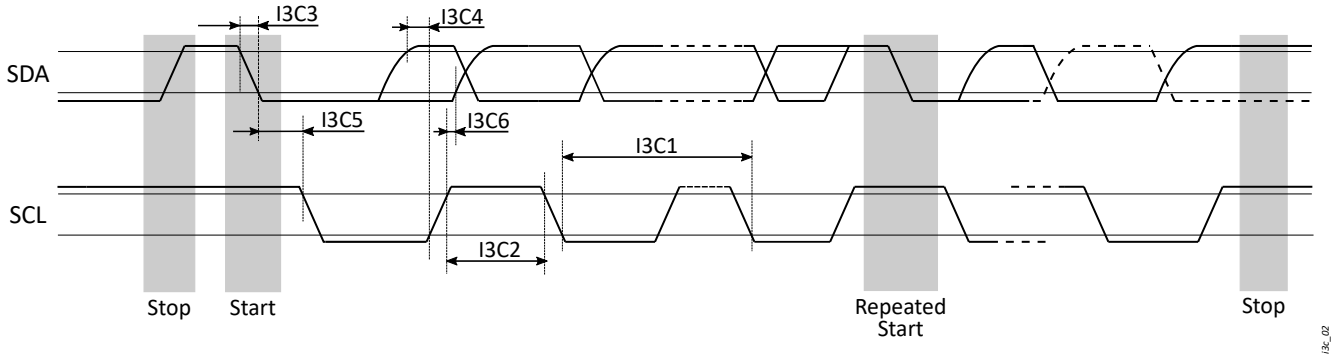
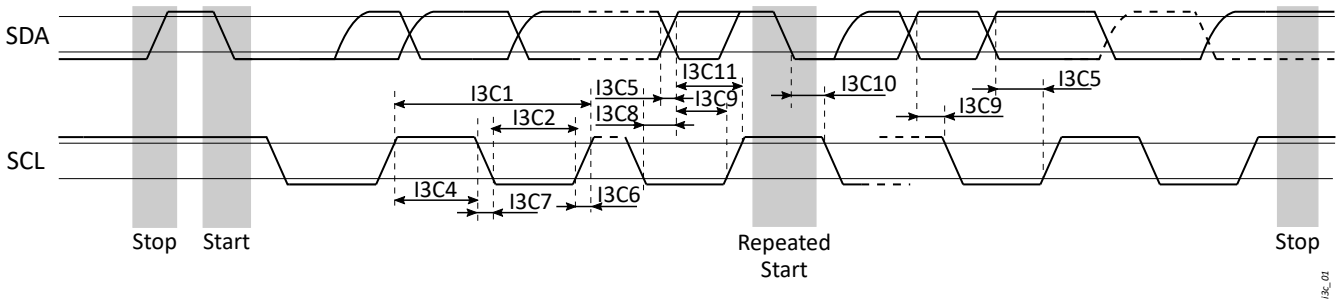


Figure 5-8 I3C Push-Pull Timing Diagram



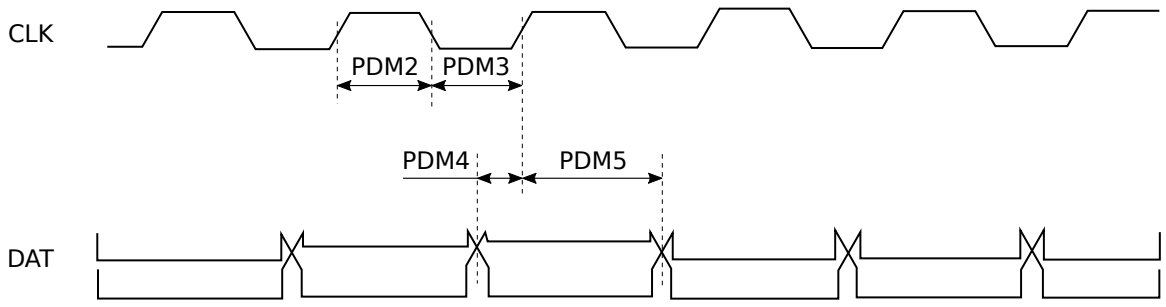
5.7.3.5 PDM Timing Characteristics

Table 5-32 and Figure 5-9 present the PDM timing characteristics.

Table 5-32 PDM Timing Characteristics

No	Parameter		Min	Typ	Max	Unit
	f_{OP}	Operating frequency, PDM_CLK	0.128		4.8	MHz
PDM2	$t_{W_CLK_H}$	Pulse duration, CLK high		48.4		% of total f_{OP} period
PDM3	$t_{W_CLK_L}$	Pulse duration, CLK low		48.4		% of total f_{OP} period
PDM4	t_{SU_DAT}	Setup time, DAT	65			ns
PDM5	t_{H_DAT}	Hold time, DAT	0			ns

Figure 5-9 PDM Timing Diagram



5.7.3.6 SPI Timing Characteristics

Table 5-33, Figure 5-10, and Figure 5-11 present the SPI timing characteristics.

Table 5-33 SPI Timing Characteristics

No	Parameter			Min	Typ	Max	Unit
SP1	t_{c_SCLK}	Cycle time, SCLK	SPI	25			ns
			LPSPI	50			ns
SP2	t_{R_SCLK}	Rise time, SCLK				3	ns
SP3	t_{F_SCLK}	Fall time, SCLK				3	ns
SP4	t_{pd_CLK-L}	Pulse duration, SCLK low		0.45 × t_{c_SCKL}			ns
SP5	t_{pd_CLK-H}	Pulse duration, SCLK high		0.45 × t_{c_SCKL}			ns
SP6	t_{s_SS}	Setup time, SS				3	ns
SP7	t_{h_SS}	Hold time, SS		0.5	0.6	0.8	ns
SP8	$t_{s_MISO_SCLK}$	Setup time, MISO to SCLK		3			ns
SP9	$t_{h_MISO_SCLK}$	Hold time, MISO to SCLK		3			ns
SP10	$t_{d_MOSI_SS}$	Delay time, MOSI to SS		3			ns
SP11	$t_{d_MOSI_SCLK}$	Delay time, MOSI to SCLK		3			ns

Figure 5-10 SPI Receive Timing Diagram

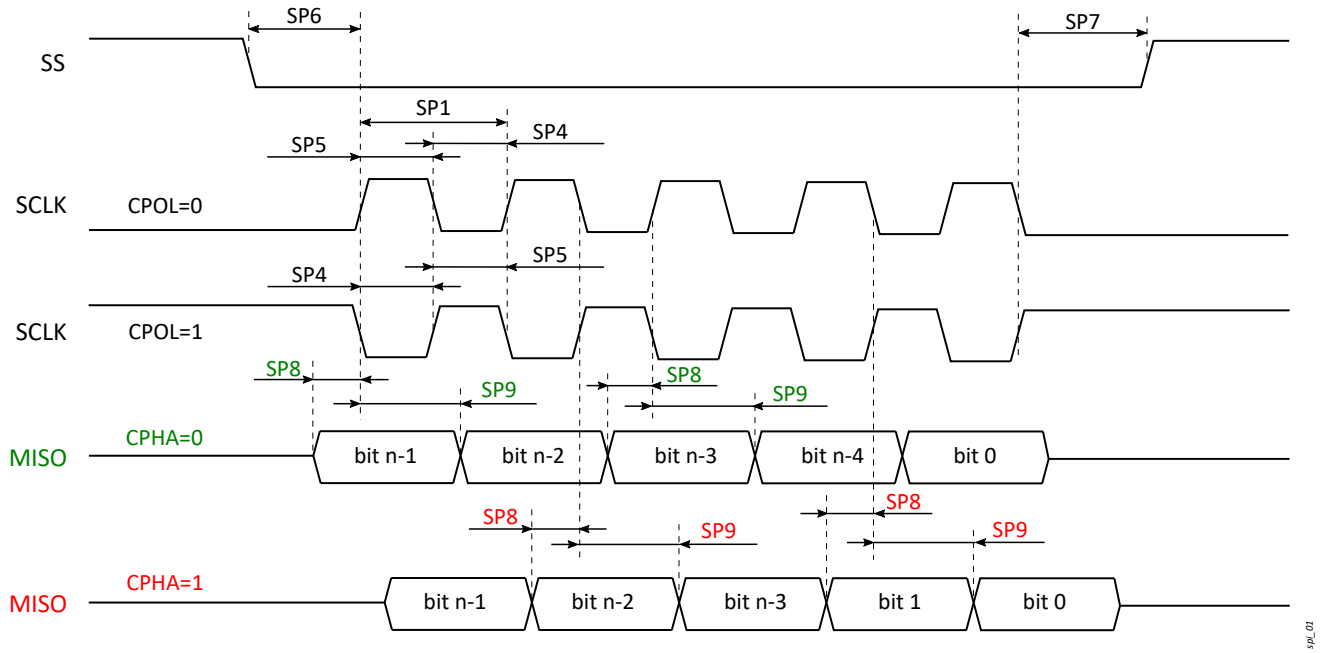
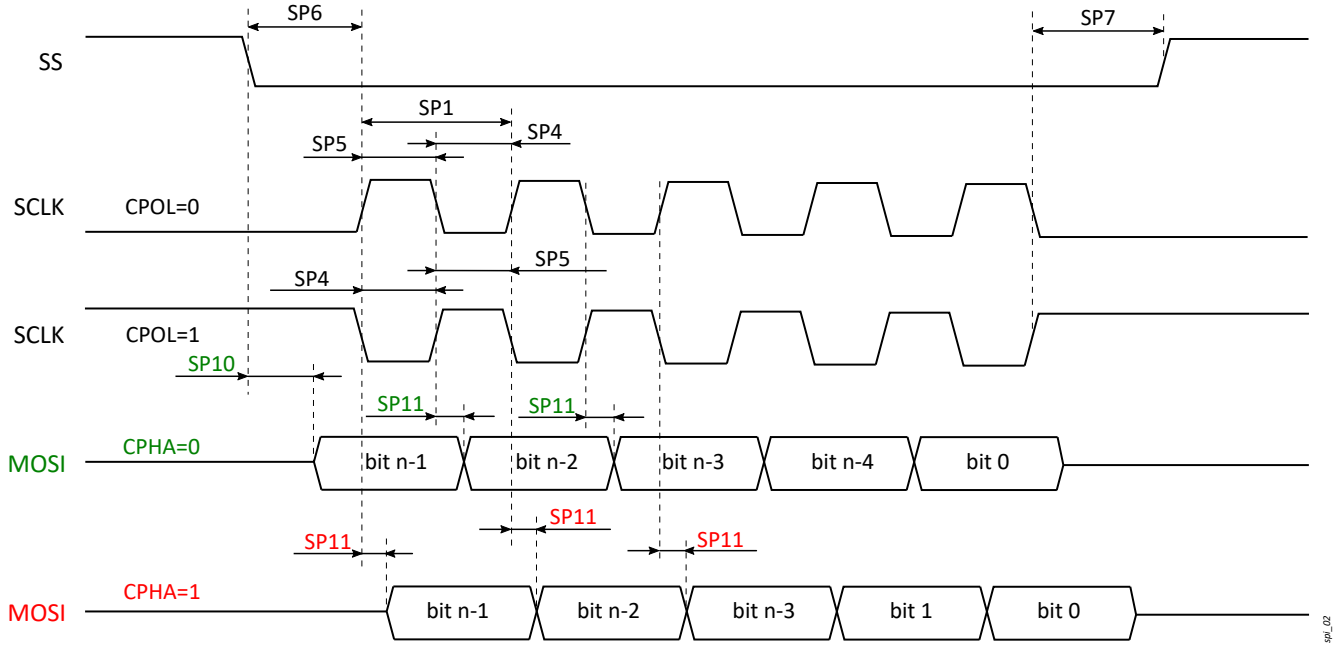


Figure 5-11 SPI Transmit Timing Diagram



5.7.3.7 UART Timing Characteristics

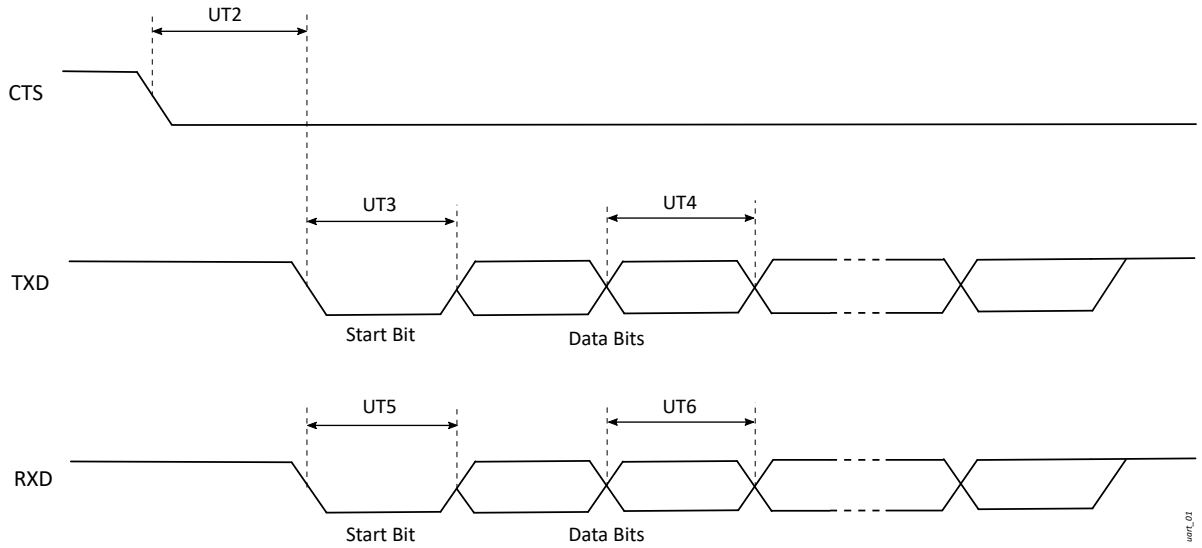
Table 5-34 and Figure 5-12 present the UART timing characteristics.

Table 5-34 UART Timing Characteristics

No	Parameter		Mode	Min	Max	Unit
	$f_{(baud)}$	Maximum programmable baud rate			2.5	Mbps
UT2	$t_{d_CTS_ST_TX}$	Delay time, receive CTSn low to start bit low		100	200	ns
UT3	$t_{pd_ST_TX}$	Pulse duration, transmit start bit, low		400	400	ns

No	Parameter		Mode	Min	Max	Unit
UT4	$t_{pd_DAT_TX}$	Pulse duration, transmit data bit, high or low		400	400	ns
UT5	$t_{pd_ST_RX}$	Pulse duration, receive start bit, low		400	400	ns
UT6	$t_{pd_DAT_RX}$	Pulse duration, receive data bit, high or low		400	400	ns

Figure 5-12 UART Timing Diagram



5.7.3.8 USB Timing Characteristics

The USB interface timing characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

5.7.4 External Memory Interfaces

5.7.4.1 OSPI Timing Characteristics

Table 5-35, Figure 5-13, Figure 5-14, and Figure 5-15 present the OSPI timing characteristics.

Table 5-35 OSPI Timing Characteristics

No	Parameter			Min	Typ	Max	Unit
OSPI Common Parameters							
	f_{op}	Operating frequency				80	MHz
O2	t_{c_CLK}	Cycle time, CLK				12.5	ns
O3	t_{pd_CLK-H}	Pulse duration, CLK high		0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	ns
O4	t_{pd_CLK-L}	Pulse duration, CLK low		0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	0.45 × t_{c_CKL}	ns
O5	t_{R_CLK}	Rise time, CLK				0.05 × t_{c_CKL}	ns
O6	t_{F_CLK}	Fall time, CLK				0.05 × t_{c_CKL}	ns
O7	$t_{s_DATA_IN}$	Setup time, DATA input		3			ns
O8	$t_{h_DATA_IN}$	Hold time, DATA input		0.5	0.6	0.8	ns
O9	$t_{d_DATA_OUT}$	Delay time, DATA output		1.45	1.8	2.375	ns
O10	$t_{h_DATA_OUT}$	Hold time, DATA output		0			ns
OSPI Specific Parameters (@ f_{op} = 80 MHz)							
O11	t_{RXD_DLY} (1)	DATA input delay	Pin set B	0.57	1.35	1.77	ns

No	Parameter			Min	Typ	Max	Unit
		(compared to RXDS line)					
O12	t_{RXDS_DLY} (1)	Programmable RXDS line delay to compensate for t_{RXD_DLY}		$t_{RXD_DLY_min}$ + 0.25 × 1/f_{op}	$t_{RXD_DLY_typ}$ + 0.25 × 1/f_{op}	$t_{RXD_DLY_max}$ + 0.25 × 1/f_{op}	ns

1. The OSPI data input lines are being delayed inside the device compared to the RXDS data strobe line. A programmable delay should be added to the RXDS line itself to overcome the delay of the data input lines. The objective is to ensure that the RXDS line is delayed by ¼ OSPI clock cycle with respect to the leading edge of the valid data lines. For more information on the programming of the RXDS line delay, refer to Section *OSPI Read Data Strobe Signal (OSPI_RXDS)* within Chapter *Cryptographic Octal SPI (OSPI)* of the device series-specific HWRM.

Figure 5-13 OSPI Timing Diagram - SDR Mode

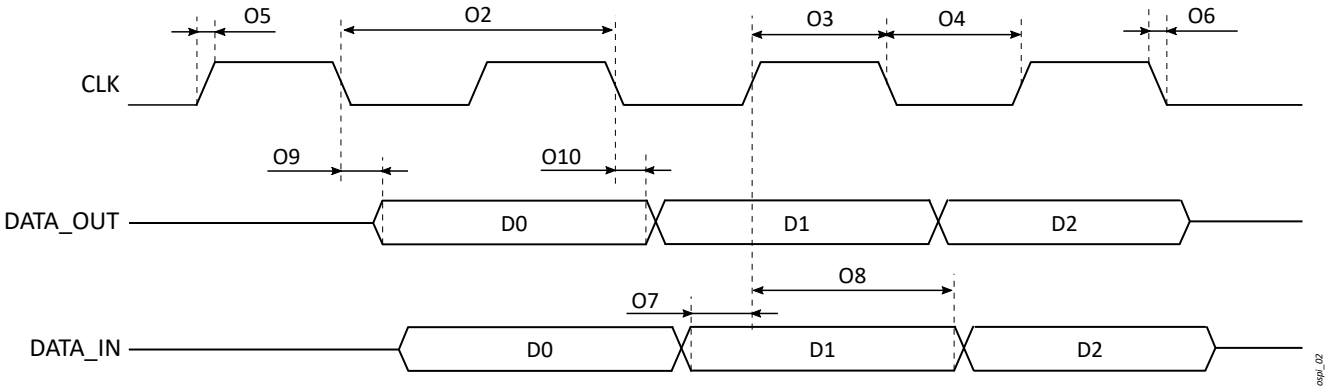


Figure 5-14 OSPI Timing Diagram - DDR Mode (Transmit)

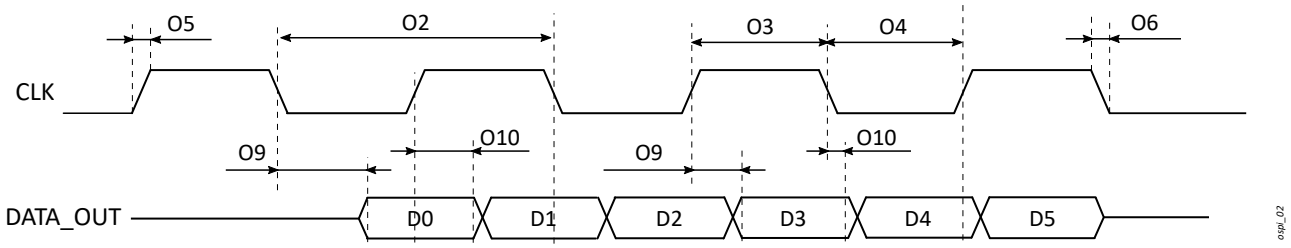
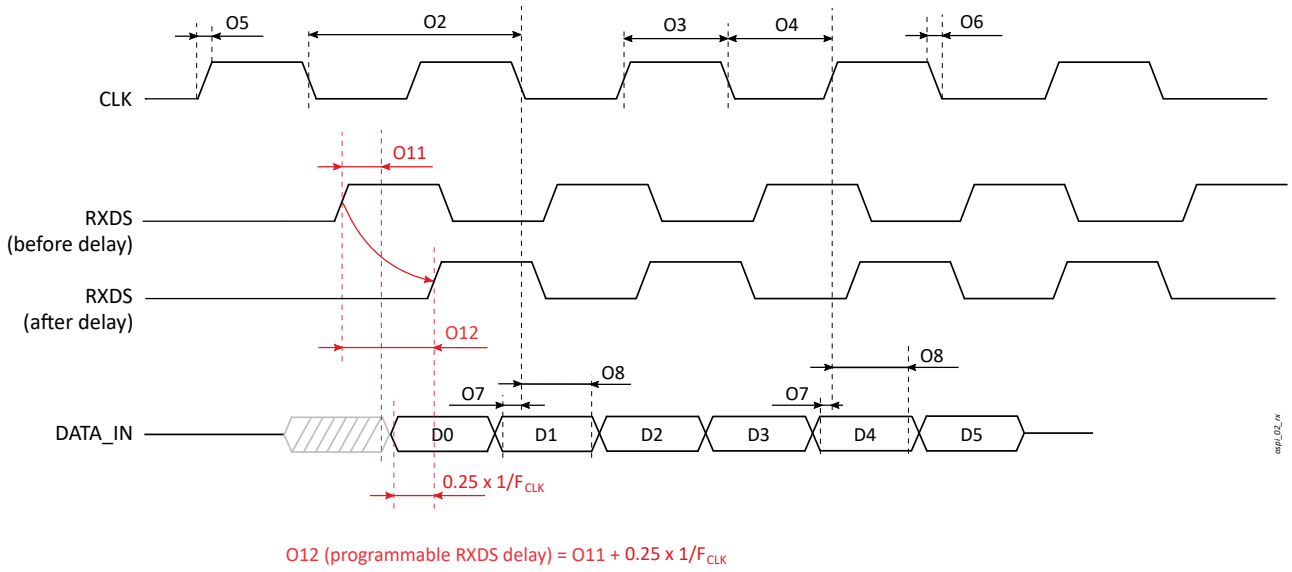


Figure 5-15 OSPI Timing Diagram - DDR Mode (Receive)



O12 (programmable RXDS delay) = O11 + 0.25 x $1/F_{CLK}$

5.7.4.2 SDMMC Timing Characteristics

Table 5-36 and Figure 5-16 present the SDMMC timing characteristics in DS mode.

Table 5-36 SDMMC Timing Characteristics (DS mode)

No	Parameter		Min	Max	Unit
DS1	t_{C_CLK}	Cycle time, CLK		50	ns
DS2	t_{R_CLK}	Rise time, CLK		10	ns
DS3	t_{F_CLK}	Fall time, CLK		10	ns
	D_{C_CLK}	Duty cycle	45	55	%
DS5	$t_{s_CMD_CLK}$	Setup time, CMD valid before CLK rising edge	11.7		ns
DS6	$t_{h_CMD_CLK}$	Hold time, CMD valid after CLK rising edge	8.3		ns
DS7	$t_{s_DATA_CLK}$	Setup time, DATA valid before CLK rising edge	11.7		ns
DS8	$t_{h_DATA_CLK}$	Hold time, DATA valid after CLK rising edge	8.3		ns

Figure 5-16 SDMMC Timing Diagram (DS mode)

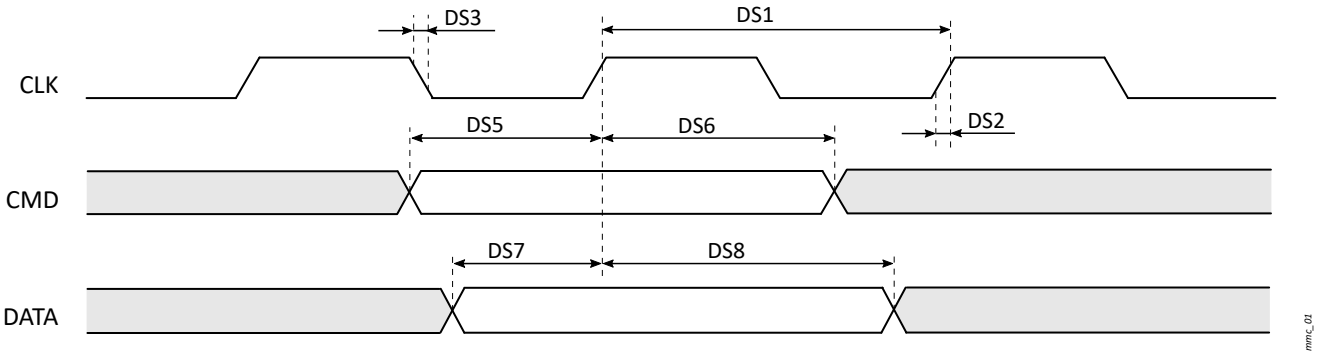


Table 5-37 and Figure 5-17 present the SDMMC timing characteristics in HS mode.

Table 5-37 SDMMC Timing Characteristics (HS mode)

No	Parameter		Min	Max	Unit
HS1	t_{c_CLK}	Cycle time, CLK		25	ns
HS2	t_{R_CLK}	Rise time, CLK		3	ns
HS3	t_{F_CLK}	Fall time, CLK		3	ns
	D_{C_CLK}	Duty cycle	45	55	%
HS5	$t_{s_CMD_CLK}$	Setup time, CMD valid before CLK rising edge	6.3		ns
HS6	$t_{h_CMD_CLK}$	Hold time, CMD valid after CLK rising edge	2.5		ns
HS7	$t_{s_DATA_CLK}$	Setup time, DATA valid before CLK rising edge	6.3		ns
HS8	$t_{h_DATA_CLK}$	Hold time, DATA valid after CLK rising edge	2.5		ns

Figure 5-17 SDMMC Timing Diagram (HS mode)

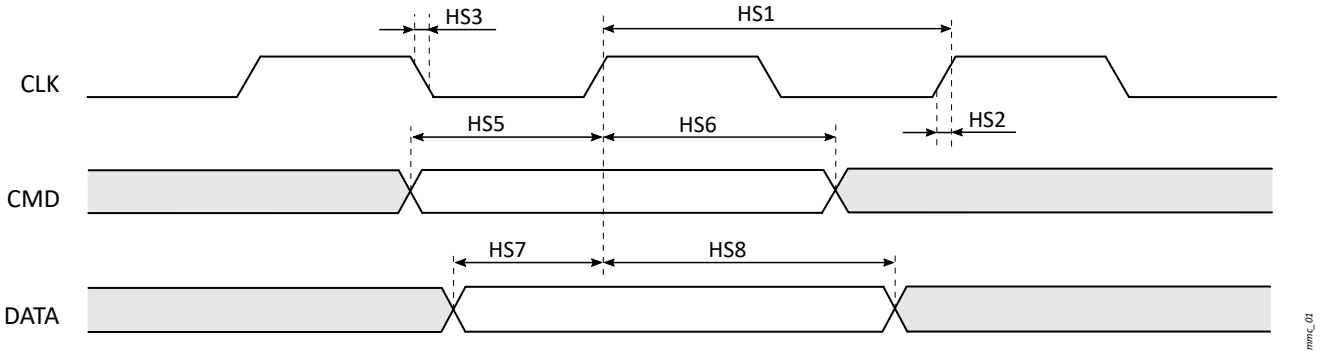
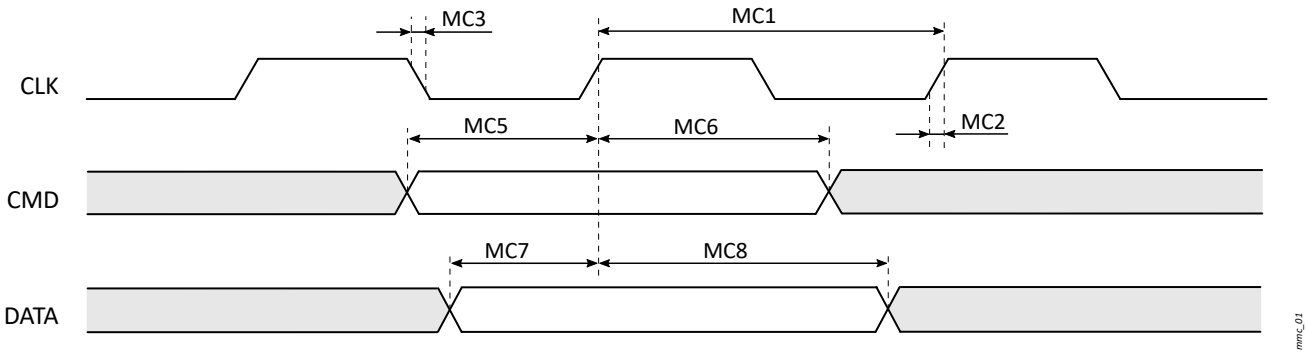


Table 5-38 and Figure 5-18 present the SDMMC timing characteristics in SDR12/SDR25 modes.

Table 5-38 SDMMC Timing Characteristics (SDR12/SDR25)

No	Parameter		Mode	Min	Max	Unit
MC1	t_{c_CLK}	Cycle time, CLK	SDR12		50	ns
			SDR25		25	ns
MC2	t_{R_CLK}	Rise time, CLK			3	ns
MC3	t_{F_CLK}	Fall time, CLK			3	ns
	D_{C_CLK}	Duty cycle		45	55	%
MC5	$t_{s_CMD_CLK}$	Setup time, CMD valid before CLK rising edge	SDR12	3		ns
			SDR25	3		ns
MC6	$t_{h_CMD_CLK}$	Hold time, CMD valid after CLK rising edge	SDR12	0.8		ns
			SDR25	0.8		ns
MC7	$t_{s_DATA_CLK}$	Setup time, DATA valid before CLK rising edge	SDR12	3		ns
			SDR25	3		ns
MC8	$t_{h_DATA_CLK}$	Hold time, DATA valid after CLK rising edge	SDR12	0.8		ns
			SDR25	0.8		ns

Figure 5-18 SDMMC Timing Diagram (SDR12/SDR25)



5.7.5 Camera Interfaces

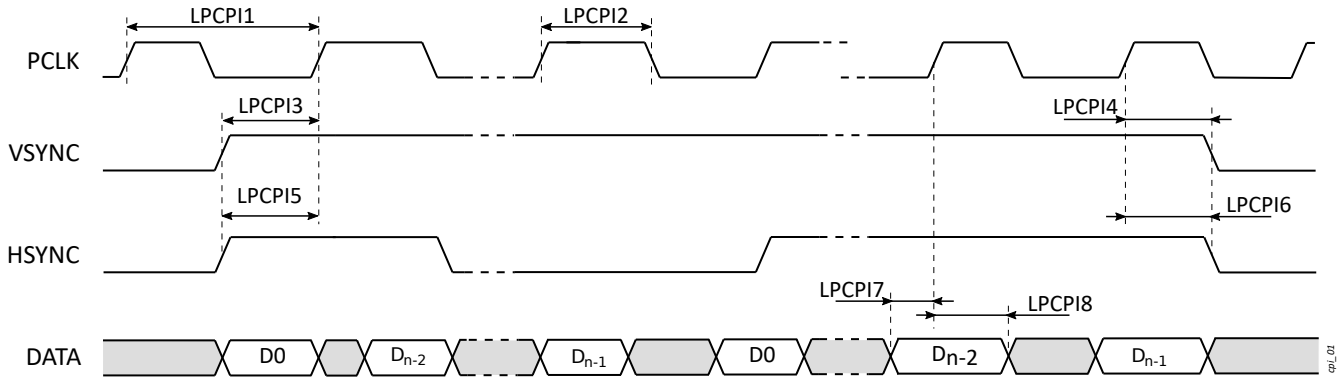
5.7.5.1 LPCPI Timing Characteristics

Table 5-39 and Figure 5-19 present the LPCPI timing characteristics.

Table 5-39 LPCPI Timing Characteristics

No	Parameter		Min	Max	Unit
LPCPI1	t_{c_MCLK}	Cycle time, PCLK	16.7		ns
LPCPI2	t_{pd_MCLK}	Pulse duration, PCLK	8.33		ns
LPCPI3	$t_{s_VSYNC_PCLK}$	Setup time, input vertical sync VSYNC valid before PCLK	3		ns
LPCPI4	$t_{h_VSYNC_PCLK}$	Hold time, input vertical sync VSYNC valid after PCLK	3		ns
LPCPI5	$t_{s_HSYNC_PCLK}$	Setup time, input horizontal sync HSYNC valid before PCLK	3		ns
LPCPI6	$t_{h_HSYNC_PCLK}$	Hold time, input horizontal sync HSYNC valid after PCLK	3		ns
LPCPI7	$t_{s_DATA_PCLK}$	Setup time, input DATA valid before PCLK	5		ns
LPCPI8	$t_{h_DATA_PCLK}$	Hold time, input DATA valid after PCLK	5		ns

Figure 5-19 LPCPI Timing Diagram



5.7.6 Display Interfaces

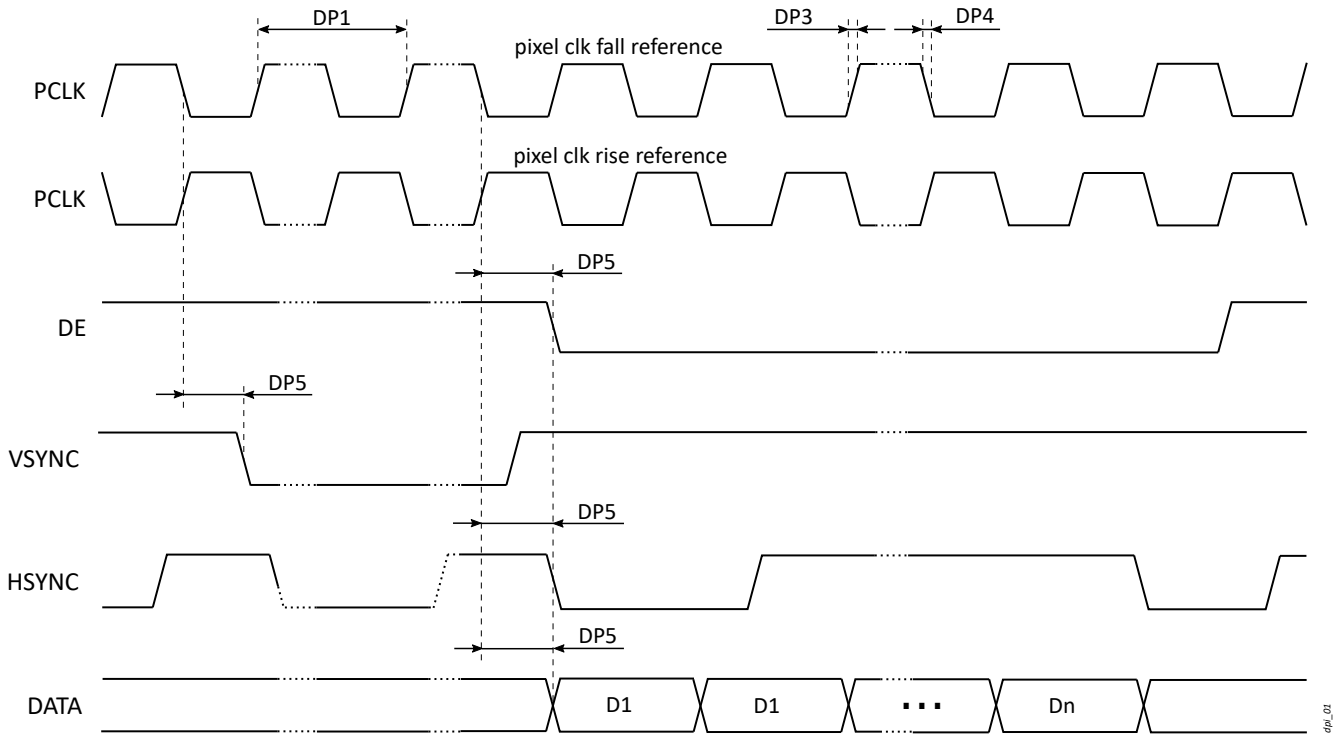
5.7.6.1 DPI Timing Characteristics

Table 5-40 and Figure 5-20 present the DPI timing characteristics.

Table 5-40 DPI Timing Characteristics

No	Parameter		Min	Max	Unit
DP1	t_c	Cycle time	20		ns
	D_{C_CLK}	Duty cycle, PCLK	40	60	%
DP3	t_{R_CLK}	Rise time, PCLK		1	ns
DP4	t_{F_CLK}	Fall time, PCLK		1	ns
DP5	$t_{d_all_to_CLK}$	Delay time, DE, VSYNC, HSYNC, DATA signals to PCLK	5		ns

Figure 5-20 DPI Timing Diagram



5.7.6.2 DSI Timing Characteristics

The DSI interface timing characteristics are compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.2, and MIPI Alliance Specification for D-PHY, Version 1.2.

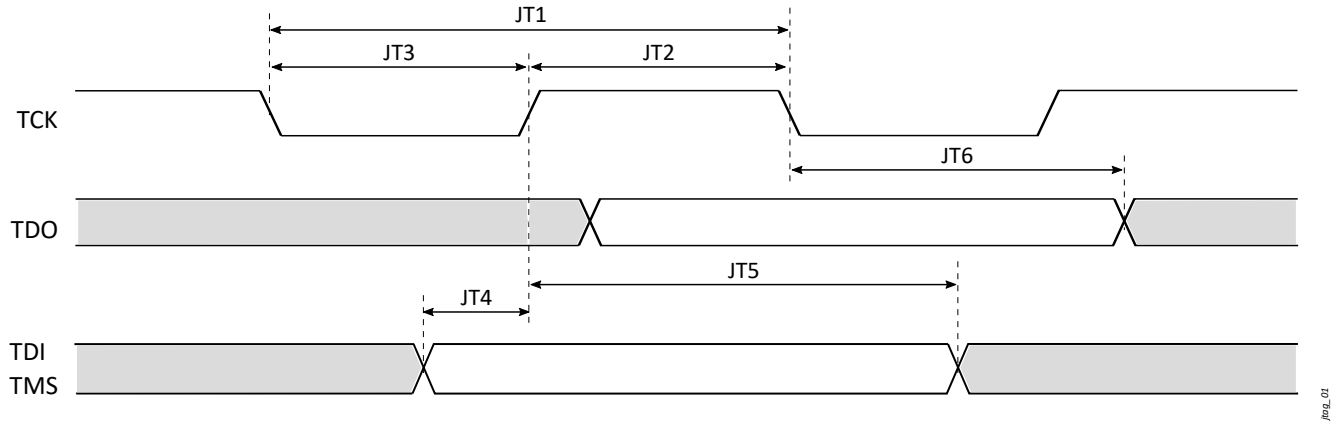
5.7.7 Debug Interface

Table 5-41 and Figure 5-21 present the JTAG timing characteristics.

Table 5-41 JTAG Timing Characteristics

No	Parameter		Min	Max	Unit
JT1	t_c	Cycle time, TCK	50	100	ns
JT2	$t_{pd_TCK\text{-}H}$	Pulse duration, TCK high	24	49	ns
JT3	$t_{pd_TCK\text{-}L}$	Pulse duration, TCK low	24	49	ns
JT4	$t_{s_TDI/TMS\text{-}TCK}$	Setup time, TDI/TMS valid before TCK rising edge	7	7	ns
JT5	$t_{h_TDI/TMS\text{-}TCK}$	Hold time, TDI/TMS valid after TCK rising edge	7	7	ns
JT6	t_{d_TDO}	Delay time, TDO valid after TCK falling edge	7	7	ns

Figure 5-21 JTAG Timing Diagram



6 Package Information

6.1 Device Marking Definition

Figure 6-1 and Figure 6-2 present the top marking reference view.

Figure 6-1 WLCSP Device Top Marking Reference

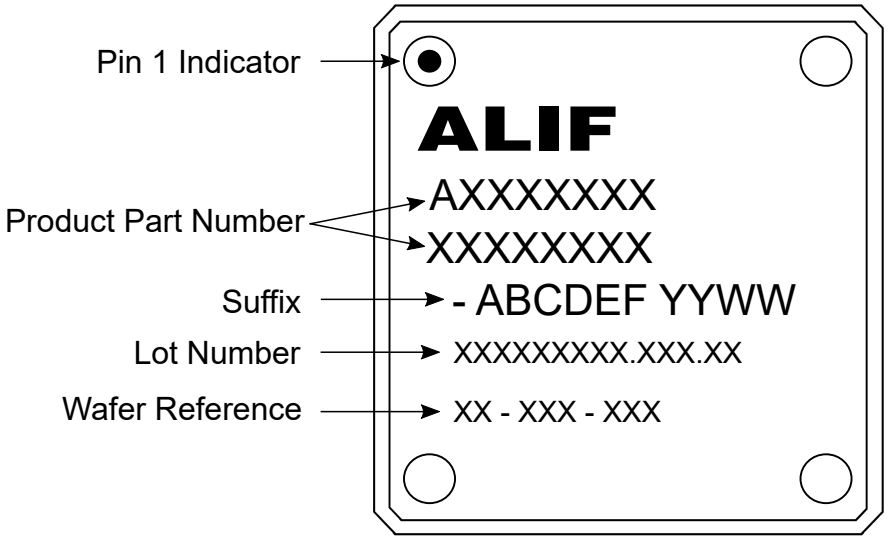


Figure 6-2 FBGA Device Top Marking Reference

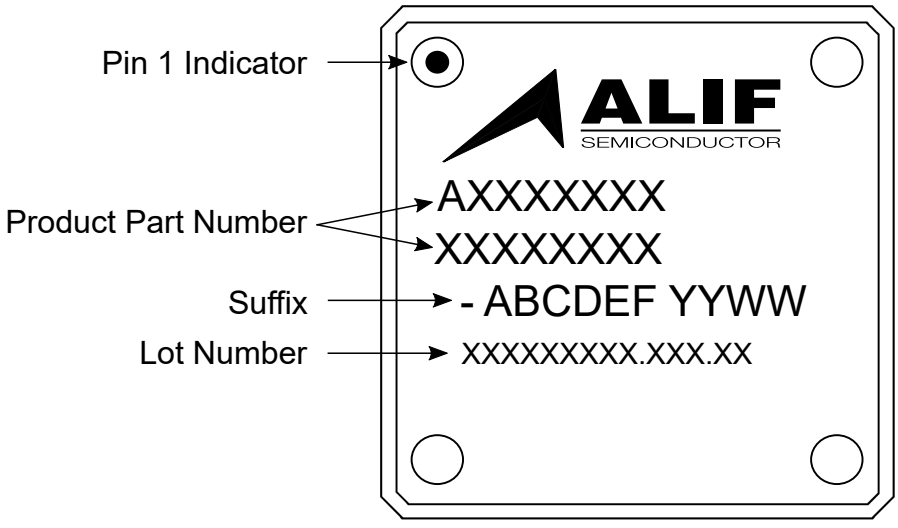


Table 6-1 presents the part number decoding for all Alif Semiconductor's product series.

Table 6-1 Product Identification

Example Part Number:	A	E	1	C	1	F	4	0	5	19	20	P	H	0
Device Manufacturer														
A - Alif Semiconductor														
Device Family														
B - BLE-connected embedded microcontrollers														
E - Ensemble, embedded processors														
Device Series														
0 - Service MCU														
1 - Efficiency MCU														
3/4 - Performance MCU														
5/6 - Fusion processor MCU/MPU														
7/8 - Extreme fusion processor MCU/MPU														
Number of Application Processing Cores / Single Core Product Designator														
0 - Zero cores														
1 - One cores														
2 - Two cores														
C - Compact														
Number of Real Time Processing Cores														
0 - Zero cores														
1 - One cores														
2 - Two cores														
Security Attribute														
B - Basic security														
F - Full security, complete life cycle management														
Machine Learning and AI Capability														
0 - Hardware Acceleration for AI/ML														
1 - MCU Vector Extension (Helium)														
4 - Single Neural Processing Unit (Ethos-U55) + MCU Vector Extension (Helium)														
8 - Dual Neural Processing Units (Ethos-U55) + MCU Vector Extension (Helium)														
9 - Dual Neural Processing Units (Ethos-U55 and Ethos-U85) + MCU Vector Extension (Helium)														
A - Triple Neural Processing Units (2× Ethos-U55 and Ethos-U85) + MCU Vector Extension (Helium)														
Wireless Capability														
0 - No wireless														
M - BLE + IEEE 802.15.4														
Peripheral Set														
0 through 9, A through Z = Level of peripheral selection mix, higher is typically more peripherals														
On-Chip Application MRAM Size														
MRAM memory size in MB														
1st digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB														
2nd digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB														

Example Part Number:	A	E	1	C	1	F	4	0	5	19	20	P	H	0
On-Chip Application SRAM Size														
SRAM memory size in MB														
1st digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB														
2nd digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB														
Package Type and Pin Count														
A - WLCSP208, 0.5 mm pitch														
B - WLCSP216, 0.4 mm pitch														
H - WLCSP120, 0.35 mm pitch														
L - FBGA194, 0.5 mm pitch														
P - FBGA120, 0.5 mm pitch														
Operating Temperature														
S - Standard (see Section 5.2.1 General Operating Conditions)														
E - Extended (see Section 5.2.1 General Operating Conditions)														
H - Industrial (see Section 5.2.1 General Operating Conditions)														
Product Revision														
0 or Blank - Original version of product														

Table 6-2 presents the Suffix (characters after main part number) decoding.

Table 6-2 Suffix Definition

Position	Description
A	ID
B	ID revision
C	Firmware version
D	Fab site. D = Dresden
E	Final assembly site. M = Malaysia, K = South Korea
F	Final test site. S = Singapore, E = USA
Space	
Y	Calendar year of device production
Y	
W	Work week of device production
W	

6.2 Package Specifications

6.2.1 WLCSP120 Package Information

6.2.1.1 WLCSP120 Thermal Operating Specifications

Table 6-3 provides thermal operating specifications for WLCSP120 package.

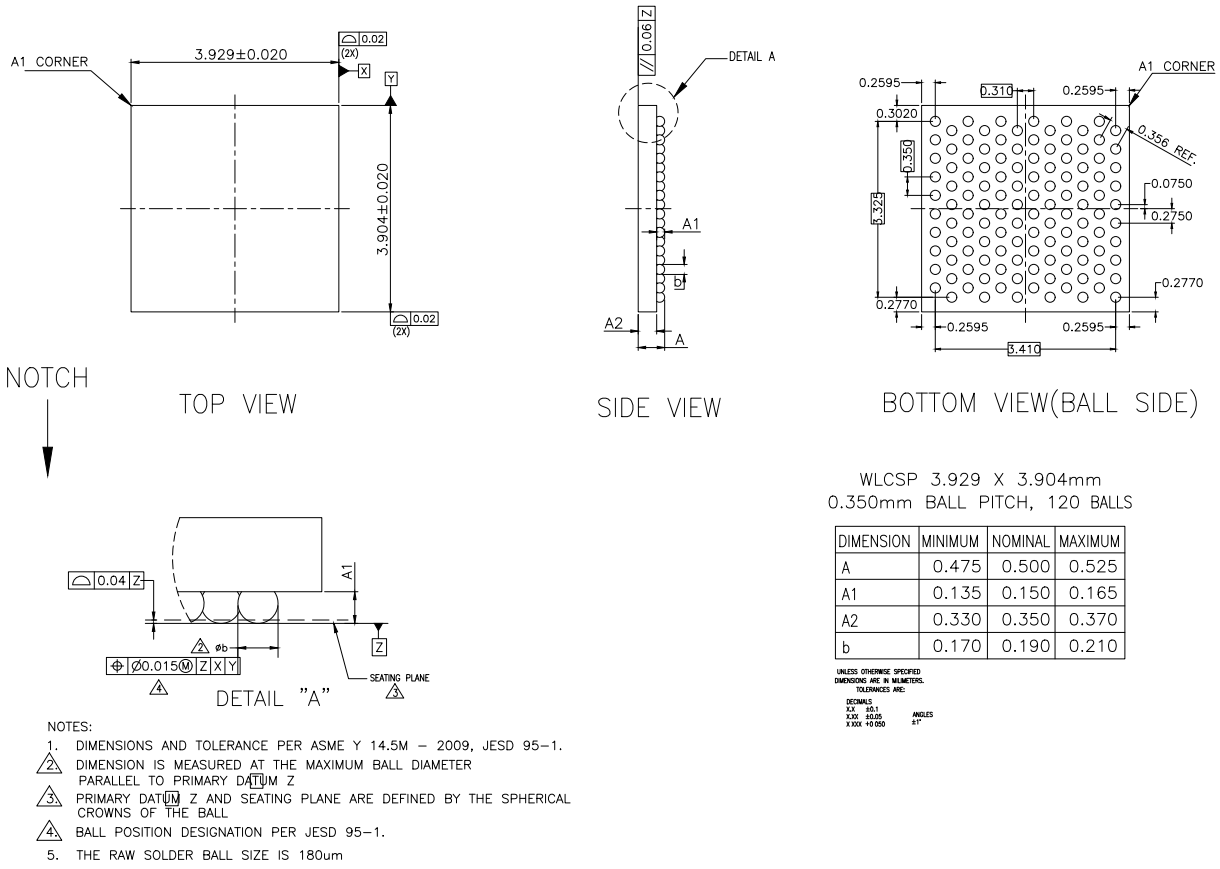
Table 6-3 WLCSP120 Thermal Operating Specifications

Parameter		Value	Unit
$R\theta_{JA}$	Thermal resistance in natural convection (junction-to-free air)	32.55	°C/W
$R\theta_{JC}$	Thermal resistance (junction-to-case)	0.11	°C/W
Ψ_{JT}	Thermal characterization parameter (junction-to-package top)	0.095	°C/W

6.2.1.2 WLCSP120 Package Outline

Figure 6-3 presents WLCSP120 package outline.

Figure 6-3 WLCSP120 Package Outline (1)



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.475	0.500	0.525
A1	0.135	0.150	0.165
A2	0.330	0.350	0.370
b	0.170	0.190	0.210

1. All linear dimensions are in millimeters.

Figure 6-4 WLCSP120 Bump Distance from Cut Edge

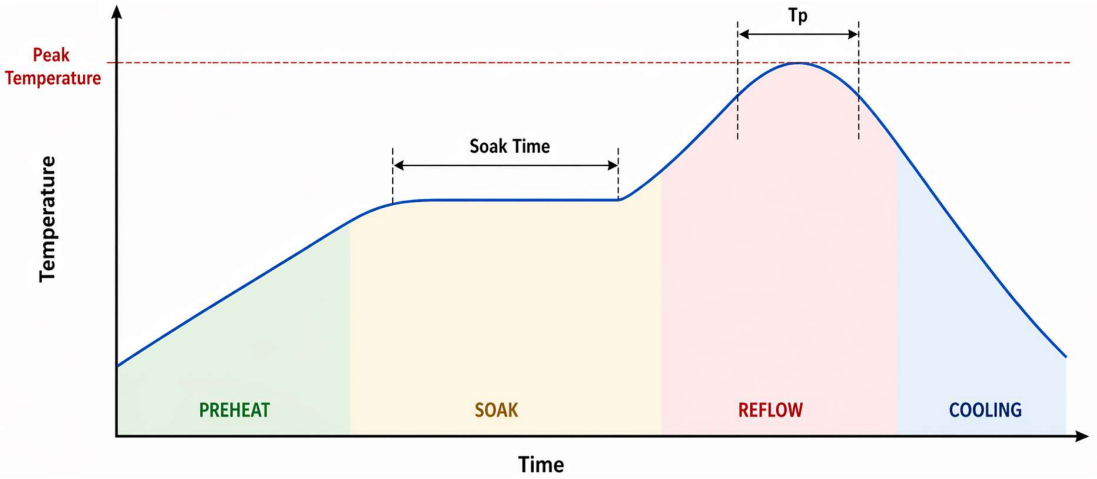
NOTE

This section is under development but is included as a placeholder for future updates.

6.2.1.3 WLCSP120 Solder Reflow Profile

The device is compliant with the IPC/JEDEC joint industry standard: J-STD-020F. The recommended solder reflow profile for this package is shown in Figure 6-5 and follows the guidelines defined in Section 8.6 of the standard.

Figure 6-5 WLCSP120 Solder Reflow Profile



Item	Parameter	Setting	Unit
1	Peak Temperature	235 – 255	°C
2	Reflow Time T_P (< 217 °C)	60 – 90	s
3	Soak Time (150 – 180 °C)	60 – 90	s

6.2.2 FBGA120 Package Information

6.2.2.1 FBGA120 Thermal Operating Specifications

Table 6-4 provides thermal operating specifications for FBGA120 package.

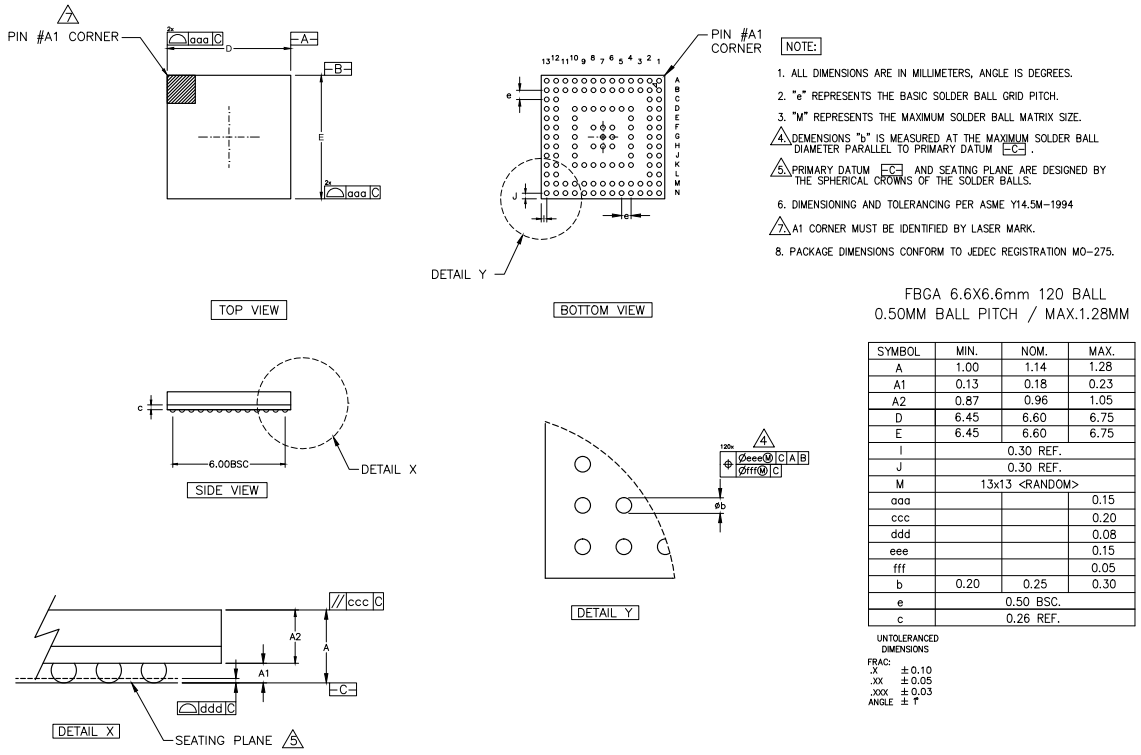
Table 6-4 FBGA120 Thermal Operating Specifications

Parameter		Value	Unit
θ_{JA}	Thermal resistance in natural convection (junction-to-free air)		°C/W
θ_{JC}	Thermal resistance (junction-to-case)		°C/W
Ψ_{JT}	Thermal characterization parameter (junction-to-package top)		°C/W

6.2.2.2 FBGA120 Package Outline

Figure 6-6 presents FBGA120 package outline.

Figure 6-6 FBGA120 Package Outline (1)



SYMBOL	MIN.	NOM.	MAX.
A	1.00	1.14	1.28
A1	0.13	0.18	0.23
A2	0.87	0.96	1.05
D	6.45	6.60	6.75
E	6.45	6.60	6.75
I		0.30 REF.	
J		0.30 REF.	
M		13x13 <RANDOM>	
aaa			0.15
ccc			0.20
ddd			0.08
eee			0.15
fff			0.05
b	0.20	0.25	0.30
e		0.50 BSC.	
c		0.26 REF.	

1. All linear dimensions are in millimeters.

6.2.2.3 FBGA120 Solder Reflow Profile

Please refer to the IPC/JEDEC joint industry standard: J-STD-020F, section 8.6 for the recommended solder reflow time and temperature profile for this package.

6.3 Storage Conditions

Table 6-5 defines specifics in the storage conditions.

Table 6-5 Storage Conditions

Parameter			Min	Max	Unit
T_{STG}	Storage temperature		-40	150	°C
%RH	Relative Humidity	WLCSP package: MSL1 (Moisture Sensitivity Level)			
		FBGA package: MSL3			

7 Ordering Information

Table 7-1 presents the optional features for each orderable part number.

Table 7-1 Orderable Part Numbers

Part Number[3]	NPU-HE	GPU2D	CANFD	CDC	DPI	DSI	MRAM	SRAM	GPIO (1.8 V)	Package	Operating Temperature
AE1C1F4051920PH0	Yes	1	2	1	1	1	1.9MB	2MB	68[2]	FBGA120	Industrial
AE1C1F4051920HH0	Yes	1	2	1	No	1	1.9MB	2MB	60[1]	WLCSP120	Industrial
AE1C1F1041010PH0	No	No	No	No	No	No	1MB	1MB	68[2]	FBGA120	Industrial
AE1C1F1041010HH0	No	No	No	No	No	No	1MB	1MB	60[1]	WLCSP120	Industrial
AE1C1F1040505PH0	No	No	No	No	No	No	0.5MB	0.5MB	68[2]	FBGA120	Industrial
AE1C1F1040505HH0	No	No	No	No	No	No	0.5MB	0.5MB	60[1]	WLCSP120	Industrial

1. GPIO[0-7], GPIOV_1, See Table 3-12 GPIO Signal Descriptions
2. GPIO[0-8], GPIOV_1, See Table 3-12 GPIO Signal Descriptions
3. Ordering designation for shipment packaging:
   - Add the following suffix to base part number:
     - -T, for Tape and Reel
     - -Y, for Tray
   - Example: AE1C1F4051920PH0-T is Tape and Reel

Table 7-2 shows the user SRAM banks with their corresponding sizes (in KB) available for each part number.

Table 7-2 Part Numbers SRAM Breakdown

Part Number	Total SRAM (KB)	SRAM0 (M55-HE ITCM) (KB)	SRAM1 (M55-HE DTCM) (KB)
AE1C1F4051920PH0	2048	512	1536
AE1C1F4051920HH0	2048	512	1536
AE1C1F1041010PH0	1024	512	512
AE1C1F1041010HH0	1024	512	512
AE1C1F1040505PH0	512	256	256
AE1C1F1040505HH0	512	256	256

For complete part number decoding, see Section 6.1 Device Marking Definition.

8 Legal and Support Information

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8.2 Related Documents and Tools

- Alif Semiconductor device series-specific Hardware Reference Manual (HWRM)
- Alif Semiconductor Software Reference Manual (SWRM)

For additional Alif Semiconductor technical documentation and software resources please visit:

- User Guides & App Notes
- Software & Tools

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the Alif Conductor tool.

8.3 Contact Information

For more information visit our website Alif Semiconductor or contact us:

contact@alifsemi.com

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8.5 Acronyms

3

3GPP
3rd Generation Partnership Project

A

ACP
Accelerator Coherency Port

ADC
Analog to Digital Converter

AES
Advanced Encryption Standard

AHI
Application Host Interface

AI
Artificial Intelligence

aiPM
autonomous intelligent Power Management

AON
Always On

API
Application Programming Interface

APSS
Application Processor Subsystem

ATOC
Application Table of Content

B

BER
Bit-Error Ratio

BLE
Bluetooth Low Energy

BLIT
Block Image Transfers

BOD
Brown-Out Detect

BOR
Brown-Out Reset

BPU
Breakpoint Unit

C

CAN
Controller Area Network

CANFD
Controller Area Network with Flexible Data rate

CCC
Common Command Code

CDC
Configurable DPI Controller

CDM
Charged Device Model

CLUT
Color Look-Up Table

CMP
Comparator

CMSIS
Common Microcontroller Software Interface Standard

CNN
Convolutional Neural Network

CPI
Camera Parallel Interface

CPU
Central Processing Unit

CRC
Cyclic Redundancy Check

CSI
Camera Serial Interface

D

DAC
Digital to Analog Converter

DAP
Debug Access Port

DDR
Double Data Rate

DL
Display List / Download

DLR
Display List Reader

DM
Device Manufacturer

DMA
Direct Memory Access

DMAC
Direct Memory Access Controller

DMIC
Digital Microphone

DPA
Differential Power Analysis

DPI
Display Parallel Interface / Display Pixel Interface

DPU
Data Processing Unit

DRD
Dual-Role Device

DSC
Display Stream Compression

DSI
Display Serial Interface

DTCM
Data Tightly-Coupled Memory

DWT
Data Watchpoint and Trace

E

ECB
Electronic Codebook

ECC
Error-Correcting Code / Elliptic-Curve Cryptography

eDRX
Extended Discontinuous Reception

EMC
Electromagnetic Compatibility

EMFI
Electromagnetic Fault Injection

EMI
Electromagnetic Interference

EMS
Electromagnetic Susceptibility

EOL
End of Life

EoTp
End of Transmission Packet

EPU
Extension Processing Unit

ESD
Electrostatic Discharge

eSIM
Embedded Subscriber Identity Module

ETH
Ethernet

EVTRTR
Event Router

EWIC
External Wakeup Interrupt Controller

F

FC
Firewall Component

FIR
Finite Impulse Response

FSR
Full-Scale Range

G

GIC
Generic Interrupt Controller

GNSS
Global Navigation Satellite Subsystem

GOPS
Giga Operations Per Second

GPIO
General-Purpose Input/Output

GPS
Global Positioning System

GPU
Graphics Processing Unit

H

HBM
Human Body Model

HCI
Host Communication Interface

HDR
High Data Rate

HE
High Efficiency

HFRC
High-Frequency Resistor-Capacitor

HFXO
High-Frequency Crystal Oscillator

HMI
Human Machine Interface

HP
High Performance

HPP
High Performance Point

HUK
Hardware Unique Key

HWRM
Hardware Reference Manual

HWSEM
Hardware Semaphore

I

I2C
Inter-Integrated Circuit

I2S
Inter-IC Sound

I3C
Improved Inter-Integrated Circuit

IBI
In-Band Interrupt

ICMP
Internet Control Message Protocol

ICV
Integration Circuit Vendor

IDE
Integrated Design Environment

IFG
Interframe Gap

IFU
Instruction Fetch Unit

IIR
Infinite Impulse Response

IMD
Intermodulation Distortion

IoT
Internet of Things

IPC
Inter-Process Communication

IPI
Image Pixel Interface

IRQRTR
Interrupt Router

iSIM
Integrated Subscriber Identity Module

ISP
In-System Programming

ITCM
Instruction Tightly-Coupled Memory

iUICC
integrated Universal Integrated Circuit Card

IWIC
Internal Wakeup Interrupt Controller

L

LCD
Liquid Crystal Display

LCS
Life Cycle State

LDE
Lockdown Extension

LDO
Low Drop-Out

LE
Low Energy

LFRC
Low-Frequency Resistor-Capacitor

LFXO
Low-Frequency Crystal Oscillator

LOM
Listen Only Mode

LP
Low-Power

LPCMP
Low-Power Comparator

LPGPIO
Low-Power General-Purpose Input/Output

LPI2C
Low-Power Inter-Integrated Circuit

LPI2S
Low-Power Inter-IC Sound

LPM
Link Power Management

LPP
Low Performance Point

LPPDM
Low-Power Pulse Density Modulation

LPRTC
Low-Power Real-Time Counter

LPSPI
Low-Power Serial Peripheral Interface

LPTIMER
Low-Power Timer

LSB
Least Significant Bit

LTE
Long-Term Evolution

LUT
Look-Up Table

M

MAC
Media Access Controller

MAU
Memory Authentication Unit

MBI
Master Bus Interface

MCU
Microcontroller Unit

ME
Monitor Extension

MHU
Message Handling Unit

ML
Machine Learning

MMU
Memory Management Unit

MPE
Master Permission Entry

MPU
Memory Protection Unit

MRAM
Magnetoresistive Random-Access Memory

MSL
Moisture Sensitivity Level

MTL
MAC Transaction Layer

MVE
M-profile Vector Extension

MWS
Mobile Wireless Standard

N

NMI
Non-Maskable Interrupt

NPP
Nominal Performance Point

NPU
Neural Processing Unit

NPU-HE
Neural Processing Unit-High Efficiency

NPU-HP
Neural Processing Unit-High Performance

NRZ
Non-Return-to-Zero

NS
Non-Secure

NVIC
Nested Vectored Interrupt Controller

NVM
Non-Volatile Memory

O

OCS
OEM-signed Configuration Settings

OEM
Original Equipment Manufacturer

OPP
Operating Performance Point

OSPI
Octal Serial Peripheral Interface

OToC
OEM-signed Table of Contents

OTP
One Time Programmable

P

PCB
Printed Circuit Board

PCM
Pulse Code Modulation

PD
Power Domain

PDM
Pulse Density Modulation

PE
Protection Extension

PLL
Phase-Locked Loop

PMU
Performance Monitoring Unit

POR
Power-On-Reset

PPI
PHY Protocol Interface / Private Peripheral Interrupt

PPS
Precise Positioning Service

PPU
Power Policy Unit

PSC
Power Sequence Controller

PSM
Power Saving Mode

PSRAM
Pseudo-Static Random-Access Memory

PSRR
Power Supply Rejection Ratio

PWM
Pulse Width Modulation

Q

QEC
Quadrature Encoder Counter

R

RAI
Release Assistance Indication

RDC
Receiver Delay Compensation

RF
Radio Frequency

RFI
Radio Frequency Interference

RLE
Run-Length Encoding

RMA
Return Merchandise Authorization

RNN
Recurrent Neural Network

RO
Read Only

ROM
Read Only Memory

RoT
Root-of-Trust

RSA
Rivest–Shamir–Adleman

RSE
Region Size Extension

RSSI
Received Signal Strength Indicator

RSTC
Reset Controller

RTC
Real-Time Counter

RTOS
Real-Time Operating System

RTSS
Real-Time Subsystem

RW
Read/Write

S

SAR
Successive Approximation Register

SAU
Security Attribution Unit

SBI
Slave Bus Interface

SCU
Snoop Control Unit

SDA
Serial Data

SDIO
Secure Digital Input/Output

SDMMC
Secure Digital / Embedded Multimedia Card

SDR
Single Data Rate

SE
Secure Enclave / Secure Enable

SESS
Secure Enclave Subsystem

SFD
Start of Frame Data / Start Frame Delimiter

SGI
Software Generated Interrupt

SHA
Secure Hash Algorithm

SIM
Subscriber Identity Module

SIMD
Single Instruction Multiple Data

SJW
Synchronization Jump Width

SMP
Symmetric Multi-Processing

SNR
Signal-to-Noise Ratio

SPA
Simple Power Analysis

SPI
Serial Peripheral Interface / Shared Peripheral Interrupt

SRAM
Static Random-Access Memory

SSP
Synchronous Serial Protocol

SST
Single Shot Transmission

STB
Store Buffer

STOC
System Table of Content

SWD
Serial Wire Debug

SWRM
Software Reference Manual

T

TCM
Tightly-Coupled Memory

TCP
Transmission Control Protocol

TDC
Transmitter Delay Compensation

TE
Translation Extension

TEE
Trusted Execution Environment

TFT
Thin-Film-Translator

TGU
TCM Gate Unit

TOC
Table of Content

TRNG
True Random Number Generator

TSENS
Temperature Sensor

U

UART
Universal Asynchronous Receiver/Transmitter

UDE
Unprivileged Debug Extension

UDP
User Datagram Protocol

UI
Unit Interval / User Interface

UL
Upload

UPP
Ultra-Low Performance Point

USB
Universal Serial Bus

UTIMER
Universal Timer

V

VTOR
Vector Table Offset Register

W

WDT
Watchdog Timer

WFE
Wait For Event

WFI
Wait For Interrupt

X

XIP
eXecute-in-Place

XO
Execute Only

Z

ZI
Zero Initialized

9 Revision History

Table 9-1 provides the history of changes to this document.

Table 9-1 Revision History

Date	Revision	Changes
September 2026	1.9	Changes from previous revision include: ■ Added table note specifying the minimum VREG_CORE_0V8 output voltage during runtime and updated the caution under Table 3-2 Power Supply Signal Descriptions ■ Updated Notes under Table 3-2 Power Supply Signal Descriptions, Table 5-4 General Operating Conditions, and Figure 5-1 Power-Up/Power-Down Sequencing ■ Updated Table 3-3 CPU State Summary and Table 3-4 Device Power Mode Summary ■ Added Caution specifying the HFXO or external clock source requirements for proper device operation in Section 3.8 Clock Generation and Control ■ Updated note about OSPI limitations in Section 3.17.1 Cryptographic OSPI Overview ■ Removed eMMC feature *Boot operation* and *alternative boot operation* in Section 3.17.2 SDMMC Overview ■ Updated LP Peripherals Power for STBY_1 in Table 5-5 Power Modes Case Definition ■ Added V_{CM} parameter to Table 5-20 ADC24 Electrical Characteristics ■ Editorial enhancements
June 2026	1.8	Changes from previous revision include: ■ Updated Secure Enclave functions in Section Features ■ Updated I2C throughput from 3.4 Mbps to 1.0 Mbps in Section Features, Section 3.16.3 I2C Overview, and Table 5-3 Maximum Performance Ratings ■ Updated Section 3.4.1 Security Architecture Overview ■ Updated Section 3.4.2 Cryptographic Services ■ Added table note (1) under Table 3-2 Power Supply Signal Descriptions and Table 5-4 General Operating Conditions ■ Added Note under Table 3-2 Power Supply Signal Descriptions, Table 5-4 General Operating Conditions, and Figure 5-1 Power-Up/Power-Down Sequencing ■ Updated the AES key length to 128 bits in Section 3.17.1 Cryptographic OSPI Overview ■ Removed HS mode column from Table 5-28 I2C Timing Characteristics ■ Editorial enhancements
April 2026	1.7	Changes from previous revision include: ■ Updated VREG_DIG_1V8 bypass option in note (3) under Table 3-2 Power Supply Signal Descriptions and Table 5-4 General Operating Conditions ■ Updated VREG_AON series resistor value to 1.0 kΩ in note (4) under Table 3-2 Power Supply Signal Descriptions ■ Updated HFXO external crystal frequency information in Section 3.8 Clock Generation and Control ■ Updated descriptions of GO_2, GO_3, and GO_4, and the typical current consumption at 3.3 V of GO_3 in Table 5-5 Power Modes Case Definition ■ Updated Figure 6-3 WLCSP120 Package Outline ■ Updated Section 6.2.1.3 WLCSP120 Solder Reflow Profile ■ Editorial enhancements

Date	Revision	Changes
March 2026	1.6	Changes from previous revision include: ■ Clarified GPIO pin numbers in Table 2-1 Device Features and Peripherals ■ Updated Section 3.20.1 ADC Overview to clarify that ADC12 modules support only one internal input (from TSENS) and it is available only to ADC120 ■ Updated Section 3.20.5 TSENS Overview to clarify that the TSENS input is available only to ADC120 ■ Updated the pin type of MIPIDSI_0_P/N to IO in Table 4-1 Pin Function Options by Location ■ Added Interconnect bus clock parameters for SYST_PCLK, SYST_HCLK, and SYST_ACLK in Table 5-3 Maximum Performance Ratings ■ Added ESR parameter to Table 5-9 External HFXO Clock Source Characteristics ■ Added values in Table 6-3 WLCSP120 Thermal Operating Specifications