ERRATA

ENSEMBLE™ FAMILY
E7 SERIES
EMBEDDED FUSION PROCESSORS

Contents

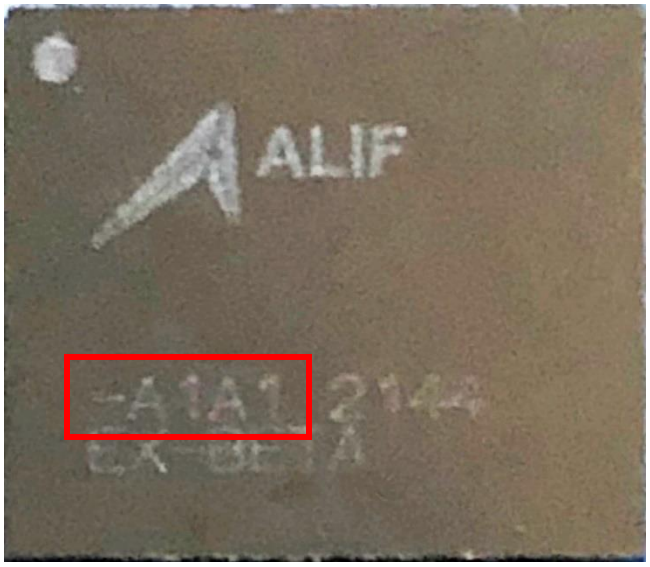
1 Silicon Identification and Scope

This document lists the items in the Ensemble E7 Series revision A1 devices that do not match the production device specification as documented in the datasheet.

Datasheet Reference: **ADTS0005 v1.0**
Silicon Versions: **Ensemble E7 revision A1 Devices**
Device Marking: **see photo below**

Device Version	Family Name	Product Identifier	Suffix
A1 Silicon	Ensemble	AE722xxx	-A1A1

The revision A1 devices are marked with "-A1A1" at the beginning of the next to last row of text on the device below the logo as shown below:



1.1 System Control Limitations

1.1.1 System Control Register Mapping Will Be Different For Production Devices

Datasheet Section Reference: various
Description
A1 2nd Sample Silicon has different address and I/O maps compared to production devices in these areas:

- Peripherals address map
- Pin-Mux map
- System Control registers address map
- Shared Peripherals Interrupt map
- Peripheral DMA Channels map

Application code that directly addresses any of these registers would need to be changed when migrating from sample silicon to production devices.

Workaround for A1 devices
No changes to application code will be necessary when moving to production devices if references and calls to peripherals, I/O pins, and functions are made through CMSIS pack calls.
Address and I/O maps for revision B devices will follow the datasheet specifications.

1.1.2 EROUTER not functional

Datasheet Section Reference: 3.13.4
Description
The Event Router (EROUTER) is not functional.
A select number of peripherals can initiate transactions and output events cannot trigger timer functions. The peripherals below are the ones that can initiate DMA transfers.

DMA0 REQ Assignment (Shared Peripherals)

Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#
UART0 Rx	0	SPI0 Rx	8	I2C0 Rx	16	I2S0 Rx	24
UART0 Tx	1	SPI0 Tx	9	I2C0 Tx	17	I2S0 Tx	25
UART1 Rx	2	SPI1 Rx	10	I2C1 Rx	18	I2S1 Rx	26
UART1 Tx	3	SPI1 Tx	11	I2C1 Tx	19	I2S1 Tx	27
UART2 Rx	4	SPI2 Rx	12	I2C2 Rx	20	I2S2 Rx	28
UART2 Tx	5	SPI2 Tx	13	I2C2 Tx	21	I2S2 Tx	29
UART3 Rx	6	SPI3 Rx	14	I3C0 Rx	22	I2S3 Rx	30
UART3 Tx	7	SPI3 Tx	15	I3C0 Tx	23	I2S3 Tx	31

Workaround
The EROUTER is functional in revision B devices.

1.1.3 Power Management Is Limited

Datasheet Section Reference: 3.7
Description
Power management is limited to only GO and STOP modes with two power domains. The IDLE, READY, and STANDBY modes are not functional. Not all peripherals may be clock-gated.

Workaround
All power modes will be available in revision B devices.

Datasheet Section Reference: 5.2.3
Description
STOP mode power mode current consumption for STOP_2 power mode (IDDST2) will exceed 2.5 µA

Because there are only two power domains in the device and no clock gating, all processors and peripherals are being clocked even if the processors are held in a stopped state. GO power mode 3.3V supply current is approximately 100 mA at room temperature plus 30 µA /MHz for the M55_HP processor and 26 µA /MHz for the M55_HE processor.

Workaround
Revision B devices are targeted to have GO power mode power per the datasheet specifications.

1.1.4 Limited Clock Frequency Scaling Options for RTSS-HE

Datasheet Section Reference: 3.9
Description
The clock frequency options for the High Efficiency Cortex-M55 CPU in the High-Efficiency Real-Time Processor System (RTSS-HE) are limited to 160 MHz, 120 MHz, or 38.4 MHz.

Workaround
Use one of the available frequency options.
Revision B devices will have all clock frequency options specified in the datasheet.

1.2 Secure Enclave Limitations

1.2.1 Some Security Features Not Enabled

Datasheet Section Reference: 3.5
Description
The RTSS-HE CPU has access to these system control registers because firewall protection is not available:

- VTOR registers for CM55-HP & CM55-HE
- Pin-Mux control registers
- Pads Control registers

Workaround
Be aware that code written for the RTSS-HE CPU would not be protected from modifying the identified system control registers that are outside of the normal RTSS-HE application domain.
Revision B devices will have all security features specified in the datasheet.

1.3 High-Performance RTSS Limitations

1.3.1 Limited Number of RTSS-HE Peripherals May Use DMA

Datasheet Section Reference: 3.14

Description

The DMA1 controller in the High-Performance Real-Time Subsystem (RTSS-HP) only supports a limited number of the peripherals attached to the M55-HP CPU. The functions supported area shown below.

DMA1 Channels Assignment (RTSS-HP)

Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#
UART4 Rx	0	CMP0	8	TIMER0A	16	P2_0	24
UART4 Tx	1	CMP1	9	TIMER0B	17	P2_1	25
UART5 Rx	2	CMP2	10	TIMER1A	18	P2_2	26
UART5 Tx	3	CMP3	11	TIMER1B	19	P2_3	27
UART6 Rx	4	ENC0	12	TIMER2A	20	P2_4	28
UART6 Tx	5	ENC1	13	TIMER2B	21	P2_5	29
UART7 Rx	6	ENC2	14	TIMER3A	22	P2_6	30
UART7 Tx	7	ENC3	15	TIMER3B	23	P2_7	31

DMA channels in GRAY are not implemented in A1 2nd Sample Silicon

Workaround

In revision B devices, the DMA1 controller supports all peripheral as specified in the datasheet.

1.4 High-Efficiency RTSS Limitations

1.4.1 LPI2S Not Functional

Datasheet Section Reference: 3.17.4

Description

The Low-Power Inter-IC Sound (LPI2S) module is not functional.

Workaround

Use of the four standard I2S modules.

The LPI2S module is functional in revision B devices.

1.4.2 LPSPI Not Functional

Datasheet Section Reference: 3.17.7

Description

The Low-Power Serial Peripheral Interface (LPSPI) module is not functional.

Workaround

Use one of the four standard SPI modules.

The LPSPI module is functional in revision B devices.

1.4.3 LPI2C Not Functional

Datasheet Section Reference: 3.17.3

Description

The Low-Power Inter-Integrated Circuit (LPI2C) module is not functional.

Workaround
The LPI2C module is functional in revision B devices.

1.4.4 LPPDM Not Functional

Datasheet Section Reference: 3.17.6
Description
The Low-Power Pulse Density Modulation (LPPDM) module is not functional.

Workaround
The LPPDM module is functional in revision B devices.

1.4.5 LPCPI Not Functional

Datasheet Section Reference: 3.20.1
Description
The low-power digital Camera Parallel Interface (LPCPI) module is not functional.

Workaround
Use the standard power CPI interface in the Shared Peripherals block.
The LPCPI module is functional in revision B devices.

1.4.6 VBATT Domain Power Consumption Reduced In 2nd Sample Silicon

Datasheet Section Reference: 5.2.3
Description
V_{BATT} domain power consumption is approximately 3 µA in 2nd sample silicon. Targeting <1.0 µA in production devices.

Workaround
None.

1.4.7 Limited Number of Peripheral May Use DMA

Datasheet Section Reference:
Description
The DMA2 controller in the High-Efficiency Real-Time Subsystem (RTSS-HE) only supports a limited number of the peripherals attached to the M55-HE CPU. The functions supported area shown below.

DMA2 Channels Assignment (RTSS-HE)

Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#	Request	DMA Ch#
ADC0	0	LPUART Rx	8	PDM0	16	P3_16	24
ADC1	1	LPUART Tx	9	PDM1	17	P3_17	25
ADC2	2	LPTIMER0	10	PDM2	18	P3_18	26
BOD	3	LPTIMER1	11	PDM3	19	P3_19	27
I3C Rx	4	CAN-FD Rx	12	PDM4	20	P3_20	28
I3C Tx	5	CAN-FD Tx	13	PDM5	21	P3_21	29
I2C3 Rx	6	LPSPI Rx	14	PDM6	22	P3_22	30

I2C3 Tx	7	LPSPI Tx	15	PDM7	23	P3_23	31

DMA channels in GRAY are not implemented in A0 1st Sample Silicon or A1 2nd Sample Silicon

Workaround

In revision B devices, the DMA2 controller supports all peripherals specified in the datasheet.

1.5 Shared Peripherals Limitations

1.5.1 I2C Not Functional

Datasheet Section Reference: 3.17.3

Description

The Inter-Integrated Circuit (I2C) modules are not functional.

Workaround

The I2C modules are functional in revision B devices.

1.5.2 PDM Not Functional

Datasheet Section Reference: 3.17.6

Description

The Pulse Density Modulation (PDM) module is not functional.

Workaround

The PDM module is functional in revision B devices.

1.5.4 GPIO Currently Grouped In Blocks 32 I/Os

Datasheet Section Reference: 3.16

Description

General Purpose I/Os (GPIOs) are currently grouped in blocks of 32 I/Os.
The grouping of GPIOs in the A1 sample devices is according to the table below:

A1 Sample Silicon

Table 3-9 GPIO Signal Descriptions

Signal Name	Pin Name	Type	Description
GPIO0			
P0_0	P0_0	IO	General purpose input/output
P0_1	P0_1	IO	General purpose input/output
P0_2	P0_2	IO	General purpose input/output
P0_3	P0_3	IO	General purpose input/output
P0_4	P0_4	IO	General purpose input/output
P0_5	P0_5	IO	General purpose input/output
P0_6	P0_6	IO	General purpose input/output
P0_7	P0_7	IO	General purpose input/output
P0_8	P0_8	IO	General purpose input/output
P0_9	P0_9	IO	General purpose input/output
P0_10	P0_10	IO	General purpose input/output
P0_11	P0_11	IO	General purpose input/output
P0_12	P0_12	IO	General purpose input/output
P0_13	P0_13	IO	General purpose input/output
P0_14	P0_14	IO	General purpose input/output
P0_15	P0_15	IO	General purpose input/output
P0_16	P0_16	IO	General purpose input/output
P0_17	P0_17	IO	General purpose input/output TSENS output voltage (see 3.22.5 Temperature Sensor)
P0_18	P0_18	IO	General purpose input/output
P0_19	P0_19	IO	General purpose input/output
GPIO 1			
GPIO1_0	P1_0	IO	General purpose input/output
GPIO1_1	P1_1	IO	General purpose input/output
GPIO1_2	P1_2	IO	General purpose input/output
GPIO1_3	P1_3	IO	General purpose input/output
GPIO1_4	P1_4	IO	General purpose input/output
GPIO1_5	P1_5	IO	General purpose input/output
GPIO1_6	P1_6	IO	General purpose input/output
GPIO1_7	P1_7	IO	General purpose input/output

Signal Name	Pin Name	Type	Description
GPIO1_8	P1_8	IO	General purpose input/output
GPIO1_9	P1_9	IO	General purpose input/output
GPIO1_10	P1_10	IO	General purpose input/output
GPIO1_11	P1_11	IO	General purpose input/output
GPIO1_12	P1_12	IO	General purpose input/output
GPIO1_13	P1_13	IO	General purpose input/output
GPIO1_14	P1_14	IO	General purpose input/output
GPIO1_15	P1_15	IO	General purpose input/output
GPIO1_16	P1_16	IO	General purpose input/output
GPIO1_17	P1_17	IO	General purpose input/output
GPIO1_18	P1_18	IO	General purpose input/output
GPIO1_19	P1_19	IO	General purpose input/output
GPIO1_20	P1_20	IO	General purpose input/output
GPIO1_21	P1_21	IO	General purpose input/output
GPIO1_22	P1_22	IO	General purpose input/output
GPIO1_23	P1_23	IO	General purpose input/output
GPIO1_24	P1_24	IO	General purpose input/output
GPIO1_25	P1_25	IO	General purpose input/output
GPIO1_26	P1_26	IO	General purpose input/output
GPIO1_27	P1_27	IO	General purpose input/output
GPIO1_28	P1_28	IO	General purpose input/output
GPIO1_29	P1_29	IO	General purpose input/output
GPIO1_30	P1_30	IO	General purpose input/output
GPIO1_31	P1_31	IO	General purpose input/output
GPIO2			
GPIO2_0	P2_0	IO	General purpose input/output
GPIO2_1	P2_1	IO	General purpose input/output
GPIO2_2	P2_2	IO	General purpose input/output
GPIO2_3	P2_3	IO	General purpose input/output
GPIO2_4	P2_4	IO	General purpose input/output
GPIO2_5	P2_5	IO	General purpose input/output
GPIO2_6	P2_6	IO	General purpose input/output
GPIO2_7	P2_7	IO	General purpose input/output
GPIO2_8	P2_8	IO	General purpose input/output
GPIO2_9	P2_9	IO	General purpose input/output
GPIO2_10	P2_10	IO	General purpose input/output
GPIO2_11	P2_11	IO	General purpose input/output
GPIO2_12	P2_12	IO	General purpose input/output
GPIO2_13	P2_13	IO	General purpose input/output
GPIO2_14	P2_14	IO	General purpose input/output
GPIO2_15	P2_15	IO	General purpose input/output
GPIO2_16	P2_16	IO	General purpose input/output
GPIO2_17	P2_17	IO	General purpose input/output
GPIO2_18	P2_18	IO	General purpose input/output
GPIO2_19	P2_19	IO	General purpose input/output

Signal Name	Pin Name	Type	Description
GPIO2_20	P2_20	IO	General purpose input/output
GPIO2_21	P2_21	IO	General purpose input/output
GPIO2_22	P2_22	IO	General purpose input/output
GPIO2_23	P2_23	IO	General purpose input/output
GPIO2_24	P2_24	IO	General purpose input/output
GPIO2_25	P2_25	IO	General purpose input/output
GPIO2_26	P2_26	IO	General purpose input/output
GPIO2_27	P2_27	IO	General purpose input/output
GPIO2_28	P2_28	IO	General purpose input/output
GPIO2_29	P2_29	IO	General purpose input/output
GPIO2_30	P2_30	IO	General purpose input/output
GPIO2_31	P2_31	IO	General purpose input/output
GPIO3			
GPIO3_0	P3_0	IO	General purpose input/output
GPIO3_1	P3_1	IO	General purpose input/output
GPIO3_2	P3_2	IO	General purpose input/output
GPIO3_3	P3_3	IO	General purpose input/output
GPIO3_4	P3_4	IO	General purpose input/output
GPIO3_5	P3_5	IO	General purpose input/output
GPIO3_6	P3_6	IO	General purpose input/output
GPIO3_7	P3_7	IO	General purpose input/output
GPIO3_8	P3_8	IO	General purpose input/output
GPIO3_9	P3_9	IO	General purpose input/output
GPIO3_10	P3_10	IO	General purpose input/output
GPIO3_11	P3_11	IO	General purpose input/output
GPIO3_12	P3_12	IO	General purpose input/output
GPIO3_13	P3_13	IO	General purpose input/output
GPIO3_14	P3_14	IO	General purpose input/output
GPIO3_15	P3_15	IO	General purpose input/output
GPIO3_16	P3_16	IO	General purpose input/output
GPIO3_17	P3_17	IO	General purpose input/output
GPIO3_18	P3_18	IO	General purpose input/output
GPIO3_19	P3_19	IO	General purpose input/output
GPIO3_20	P3_20	IO	General purpose input/output
GPIO3_21	P3_21	IO	General purpose input/output
GPIO3_22	P3_22	IO	General purpose input/output
GPIO3_23	P3_23	IO	General purpose input/output
LPGPIO			
LPGPIO_0	P4_0	IO	Low power general purpose input/output
LPGPIO_1	P4_1	IO	Low power general purpose input/output
LPGPIO_2	P4_2	IO	Low power general purpose input/output
LPGPIO_3	P4_3	IO	Low power general purpose input/output
LPGPIO_4	P4_4	IO	Low power general purpose input/output
LPGPIO_5	P4_5	IO	Low power general purpose input/output
LPGPIO_6	P4_6	IO	Low power general purpose input/output

Signal Name	Pin Name	Type	Description
LPGPIO_7	P4_7	IO	Low power general purpose input/output

Workaround

Revision B devices will have GPIOs grouped is blocks of 8 I/Os as specified in the datasheet.

1.5.5 Port 0 Pins Are Analog and Not GPIO And Not Available

Datasheet Section Reference: 3.16

Description

Port 0 pins, designated as P0_[0:19] in group GPIO0 in the A0/A1 table 3-9 shown above are solely analog I/Os and cannot be used as General-Purpose I/Os.

Workaround

If GPIOs are needed, use other GPIO pins on other ports.
In revision B devices, pins in signal groups GPIO0, GPIO1, and GPIO2 can be used as General-Purpose I/Os or analog I/Os as specified in the datasheet.

1.5.6 ADC Single-Ended Reference Voltage Not Internally Connected

Datasheet Section Reference: 3.20.1

Description

The internal connection of the ADC reference to ground for single-ended input mode is not present in A1 devices.

Workaround

For A1 devices, the negative input to the ADC (INM) should be tied to ground.
This will be fixed in revision B devices.

1.5.7 ADC24 Not Functional

Datasheet Section Reference: 3.20.1

Description

The 24-bit ADC24 module is not functional in A1 devices.

Workaround

Use ADC12 modules for revision A1 designs. The ADC24 module will be fixed in revision B devices.

1.5.8 High-Speed Comparator (CMP) Interrupts Are Inverted in A1

Datasheet Section Reference: 3.20.3

Description

With CMP polarity inversion bit cleared, interrupts are normally generated from the CMP block when Input A > Input B. Polarity inversion can then be enabled to generate another interrupt when Input B > Input A. However, in revision A1 devices the comparator output is inverted.

Workaround

The comparator polarity inversion bit should be enabled in the CMP before enabling interrupts in A1 devices. This will result in an interrupt being generated when Input A > Input B. The interrupt service routine (ISR) can then clear the polarity inversion bit to allow another interrupt to be generated when Input A < Input B.
This limitation is fixed in revision B devices.

1.7 External Memory Expansion Limitations

1.7.1 Cannot Extend Internal SRAM Capacity With External OctalSPI SRAM

Datasheet Section Reference: 3.11.3

Description

CPUs and bus masters cannot use external OctalSPI SRAM to extend internal SRAM capacity.

Workaround

Revision B devices can use OctalSPI SRAM to extend internal SRAM as specified in the datasheet.

Document History

Version	Change Log
1.3	Pre-release
1.4	Added information on ADC and COMP behavior
1.5	Added note that ADC24 is not functional in Revision A1 devices