

# Errata and Specification Changes Revision B1 Silicon

E3 Series Microcontrollers
Ensemble Family

## **Ensemble Errata**



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## 1 Document Scope and Device Identification

#### This document includes:

- ERRATA for functions in Ensemble E3 Series, revision B1 devices, that do not match the device specification as documented in the current datasheet.
- SPECIFICATION CHANGES that will appear in the next revision of datasheet.

Current Datasheet Reference: ADTS0007 v2.4 (E3 Series MCUs)

Applicable Silicon Version: Revision B1

Device Marking Identification: See photos below:







**WLCSP208** Package



# 2 ERRATA

#### 2.1 STANDBY Low-Power Mode is Not Enabled

#### Description

The device will not enter STANDBY mode when commanded by software.

#### Workaround

While there is no workaround for revision B1 devices, this limitation will be removed in revision B2 devices.

#### 2.2 One of the Two OctalSPI Interfaces Does Not Support HyperBus Protocol

#### Description

OctalSPI interface with designation OSPI1 does not support the HyperBus protocol for connection to external HyperRAM memory modules. However, the OctalSPI interface designated as OSPI0 does support HyperRAM protocol.

#### Workaround

Use OctalSPI port OSPI0 in revision B1 devices to connect external HyperRAM modules, do not use port OSPI1 for HyperRAM modules.

This limitation will be removed in B2 devices where both OctalSPI ports support HyperRAM.

## 3 SPECIFICATION CHANGES

## 3.1 Power Mode Definitions, Power Consumption, and Wake Times

#### Description

The table below provides an overview of the changes that will be applied to the next version of the datasheet regarding Low Power Modes, Power Consumption, and Wake Timing.

	Danier Manda			SRAM			Clock	Main	LP Dominion and the	Wake-Up	Current Consumption				Wake Time to Reach GO Mode			
	Power Mode	Regulation	MRAM	Bulk SRAM	M55-HP TCM	M55-HE TCM	4KB Backup	Source	Peripherals Power	Peripherals Power	Sources	Min	Тур	Max	Units	Тур	Units	
GO Mode	s											I <sub>VDD_3</sub>	v3 when V	DD_3V3 =	3.3V			
GO_1	All NPU cores running, all CPU cores running CoreMark max freq from PLL. All CPU cores running CoreMark at max	_		ON	0.11	0.11	ON			ON with				TBD 29.7		mA mA		
	requency from PLL. No NPU enabled. Only M55-HP running CoreMark at 400			ON ON	ON	OFF ON	ON	PLL	clocks gated	All ON	Any interrupt from a powered peripheral		16		mA	N/A		
GO_4	MHz from PLL. No NPU is enabled. Only M55-HE running WHILE(1) at 76.8 MHz from HFRC. No NPU is enabled.		OFF	055	OFF	ON		HFRC	All OFF				2.1 27		mA uA/MHz uA/MHz	19/4		
GO_5	Only M55-HE running WHILE(1) at 19.2 MHz from HFRC. No NPU is enabled.			OFF									725 38		uA uA/MHz			
READY M												I <sub>VDD_3</sub>	<sub>v3</sub> when V	DD_3V3 =	3.3V			
RDY_1	M55-HP WFI at 400MHz from PLL.  M55-HE powered off M55-HE WFI at 78.6 MHz from HFRC.	DC-DC OFF	OFF	ON	ON	OFF	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered		11.6		mA	<75	ns	
RDY_2	M55-HP powered off			OFF	OFF	ON		HFRC	All OFF		peripheral		1.6 <sub>V3</sub> when V	DD 3//3 -	mA	<200	ns	
IDLE_1	All CPU cores powered off. 38.4MHz clock from HFXO	- DC-DC OFF		OFF	F OFF	OFF but retained		HFXO	ON with		Any interrupt	VDD 3	2.8	_3v3 =	mA	2 - 4	us	
IDLE_2	All CPU cores powered off. 600KHz clock from HFRC		OFF					HFRC	clocks gated	All ON	from a powered peripheral		875		uA	2 - 4	us	
STANDBY	Modes											I <sub>VDD_3</sub>	<sub>v3</sub> when V	DD_3V3 =	3.3V			
STBY_1	All CPU cores powered off. HFRC ready	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral		55		uA	2 - 4	us	
STOP Mo	des											I <sub>VDD_BA</sub>	π when V	DD_BATT	= 3.0V			
STOP_1	STOP_2 plus 512KB of M55-HE TCM SRAM retained	LDO				OFF but retained		LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral		4800		nA			
STOP_2	STOP_3 plus 4KB Backup SRAM retained		OFF	OFF	OFF	OFF							1350		nA	1.1	ms	
STOP_3	STOP_4 plus LPTIMER, BOD, CMP, and LPGPIO active STOP 5 plus LPRTC running						OFF						1300		nA			
STOP_4	from 32KHz LFXO  32KHz LFRC running,									LPRTC ON			1250		nA			
STOP_5	all other functions off							LFRC		All OFF			1100		nA			
I/O Domain Adder for STOP in all cases													ode Curre VDD_VDD 200			N	/A	

# **Document History**

Version	Change Log
1.0	Original Release 21 June 2023
1.1	Changed applicable E3 Series MCU Datasheet from v2.3 to v2.4