



Errata and Specification Changes

Revision B1 Silicon

E3 Series Microcontrollers Ensemble Family

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1 Document Scope and Device Identification

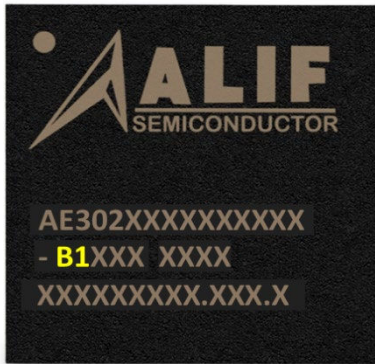
This document includes:

- ERRATA for functions in Ensemble E3 Series, revision B1 devices, that do not match the device specification as documented in the current datasheet.
- SPECIFICATION CHANGES that will appear in the next revision of datasheet.

Current Datasheet Reference: ADTS0007 v2.4 (E3 Series MCUs)

Applicable Silicon Version: Revision B1

Device Marking Identification: See photos below:



FBGA194 Package



WLCSP208 Package

2 ERRATA

2.1 STANDBY Low-Power Mode is Not Enabled

Description

The device will not enter STANDBY mode when commanded by software.

Workaround

While there is no workaround for revision B1 devices, this limitation will be removed in revision B2 devices.

2.2 One of the Two OctalSPI Interfaces Does Not Support HyperBus Protocol

Description

OctalSPI interface with designation OSPI1 does not support the HyperBus protocol for connection to external HyperRAM memory modules. However, the OctalSPI interface designated as OSPI0 does support HyperRAM protocol.

Workaround

Use OctalSPI port OSPI0 in revision B1 devices to connect external HyperRAM modules, do not use port OSPI1 for HyperRAM modules.

This limitation will be removed in B2 devices where both OctalSPI ports support HyperRAM.

3 SPECIFICATION CHANGES

3.1 Power Mode Definitions, Power Consumption, and Wake Times

Description

The table below provides an overview of the changes that will be applied to the next version of the datasheet regarding Low Power Modes, Power Consumption, and Wake Timing.

Power Mode	Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption				Wake Time to Reach GO Mode		
			Bulk SRAM	M55-HP TCM	M55-HE TCM	4KB Backup					Min	Typ	Max	Units	Typ	Units	
GO Modes											I_{VDD_3V3} when $VDD_3V3 = 3.3V$						
GO_1	DC-DC	ON	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral		TBD			mA	N/A	
GO_2												29.7			mA		
GO_3												16			mA		
GO_4												40			uA/MHz		
GO_5												2.1			mA		
						27				uA/MHz							
											725					uA	
												38				uA/MHz	
READY Modes											I_{VDD_3V3} when $VDD_3V3 = 3.3V$						
RDY_1	DC-DC	OFF	ON	ON	OFF	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral		11.6			mA	<75	ns
RDY_2							HFRC	All OFF					mA	<200	ns		
IDLE Modes											I_{VDD_3V3} when $VDD_3V3 = 3.3V$						
IDLE_1	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral		2.8			mA	2 - 4	us
IDLE_2							HFRC						uA	2 - 4	us		
STANDBY Modes											I_{VDD_3V3} when $VDD_3V3 = 3.3V$						
STBY_1	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral		55			uA	2 - 4	us
STOP Modes											I_{VDD_BATT} when $VDD_BATT = 3.0V$						
STOP_1	LDO	OFF	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral		4800			nA	1.1	ms
STOP_2												1350			nA		
STOP_3												1300			nA		
STOP_4												1250			nA		
STOP_5																LFRC	All OFF
I/O Domain Adder for STOP in all cases											STOP Mode Current adder $I_{VDD_IO_1V8}$ when $VDD_VDD_IO_1V8 = 1.8V$						
												200				nA	

Document History

Version	Change Log
1.0	Original Release 21 June 2023
1.1	Changed applicable E3 Series MCU Datasheet from v2.3 to v2.4