Errata and Specification Changes

Revision B2 Silicon

Ensemble Family

E1, E3 Series Microcontrollers
E5, E7 Series Fusion Processors

Contents

1 Document Scope and Device Identification

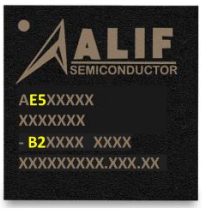
This document includes:

1. The **ERRATA** reflecting functions in silicon revision B2 of Ensemble Family devices that do not match the specifications in the published v2.5 datasheets. Functional limitations resulting from these errata for silicon revision B2 will be corrected in the coming silicon revision B3. The specifications in version v2.5 datasheets represent the function of the coming silicon revision B3 devices.
2. The **SPECIFICATION CHANGES and UPDATES** in v2.5 datasheets compared to the previously published version v2.4 datasheets.

Current Datasheet Reference:

Document Number	Version	Datasheet Description
ADTS0008	v2.5	E1 Series MCUs
ADTS0007	v2.5	E3 Series MCUs
ADTS0006	v2.5	E5 Series Fusion Processors
ADTS0005	V2.5	E7 Series Fusion Processors

Listed Errata is Applicable to Silicon Version: Revision B2
B2 Silicon Device Marking Identification: See images below.

Device Series	FBGA194 Package	WLCSP208 Package
E1		N/A
E3		
E5		
E7		

2 ERRATA

2.1 USB Host Mode is Not Enabled

Applies to:
E1, E3, E5, E7 devices.

Description
The USB 2.0 Low Speed/Full Speed/High Speed interface will not support USB Host mode. Only USB Device mode is supported.

Workaround
While there is no workaround for revision B2 devices, **this limitation will be removed in revision B3 devices where USB Host mode will be operational, as well as USB Device mode**.

2.2 Limitations to Restarting some Clock Sources that Originate from PLL

Applies to:
E1, E3, E5, E7 devices.

Description
Powering on the PLL by software command after the PLL was previously powered off by software command may result in an incorrect clock frequency on the 160MHz or 80MHz branches of the clock tree, both of which originate from the 480MHz portion of PLL outputs. There are no problems with any other clock branches derived from the PLL related to this software-initiated power cycle sequence.

160MHz and 80MHz clock sources affect the operation of the RTSS-HE (Real Time Subsystem – High Efficiency) that includes the M55-HE (Cortex-M55 160MHz CPU core) and the NPU-HE (Ethos-U55 128 MAC NPU accelerator).

When this issue occurs, it is possible that the frequency of either the 160MHz or the 80MHz clock source will be above or below their expected frequencies.

Please note that there are no clocking problems if the PLL is powered on from a device cold power up cycle and the PLL is not subsequently powered off and powered back on via software.

Workaround
Use any one of these methods to avoid clocking issues:

- Do not choose to use the 160MHz or 80MHz clock source for operating the RTSS_HE, instead choose either the 120MHz or 60MHz clock source.
- Use the 160MHz or 80MHz clock source but delay at least 150us before issuing a software command to repower the PLL after a previously commanding the PLL power off via software.
- Use the 160MHz or 80MHz clock source but maintain PLL power during STANDBY mode (do not turn off the PLL via software). This will add about 800uA at 3.3V to the STANDBY mode current.

These clocking limitations will be removed in revision B3 devices

3 SPECIFICATION CHANGES and UPDATES

3.1 Power Mode Definitions, Power Consumption, and Wake Times

3.1.1 E1 Series

Description

Specifications in Ensemble Series E1 device datasheet v2.5 that have been updated relative to E1 device datasheet v2.4. Some specifications have been changed, and wake times have been added to the table (Datasheet Section 5.2.2.1).

E1 Series MCUs

Power Mode		Voltage Regulation	MRAM	SRAM			Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HE TCM	4KB Backup					Typical	Units	Typical	Units
GO Modes														
GO_1	M55-HE running CoreMark at 160 MHz. NPU running convolution MAC workload.	DC-DC	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	20[3]	mA	N/A	
											125	uA/MHz		
GO_2	M55-HE running CoreMark at 160 MHz. No NPU is enabled.										15[3]	mA		
											96	uA/MHz		
GO_3			OFF	OFF							13[3]	mA		
											81	uA/MHz		
GO_4	M55-HE running WHILE(1) at 76.8 MHz. No NPU is enabled.						HFRC	All OFF			2.1	mA		
											27	uA/MHz		
GO_5	M55-HE running WHILE(1) at 19.2 MHz. No NPU is enabled.										725	uA		
											38	uA/MHz		
READY Modes														
RDY_1	M55-HE in WFI[2] at 160MHz.	DC-DC	OFF	OFF	ON	ON	PLL	ON with clocks	All ON	Any interrupt from a powered peripheral	8.7[4]	mA	<100	ns
RDY_2	M55-HE in WFI at 78.6 MHz.						HFRC	All OFF			1.4	mA	<200	ns
IDLE Modes														
IDLE_1	CPU and NPU cores powered off. 38.4MHz clock.	DC-DC	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral[1]	2.5	mA	2 - 4	us
IDLE_2	CPU and NPU cores powered off. 600KHz clock.						HFRC				900	uA	2 - 4	us
STANDBY Modes														
STBY_1	CPU and NPU cores powered off. HFRC ready	DC-DC	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral	65	uA	2 - 4	us
STOP Modes														
STOP_1	STOP_2 plus 512KB of M55-HE TCM SRAM retained	LDO	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral	6150	nA	1.1	ms
STOP_2	STOP_3 plus 4KB Backup SRAM retained				OFF						1450	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, CMP, and LPGPIO active					OFF					1400	nA		
STOP_4	STOP_5 plus LPRTC running from 32KHz LFXO								LPRTC + LPGPIO ON		1350	nA		
STOP_5	32KHz LFRC running, all other functions off						LFRC		LPGPIO ON		1250	nA	N/A	
I/O Domain Adder for STOP in all cases											STOP Mode Current adder $I_{VDD\_IO\_1V8}$ when VDD_VDD_IO_1V8 = 1.8V			
											200	nA		

1. If RTSS-HE is powered down then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are powered down too.
2. WFI: Wait for Interrupt.
3. At ACLK = 100 MHz, HCLK = 100 MHz.
4. At ACLK = 100 MHz, HCLK = 50 MHz, PCLK = 25MHz.

3.1.2 E3 Series

Description

Specifications in Ensemble Series E3 device datasheet v2.5 that have been updated relative to E3 device datasheet v2.4. Some specifications have been changed, and wake times have been added to the table (Datasheet Section 5.2.2.1).

E3 Series MCUs

Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	4KB Backup					Typical	Units	Typical	Units
GO Modes															
GO_1	All CPU cores running CoreMark at max frequency. Both NPU cores running convolution MAC workload.	DC-DC	ON	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	51[3]	mA	N/A	
GO_2	Both CPU cores running CoreMark at max frequency. No NPU enabled.											27[3]	mA		
GO_3	Only M55-HP running CoreMark at 400 MHz. No NPU is enabled.					OFF						21[3]	mA		
												52	uA/MHz		
GO_4	Only M55-HE running WHILE(1) at 76.8 MHz. No NPU is enabled.		OFF	OFF	OFF	ON		HFRC	All OFF			2.1	mA		
												27	uA/MHz		
GO_5	Only M55-HE running WHILE(1) at 19.2. No NPU is enabled.											725	uA		
												38	uA/MHz		
READY Modes															
RDY_1	M55-HP WFI[2] at 400MHz from PLL. M55-HE powered off	DC-DC	OFF	OFF	ON	OFF	ON	PLL	ON with clocks	All ON	Any interrupt from a powered peripheral	13.5[4]	mA	<40	ns
RDY_2	M55-HE WFI at 78.6 MHz from HFRC. M55-HP powered off				OFF	ON		HFRC	All OFF			1.4	mA	<200	ns
IDLE Modes															
IDLE_1	All CPU cores powered off. 38.4MHz clock from HFXO	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral[1]	2.5	mA	2 - 4	us
IDLE_2	All CPU cores powered off. 600KHz clock from HFRC							HFRC				900	uA	2 - 4	us
STANDBY Modes															
STBY_1	All CPU cores powered off. HFRC ready	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral	65	uA	2 - 4	us
STOP Modes															
STOP_1	STOP_2 plus 512KB of M55-HE TCM SRAM retained	LDO	OFF	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral	6150	nA	1.1	ms
STOP_2	STOP_3 plus 4KB Backup SRAM retained					OFF						1450	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, CMP, and LPGPIO active						OFF					1400	nA		
STOP_4	STOP_5 plus LPRTC running from 32KHz LFXO									LPRTC + LPGPIO ON		1350	nA		
STOP_5	32KHz LFRC running, all other functions off							LFRC		LPGPIO ON		1250	nA	N/A	
I/O Domain Adder for STOP in all cases												STOP Mode Current adder $I_{VDD\_IO\_1V8}$ when VDD_VDD_IO_1V8 = 1.8V			
												200	nA		

1. If RTSS-HE is powered down then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are powered down too.
2. WFI: Wait for Interrupt.
3. At ACLK = 200 MHz, HCLK = 200 MHz.
4. At ACLK = 100 MHz, HCLK = 50 MHz. PCLK = 25 MHz.

3.1.3 E5 Series

Description

Specifications in Ensemble Series E5 device datasheet v2.5 that have been updated relative to E5 device datasheet v2.4. Some specifications have been changed, and wake times have been added to the table (Datasheet Section 5.2.2.1).

E5 Series Fusion Processors

Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	4KB Backup					Typical	Units	Typical	Units
GO Modes															
GO_1	All CPU cores running CoreMark at max frequency. Both NPU cores running convolution MAC workload.	DC-DC	ON	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	81[3]	mA	N/A	
GO_2	All CPU cores running CoreMark at max frequency. No NPU enabled.											51	mA		
GO_3	Only A32-0 running CoreMark at 800 MHz. No NPU is enabled.											46	mA		
												58	uA/MHz		
GO_4	Only M55-HP running CoreMark at 400 MHz. No NPU is enabled.		OFF	OFF		OFF						25[3]	mA		
												62	uA/MHz		
GO_5	Only M55-HE running WHILE(1) at 76.8 MHz. No NPU is enabled.				OFF	ON		HFRC	All OFF			2.1	mA		
												27	uA/MHz		
GO_6	Only M55-HE running WHILE(1) at 19.2. No NPU is enabled.											725	uA		
												38	uA/MHz		
READY Modes															
RDY_1	M55-HP WFI[2] at 400MHz from PLL. M55-HE powered off	DC-DC	OFF	OFF	ON	OFF	ON	PLL	ON with clocks	All ON	Any interrupt from a powered peripheral	13.5[4]	mA	<40	ns
RDY_2	M55-HE WFI at 78.6 MHz from HFRC. M55-HP powered off				OFF	ON		HFRC	All OFF			1.4	mA	<200	ns
IDLE Modes															
IDLE_1	All CPU cores powered off. 38.4MHz clock from HFXO	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral[1]	2.5	mA	2 - 4	us
IDLE_2	All CPU cores powered off. 600KHz clock from HFRC							HFRC				900	uA	2 - 4	us
STANDBY Modes															
STBY_1	All CPU cores powered off. HFRC ready	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral	65	uA	2 - 4	us
STOP Modes															
STOP_1	STOP_2 plus 512KB of M55-HE TCM SRAM retained	LDO	OFF	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral	6150	nA	1.1	ms
STOP_2	STOP_3 plus 4KB Backup SRAM retained					OFF						1450	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, CMP, and LPGPIO active						OFF					1400	nA		
STOP_4	STOP_5 plus LPRTC running from 32KHz LFXO									LPRTC + LPGPIO ON		1350	nA		
STOP_5	32KHz LFRC running, all other functions off							LFRC		LPGPIO ON		1250	nA	N/A	
I/O Domain Adder for STOP in all cases												STOP Mode Current adder $I_{VDD\_IO\_1V8}$ when VDD_VDD_IO_1V8 = 1.8V			
												200	nA		

1. If RTSS-HE is powered down then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are powered down
2. WFI: Wait for Interrupt.
3. At ACLK = 400 MHz, HCLK = 200 MHz.
4. At ACLK = 100 MHz, HCLK = 50 MHz, PCLK = 25MHz.

3.1.3 E7 Series

Description

Specifications in Ensemble Series E7 device datasheet v2.5 have been updated relative to E7 device datasheet v2.4. Some specifications have been changed, and wake times have been added to the table (Datasheet Section 5.2.2.1).

E7 Series Fusion Processors

Power Mode		Voltage Regulation	MRAM	SRAM				Clock Source	Main Peripherals Power	LP Peripherals Power	Wake-Up Sources	Current Consumption		Wake Time to Reach GO Mode	
				Bulk SRAM	M55-HP TCM	M55-HE TCM	4KB Backup					Typical	Units	Typical	Units
GO Modes															
GO_1	All CPU cores running CoreMark at max frequency. Both NPU cores running convolution MAC workload.	DC-DC	ON	ON	ON	ON	ON	PLL	ON with clocks gated	All ON	Any interrupt from a powered peripheral	94[3]	mA	N/A	
GO_2	All CPU cores running CoreMark at max frequency. No NPU enabled.											64	mA		
GO_3	A32-0 and A32-1 running CoreMark at 800 MHz. No NPU is enabled.											58	mA		
												72	uA/MHz		
GO_4	Only M55-HP running CoreMark at 400 MHz. No NPU is enabled.		OFF	OFF		OFF						25[3]	mA		
												62	uA/MHz		
GO_5	Only M55-HE running WHILE(1) at 76.8 MHz. No NPU is enabled.				OFF	ON		HFRC	All OFF			2.1	mA		
												27	uA/MHz		
GO_6	Only M55-HE running WHILE(1) at 19.2. No NPU is enabled.											725	uA		
												38	uA/MHz		
READY Modes															
RDY_1	M55-HP WFI[2] at 400MHz from PLL. M55-HE powered off	DC-DC	OFF	OFF	ON	OFF	ON	PLL	ON with clocks	All ON	Any interrupt from a powered peripheral	13.5[4]	mA	<40	ns
RDY_2	M55-HE WFI at 78.6 MHz from HFRC. M55-HP powered off				OFF	ON		HFRC	All OFF			1.4	mA	<200	ns
IDLE Modes															
IDLE_1	All CPU cores powered off. 38.4MHz clock from HFXO	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFXO	ON with clocks gated	All ON	Any interrupt from a powered peripheral[1]	2.5	mA	2 - 4	us
IDLE_2	All CPU cores powered off. 600KHz clock from HFRC							HFRC				900	uA	2 - 4	us
STANDBY Modes															
STBY_1	All CPU cores powered off. HFRC ready	DC-DC	OFF	OFF	OFF	OFF but retained	OFF but retained	HFRC	All OFF	LPUART, LPI2C ON + STOP Mode peripherals	Any interrupt from a powered peripheral	65	uA	2 - 4	us
STOP Modes															
STOP_1	STOP_2 plus 512KB of M55-HE TCM SRAM retained	LDO	OFF	OFF	OFF	OFF but retained	OFF but retained	LFXO	All OFF	LPRTC, LPTIMER, CMP, BOD, LPGPIO ON	Any interrupt from a powered peripheral	6150	nA	1.1	ms
STOP_2	STOP_3 plus 4KB Backup SRAM retained					OFF						1450	nA		
STOP_3	STOP_4 plus LPTIMER, BOD, CMP, and LPGPIO active						OFF					1400	nA		
STOP_4	STOP_5 plus LPRTC running from 32KHz LFXO									LPRTC + LPGPIO ON		1350	nA		
STOP_5	32KHz LFRC running, all other functions off							LFRC		LPGPIO ON		1250	nA	N/A	
I/O Domain Adder for STOP in all cases												STOP Mode Current adder $I_{VDD\_IO\_1V8}$ when VDD_VDD_IO_1V8 = 1.8V			
												200	nA		

1. If RTSS-HE is powered down then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are powered down
2. WFI: Wait for Interrupt.
3. At ACLK = 400 MHz, HCLK = 200 MHz.
4. At ACLK = 100 MHz, HCLK = 50 MHz, PCLK = 25 MHz.

3.2 Key Specification Updates

3.2.1 Source Voltage

- Signal name changes: (Datasheet Section 3.6.2)
  - VDD_3V3 is now VDD_MAIN
  - VDD_BUCK_3V3 is now VDD_BUCK
  - VDD_MIPI_0V8 is now VREG_MIPI_0V8
- Specification changes (Datasheet Section 5.2.1)
  - VDD_MAIN
    - Was 1.70V min to 4.20V max, now 1.75V min to 4.20V max
  - VDD_BUCK
    - Was 1.80V min to 4.20V max, now 1.75V min to 4.20V max
- New signal added (Datasheet Sections 3.6.2, 4.1 and 4.2)
  - VDD_PLL_0V8
    - Was previously named N.C. (no connect), now is named VDD_PLL_0V8
    - This voltage input must be connected to the VREG_CORE_0V8 voltage output
- New mandatory decoupling requirement (Datasheet Section 3.6.2)
  - VREG_AON
    - Now requires power decoupling to ground through a 1uF capacitor and a 4.7K ohm resistor in series

Note: Please see new Application Note AAPN0027, PCB Layout Guidelines for Ensemble MCUs and Fusion Processors, for detailed information about power decoupling for all power pins.

3.2.2 Watchdog Timer Function

- Watchdog timer (WDT) will not automatically generate a chip-level reset upon WDT timeout: (Datasheet Section 3.15.3)
  - Upon a WDT timeout event, a non-maskable interrupt (NMI) will be correctly generated but the configurable automatic hardware chip-level reset will not be generated in association with this WDT timeout event. The option to generate an automatic hardware chip level reset associated with a WDT timeout event is no longer possible and is removed from the specifications. Instead, A chip-level reset associated with a WDT timeout event must be implemented within the WDT NMI interrupt handler routine firmware.

3.2.3 OctalSPI Interface Speed

- Operation Speed Increase: (Datasheet Section 3.17.1)
  - Maximum frequency of both OctalSPI interfaces have increased
    - Was 80MHz SDR & 160MHz DDR max, now 100MHz SDR & 200MHz DDR max

3.2.4 Debug Trace Signals on JTAG Port Pins

- Data collected during a debug trace session cannot be transmitted externally using the JTAG debug port pins (Datasheet Section 3.21 for E1 and E3 Series, 3.22 for E5 and E7 Series)
  - Code execution tracing during debug (Arm Debug Spec ADIv6.0) is fully functional and stores the resulting trace data in on-chip SRAM that can be read out of the Ensemble device for formatting and post-analysis. However, this trace data cannot be transmitted directly from the Ensemble device to a debug probe or emulator via the four JTAG trace

data pins (JTAG_TDATA0-3). These pins and associated clock signal JTAG_TRACECLK are not functional and are removed from the specifications.

3.2.5 Fastest Peripheral Operation per Multiplexed Pin Port Option

- Guidance was added to choose the fastest operation based on selection the optimum pin/port multiplex option for interface peripherals (Datasheet Section 4.2)
    - OctalSPI interface OSPI0 has fastest operation (100MHz SDR &200MHz DDR) on signal multiplex option B
    - OctalSPI interface OSPI1 has fastest operation (100MHz SDR & 200MHz DDR) on signal multiplex option C
    - SDMMC interface has fastest operation (50MHz) on signal multiplex option C

3.2.6 On-chip Memory Access Rate

- MRAM (Datasheet Section 5.4)
    - A new DMA write mode has been added
    - Read/write times and rates have been updated
- SRAM (Datasheet Section 5.4)
    - Read/write times and rates have been added for each individual SRAM block

3.2.7 Analog to Digital Converters

- ADC12 (Datasheet Section 5.6.1)
    - Hardware averaging of at least 2 samples is required
    - Specifications have been updated
- ADC24 (Datasheet Section 5.6.1)
    - Specifications have been updated

3.2.8 WLCSP208 Package Size

- CSP208 body size (Datasheet Section 6.2.1.2)
    - Increased slightly from 7.512mm x 6.674mm, to 7.574mm x 6.850mm
    - No other mechanical dimensions have changed

Document History

Version	Change Log
1.0	Original Release, 7 Nov 2023