Functional Errata

Revision B2 Silicon

Ensemble Family

E1, E3 Series Microcontrollers
E5, E7 Series Fusion Processors

Contents

1 Document Scope and Device Identification

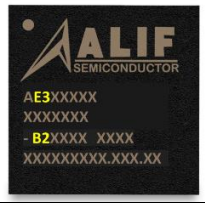
This document includes:

The **ERRATA** related to functions in silicon revision B2 of Ensemble Family devices that do not match the specifications in the published v2.6 datasheets. Functional limitations resulting from these errata for silicon revision B2 will be corrected in the coming silicon revision B3. The specifications in version v2.6 datasheets represent the function of the coming silicon revision B3 devices.

Current Datasheet Reference:

Document Number	Version	Datasheet Description
ADTS0008	v2.6	E1 Series MCUs
ADTS0007	v2.6	E3 Series MCUs
ADTS0006	v2.6	E5 Series Fusion Processors
ADTS0005	V2.6	E7 Series Fusion Processors

Listed Errata in this Document are Applicable to Silicon Version: Revision B2
B2 Silicon Device Marking Identification: See images below.

Device Series	FBGA194 Package	WLCSP208 Package
E1		N/A
E3		
E5		
E7		

2 ERRATA

2.1 USB Host Mode is Not Enabled

Applies to:
E1, E3, E5, E7 devices.

Description
The USB 2.0 Low Speed/Full Speed/High Speed interface will not support USB Host mode. Only USB Device mode is supported.

Workaround
While there is no workaround for revision B2 devices, **this limitation will be removed in revision B3 devices where USB Host mode will be operational, as well as USB Device mode**.

2.2 Limitations to Restarting some Clock Sources that Originate from PLL

Applies to:
E1, E3, E5, E7 devices.

Description
Powering on the PLL by software command after the PLL was previously powered off by software command may result in an incorrect clock frequency on the 160MHz or 80MHz branches of the clock tree, both of which originate from the 480MHz portion of PLL outputs. There are no problems with any other clock branches derived from the PLL related to this software-initiated power cycle sequence.

160MHz and 80MHz clock sources affect the operation of the RTSS-HE (Real Time Subsystem – High Efficiency) that includes the M55-HE (Cortex-M55 160MHz CPU core) and the NPU-HE (Ethos-U55 128 MAC NPU accelerator).

When this issue occurs, it is possible that the frequency of either the 160MHz or the 80MHz clock source will be above or below their expected frequencies.

Please note that there are no clocking problems if the PLL is powered on from a device cold power up cycle and the PLL is not subsequently powered off and powered back on via software.

Workaround
Use any one of these methods to avoid clocking issues:

- Do not choose to use the 160MHz or 80MHz clock source for operating the RTSS_HE, instead choose either the 120MHz or 60MHz clock source.
- Use the 160MHz or 80MHz clock source but delay at least 150us before issuing a software command to repower the PLL after a previously commanding the PLL power off via software.
- Use the 160MHz or 80MHz clock source but maintain PLL power during STANDBY mode (do not turn off the PLL via software). This will add about 800uA at 3.3V to the STANDBY mode current.

These clocking limitations will be removed in revision B3 devices

2.3 Excessive STOP Mode Current Consumption

Applies to:
E1, E3, E5, E7 devices.

Description
The current consumed in the STOP power mode will be approximately 1200 nA higher than the specified values. 1200 nA should be added to each of the specifications for datasheet parameters STOP_1, STOP_2, STOP_3, STOP_4, and STOP_5 that appear in the table 5.5 of section 5.2.2.1 of each datasheet.

Workaround
While there is no workaround for revision B2 devices, **this excessive STOP mode current will not be present in revision B3 devices.**

2.4 Inaccuracy of Internal Temperature Sensor

Applies to:
E1, E3, E5, E7 devices.

Description
The internal temperature sensor (TSENS) when read by the ADC12 converter will reflect a temperature accuracy of +/- 10 °C and will have no path to calibrate to an accuracy of +/- 1 °C. The TSENS accuracy specification should be +/- 3.0 °C, with a path to calibrate to +/- 1.0 °C. Refer to datasheet section 3.20.5 for series E1 and E3, section 3.21.5 for series E5 and E7 devices.

Workaround
While there is no workaround for revision B2 devices, this TSENS inaccuracy will not be present in revision B3 devices and the performance will meet the specification of +/- 3.0 °C, with a path to calibrate to +/- 1.0 °C**.**

Document History

Version	Change Log
1.0	Original Release, 7 Nov 2023
1.1	Updated 4 Dec 2023 • Modified section 3.2.2 to indicate WDT has no issue with chip-level reset in APSS. Issue is only with RTSS • Modified section 3.2.8 to add additional info regarding bump distance from edge for WLCSP208 • Added new sections 3.2.9, 3.2.10, 3.2.11, 3.2.12
1.2	Updated 4 Jan 2024 • Added new sections 2.3, 2.4, 3.2.13
1.3	Updated 16 Jan 2024 Changed reference to datasheet version. Was referencing Ensemble datasheets version v2.5, now referencing datasheets version v2.6. This document no longer includes specification changes because all previous specification changes are now incorporated into v2.6 datasheets. This document now includes only specification errata.