ALIF SEMICONDUCTOR

Autonomous Intelligent Power Management (aiPM™): Simplifying power management and eliminating the PMIC

On-Device AI/ML Applications Photo credit: Adobe Stock

Introduction

Most edge solutions are battery powered and therefore must be power-optimized to maximize battery life in between charges/ battery replacements. On a massive scale, this optimization reduces the amount of maintenance required with a wireless sensor network (WSN) installation, saving time and cost. On a smaller scale, such as consumer applications where the user is responsible for device maintenance, it makes for a much more seamless user experience without the need to be tethered to an outlet or a power bank to recharge the device.

The task of maximizing battery life has been ongoing for intelligent, connected devices: power efficient protocols such as BLE have been put in place to ensure less power is taken from radio transmission. Furthermore, in the mission to minimize latency, there is a high requirement for local processing where AI/ML algorithms are run closer to the edge. In some ways, edge computing forces a much higher burden on power management, in others, it can remove the need for a frequent connection to the cloud — a process that is power intensive with its frequent radio transmissions — to remove a large power burden from the entire system (edge to cloud).

In this drive to maximize battery life, it is important that all processing occurring on the device itself is run as efficiently as possible, while the device is turned off as much as possible, drawing almost negligible amounts of current. Even within the field of consumer appliances, including just about anything that is plugged into a wall and never unplugged (e.g., chargers, TV adapters, washing machines, etc.), there is now a desire to minimize “vampire power”, or the power that is drawn by the device while on standby.

Battery capabilities expectations call for intelligent power handling from the system level down to chip level. Alif Semiconductor® addresses these expectations on all of its MCUs with its exclusive Autonomous Intelligent Power Management (aiPM™) technology that allows fine-grained control of when resources in the chip are being powered. This technique produces best-in-class low-power operation allowing intelligent devices to last longer on smaller batteries. This article dives into the need for more efficient device processing for edge devices and how aiPM enables unrivaled power performance in this industry.

The Edge Device Processing Gap

In every industry there is now a breadth and depth of technology that aims to support this constant expansion of edge devices. Much of the hardware meant to support this ecosystem is separated into distinct functional blocks (e.g., wireless ICs, chipsets, PMICs, etc.) with updates to these products often resulting in the limitation of backwards compatibility with legacy products, IP, and silicon processes. This limitation leaves major gaps in terms of security, connectivity, hardware acceleration, integration, and software reuse. These gaps become more apparent with the increasing utilization of edge computing with intelligence being brought closer to the device, putting a compute burden on the already space-and power-constrained applications.

Alif Semiconductor addresses this niche with the introduction of efficient microcontroller platforms, such as the Alif Ensemble® and Balletto™ families with high-performance and high-efficiency cores. The Ensemble family (e.g., E1, E3, E5, and E7) begins with single-core Arm Cortex-M55 MCUs with an optional dedicated Ethos-U55 microNPU for accelerating ML workloads. The MCUs can be scaled up to triple-core and quad-core "fusion processors" (E5, or E7) which combine MCU, MPU, and NPU in a single device.

The Balletto family builds upon this with the addition of BLE 5.3 and IEEE 802.15.4 wireless connectivity. aiPM technology underpins all of these MCUs by dynamically powering only the logic and associated memory that are in use at any given time, offering extremely low power consumption relative to alternative low-power architectures. **(Figure 1)**

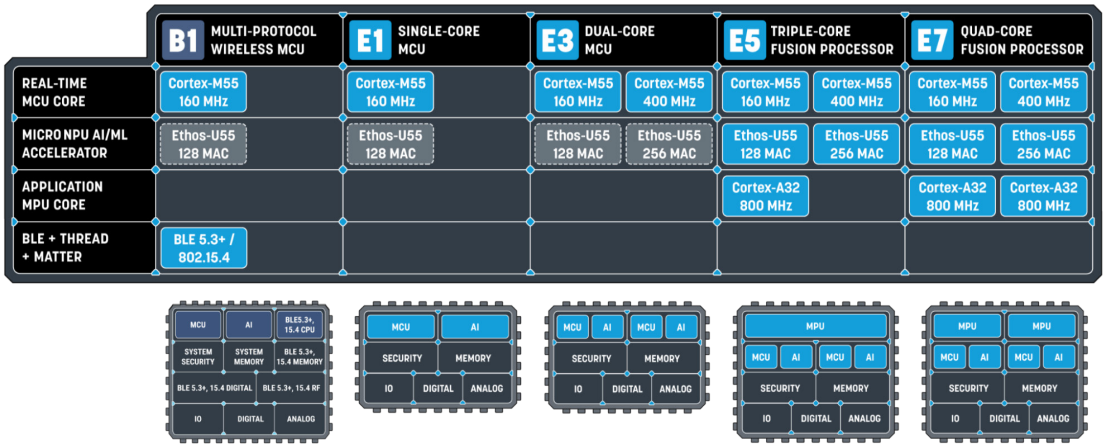


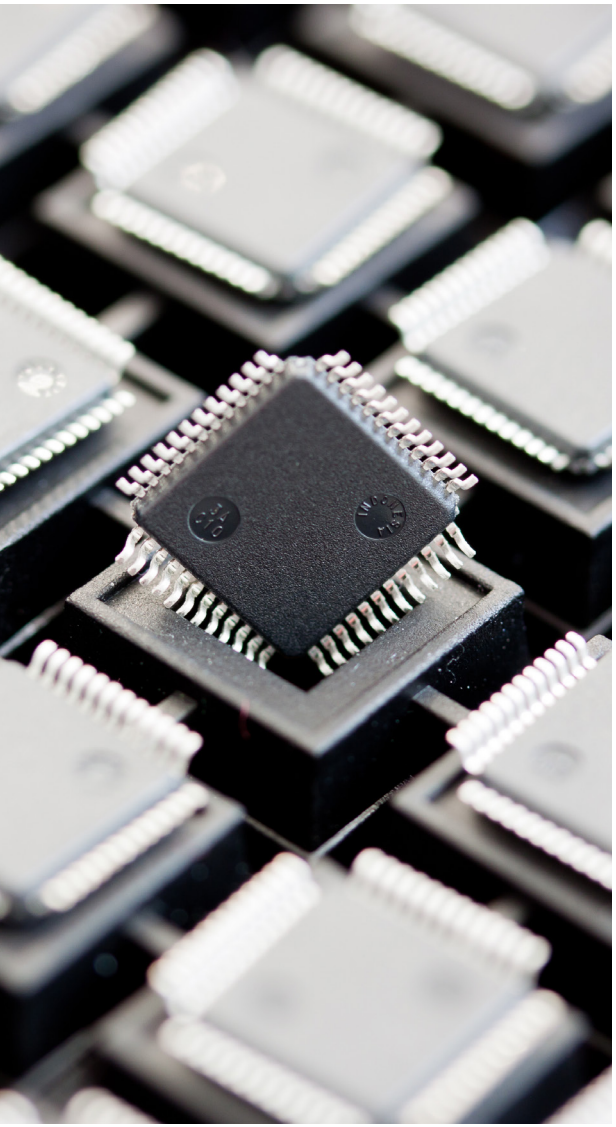
Figure 1: Alif Semiconductor's portfolio fills the gap for edge devices by providing highly-optimized cores that can be scaled up or down depending upon the application.

What is aiPM?

aiPM technology uses power saving features such as running at high or low frequencies, clock gating as necessary, powering off unused regions, and sleeping for extended periods to accomplish ultra-low power consumption that address the power requirements of the application with agility. The five available modes include: RUN, READY, IDLE, STANDBY, and STOP.

Power consumption measurements were taken of an Alif MCU device pin while operating at 3.3 V: In STOP mode the device runs at less than 1.6 µA with the real-time clock (RTC) running and wake sources active. In RUN/GO mode, the device consumes 27 µA/MHz with Cortex-M55 CPU running code from SRAM.

Multi-core devices are designed such that the Cortex-M55 MCU/Ethos-U55 NPU pair can operate at very low power levels whilst sensing the surroundings (vibration, motion, acoustics, video). The high-efficiency Cortex-M55 MCU will then wake up other portions of the device



Integrated circuits Photo credit: Adobe Stock

such as the Ethos-U55 NPU, the Cortex-A32 MPU(s), graphics, USB, etc., in an iterative approach to execute the workload based on the immediate use case. Finally, aiPM technology will ensure each section is shut off when it is no longer needed.

How aiPM Solves Existing Power Management Challenges

The Need for External Power Management

The task of power management for the embedded system is generally complex and it is typically not integrated into the chip itself. PMICs are a common solution to generate several voltage rails from a single source by integrating a number of functions such as DC-DC conversion, linear regulation (LDOs), battery charging, and power sequencing. In battery-powered designs for example, the PMIC will remove the need for a control interface, automatically handling charging/discharging of the battery. When chips are paired with external sensors and peripherals, a PMIC is often necessary to regulate voltage to the different loads.

The solution is perfectly sufficient for an embedded design, however, PMICs are still often necessary to handle the power management of the chip itself. Older MPUs, for instance, often need an external source to manage the voltage supplied to the core while MCUs tend to handle power management internally.

A PMIC is almost always needed for more specialized chipsets such as multiprotocol wireless MCUs. Low-power MCUs will also often have a power management unit (PMU) or PMIC that must be used in order to activate the various “supply modes” of the MCU itself by, for instance, controlling various regulators or enabling the specific power supply sequences required for various use cases. This brings added cargo to the end solution, increasing both cost and space. With aiPM, all power modes are readily managed. In addition, with internal power conditioning, sequencing, and regulation **(Figure 2)**, aiPM can take the place of separate power management ICs (PMICs).

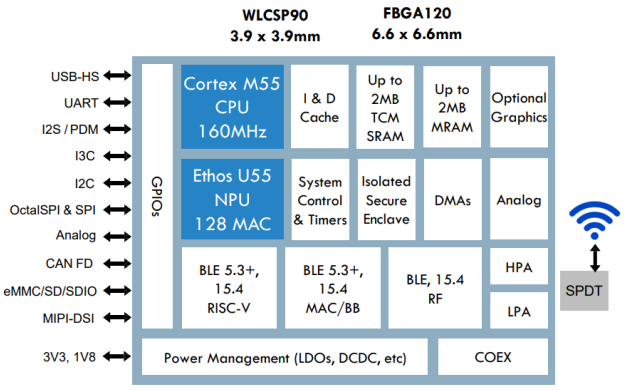


Figure 2: Balletto has integrated power conditioning circuitry that allows it to take the place of many PMICs.

The Difficulty with Enabling Power Saving Modes

As stated earlier, the need for external hardware to enable the power saving modes of the processor could further complicate an embedded solution, requiring customers to stay within an ecosystem to simplify development and speed time to market. This complication can potentially cause difficulties for upgrades to outdated devices and compatibility issues when diverging from the established hardware solution. The aiPM solution is integrated within each of the Alif Semiconductor chips where sections of the chip are on only when they are needed, and off when they're not. This is based on the immediate processing load-per-use case making even the complex quad-core devices behave like small purpose-built low-power MCUs when they need to. Software implementation is also eased where all that is needed from the developer is to call the aiPM API and have it power off the CPU. It will check if all cores are done processing, or if the chip still has work to do, and autonomously bring the device down to the lowest possible state it can operate in through clock-gating.

The concept of the Internet of Things Photo credit: Adobe Stock

Conclusion

Edge devices are often powered by small batteries in enclosures with considerable size constraints, from smartwatches and TWS earbuds to streetlamps in smart cities. These power and size considerations have tightened even further by adding more computing power to these devices with the requirement to process complex AI/ML algorithms to provide a seamless user experience or in edge computing applications. Power-hungry data processing puts further strain on the battery, calling for more efficient use of the processing resources.

Alif Semiconductor addresses these battery issues by leveraging high-performance, high-efficiency cores in each of their MCUs. Separated by different operating modes, these cores will employ various power saving features to ensure the lowest amount of power is being consumed for the given task. The underlying aiPM technology allows developers to easily enable fine-grained power management in each of Alif Semiconductor's chips based upon their application.

Alif's highly integrated technology platforms include the power management circuitry found in PMICs, often removing the need for a separate IC for power management. This integration eases both the size and power design constraints on embedded applications while removing the added BOM costs from extra components.

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