

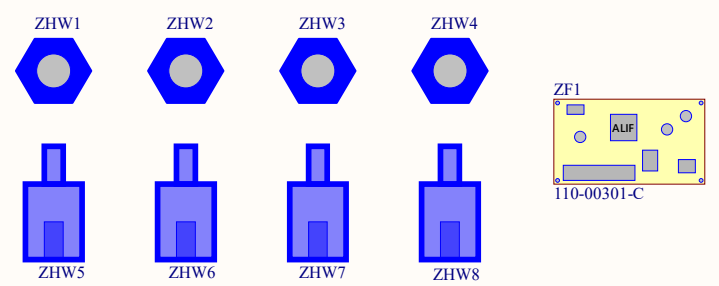
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REVISION	DESCRIPTION	DATE	APPROVED

Revision History:

REV	DATE	Description:
B	25-MAY-2022	Initial Release, copied from 120-00301-B
C	15-JUN-2023	Fixed swapped MIPI_CSI_C pair with MIPI_CSI_0 pair on BGA194

**Required 2.54mm Shunts:**  
**J5** VDD\_3V3 Current Measurement  
**J6** VDD\_1V8 Current Measurement  
**J7** Battery Current Measurement  
**J8-1 J8-2** FLEXIO = 1.8V \* default  
**J8-2 J8-3** FLEXIO = 3.3V  
**J9-1 J9-2** SD Flash Power = 3.3V \* default  
**J9-2 J9-3** SD Flash Power = 1.8V for "LV" Cards  
**J13-1 J13-2** Click Board Power = 1.8V \* default  
**J13-3 J13-4** Click Board Power = 3.3V  
**J13-5 J13-6** Click Board Power = 5.0V  
**J19-1 J19-2** Camera Analog V = 2.8V  
**J19-2 J19-3** Camera Analog V = 2.6V \* default  
**Optional 2.54mm Shunts:**  
**J26-1 J26-3 and J24-2 J24-4** UART2  
**J26-3 J26-5 and J24-4 J24-6** UART4 \* default

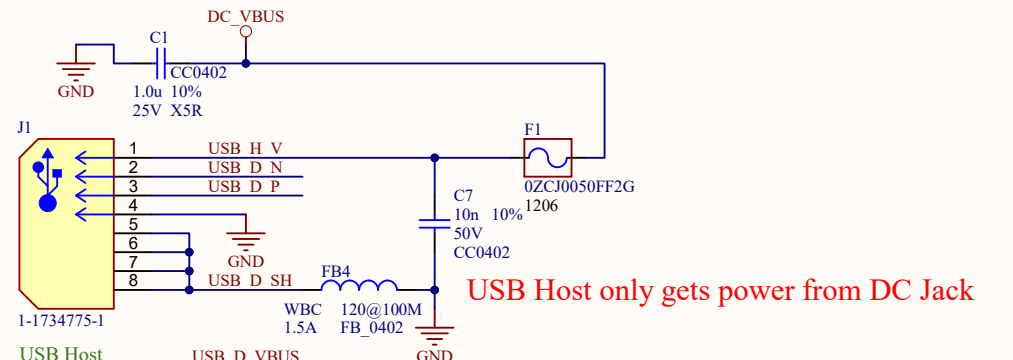


Nylon Mounting Hardware (H1 - H4)

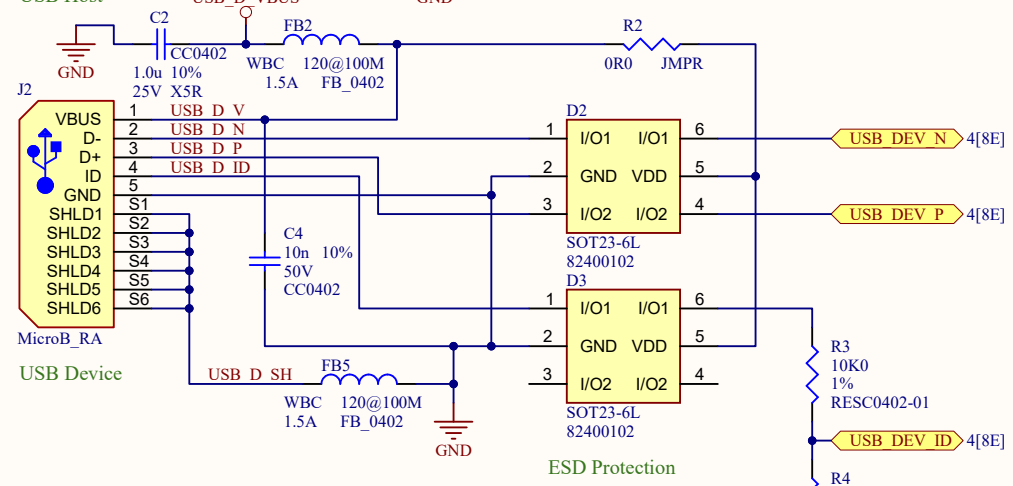
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ENG: K Braun	--/--	00301	PROJECT REVISION: Not in version control	DOCUMENT REVISION: Not in version control
DSN: K Braun	--/--		DESIGN ITEM: Not in version control	
CHK: n/a	--/--		TITLE	
REFERENCE DOCUMENTS			<b>ENSEMBLE DEV KIT BOARD</b>	
BOM: 251-00301		SIZE	CAGE CODE	DWG NO.
ASSY DWG: 121-00301		<b>B</b>	none	221-00301
FAB DWG: 211-00301		SCALE: none	FILE NAME	1-RevisionHistory.SchDoc
PCB DWG: 110-00301-C			SHEET	1 OF 12

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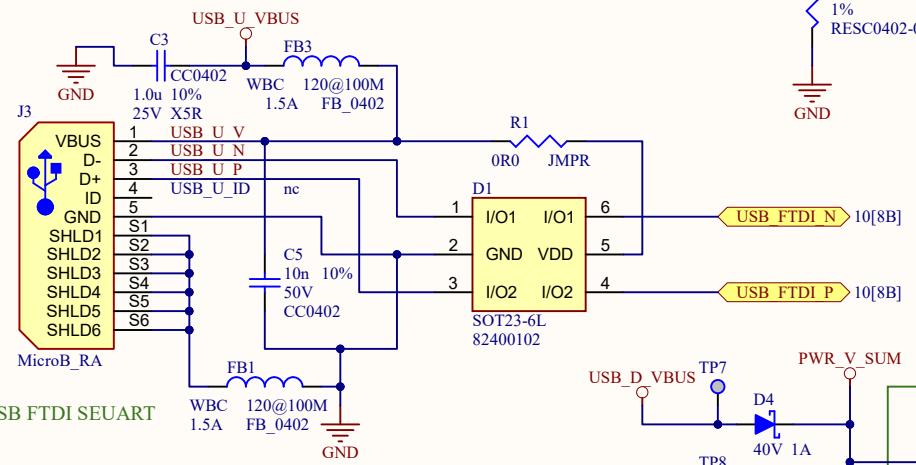
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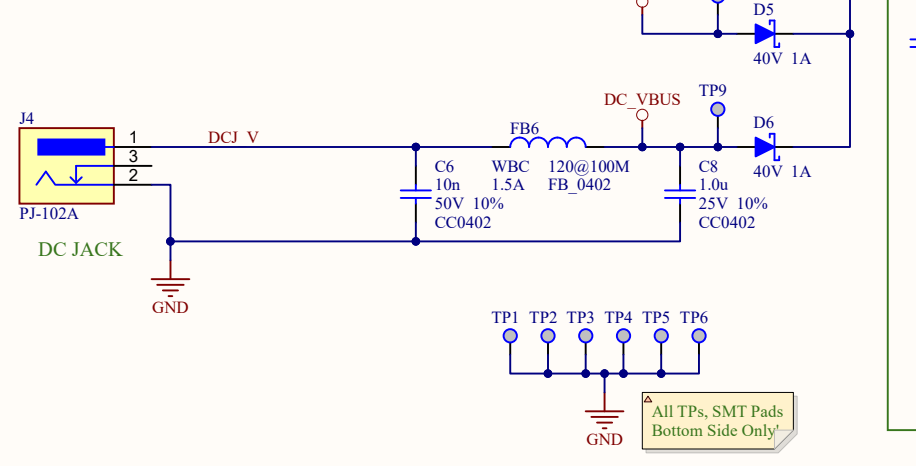
USB Host only gets power from DC Jack



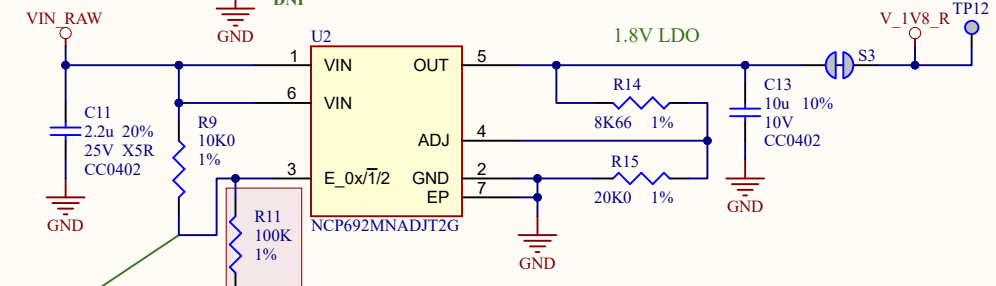
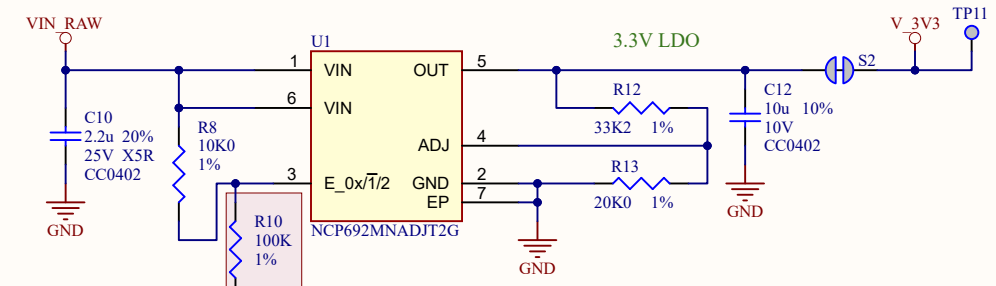
ESD Protection



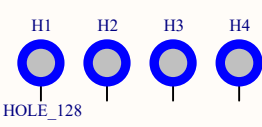
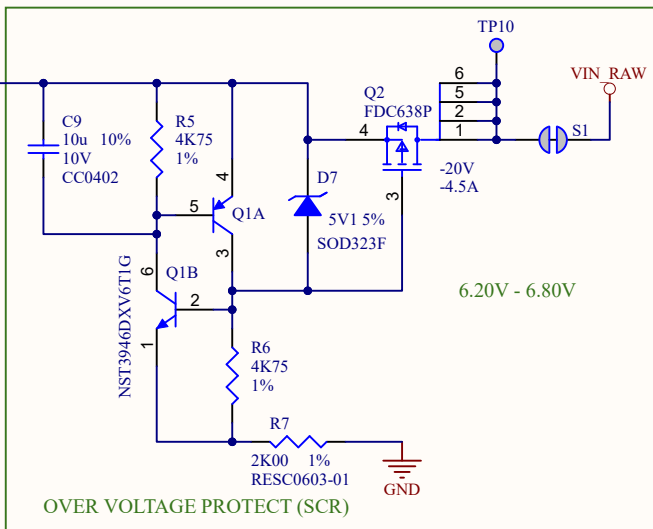
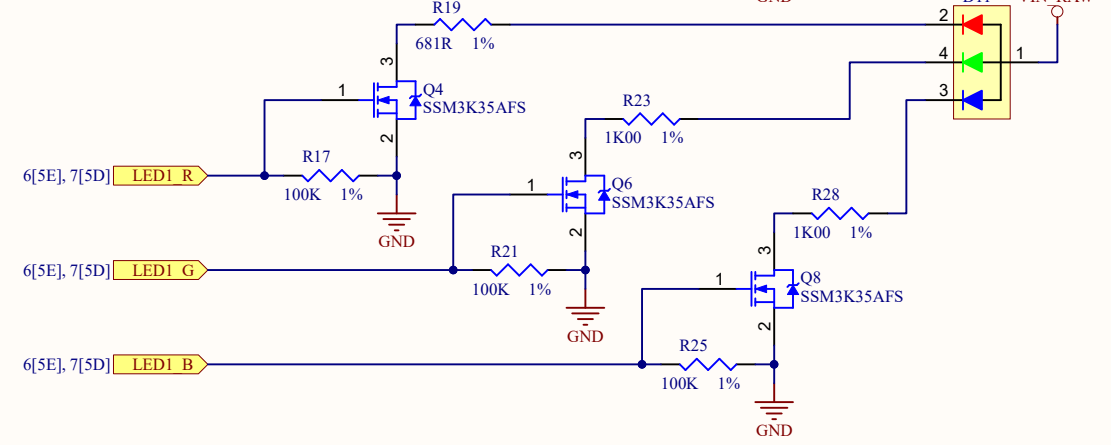
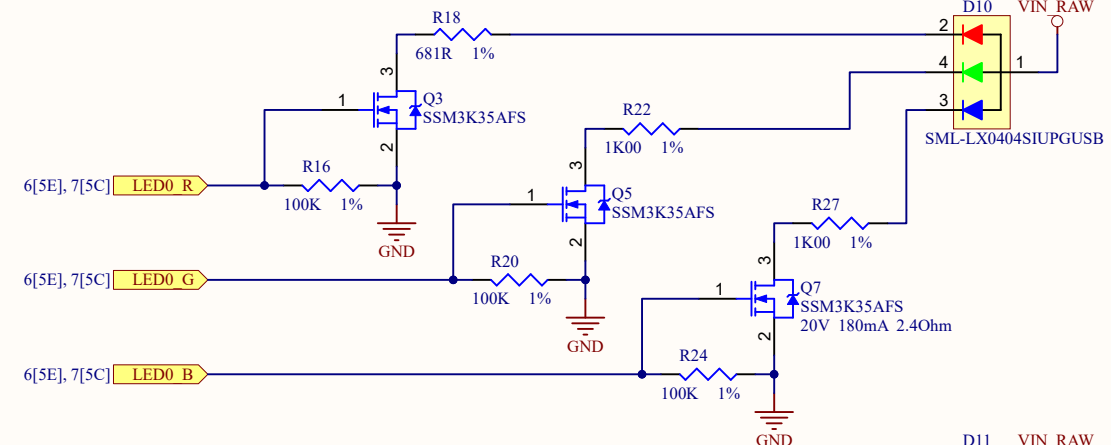
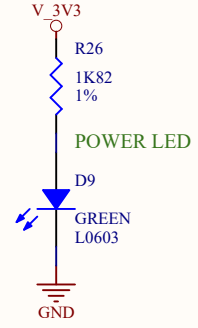
USB FTDI SEUART



All TPs, SMT Pads Bottom Side Only



Device	R(raw) out	R(gnd) out
NCP690	out	out
NCP691	out	in
NCP692	in	out

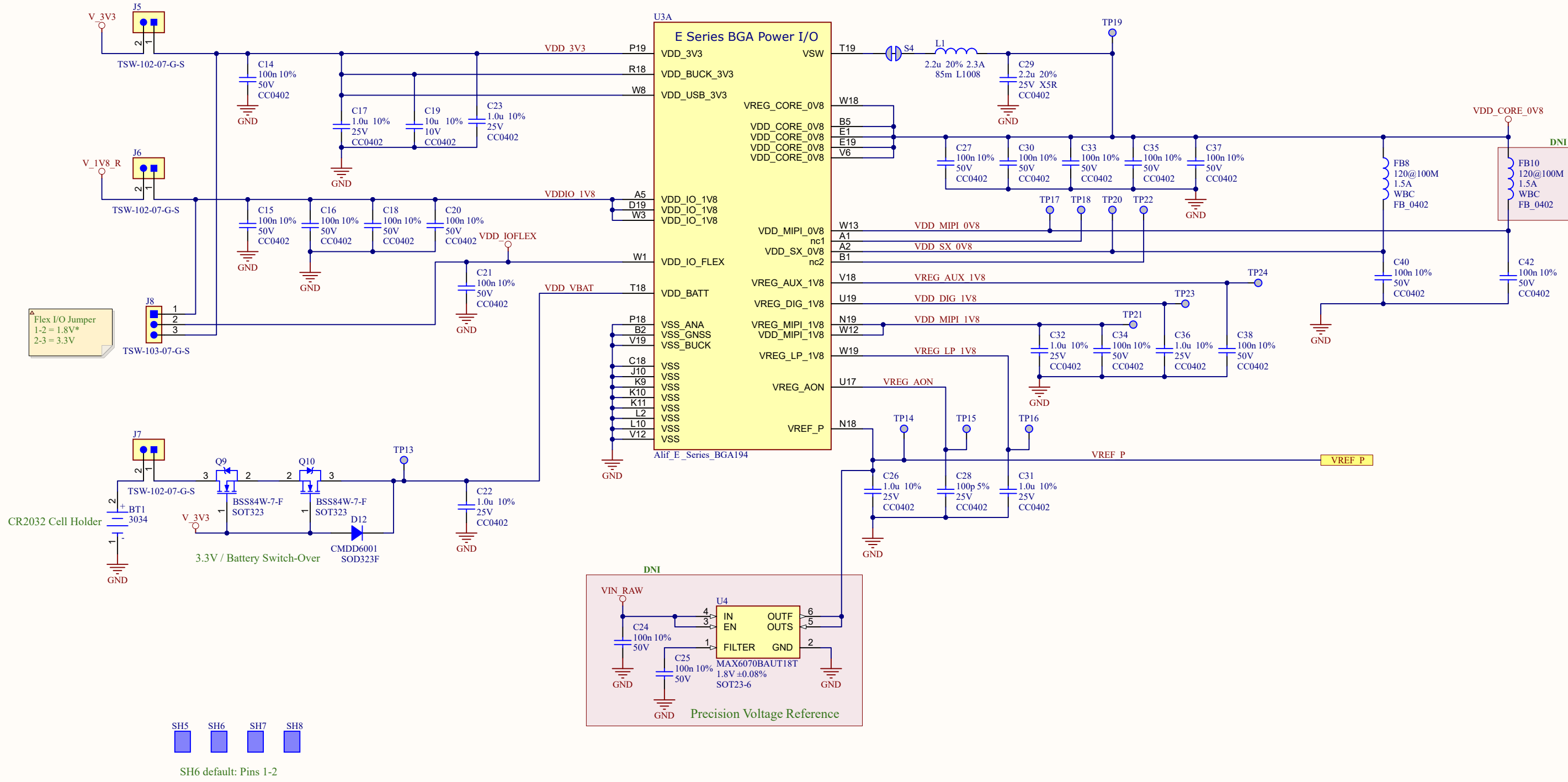


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DSN: K Braun	--/--	PROJECT REVISION: Not in version control	DESIGN ITEM: Not in version control
CHK: n/a	--/--	TITLE: ENSEMBLE DEV KIT BOARD	
REFERENCE DOCUMENTS		BOM: 251-00301	
ASSY DWG: 121-00301	SIZE: B	CAGE CODE: none	DWG NO.: 221-00301
FAB DWG: 211-00301	SCALE: none	FILE NAME: 2-PowerInput.SchDoc	REV: 2
PCB DWG: 110-00301-C	SHEET 2 OF 12		

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221-00301	DWG. NO.	3	REV. SMT.
REVISION	DESCRIPTION	DATE	APPROVED

### CPU Power Supplies

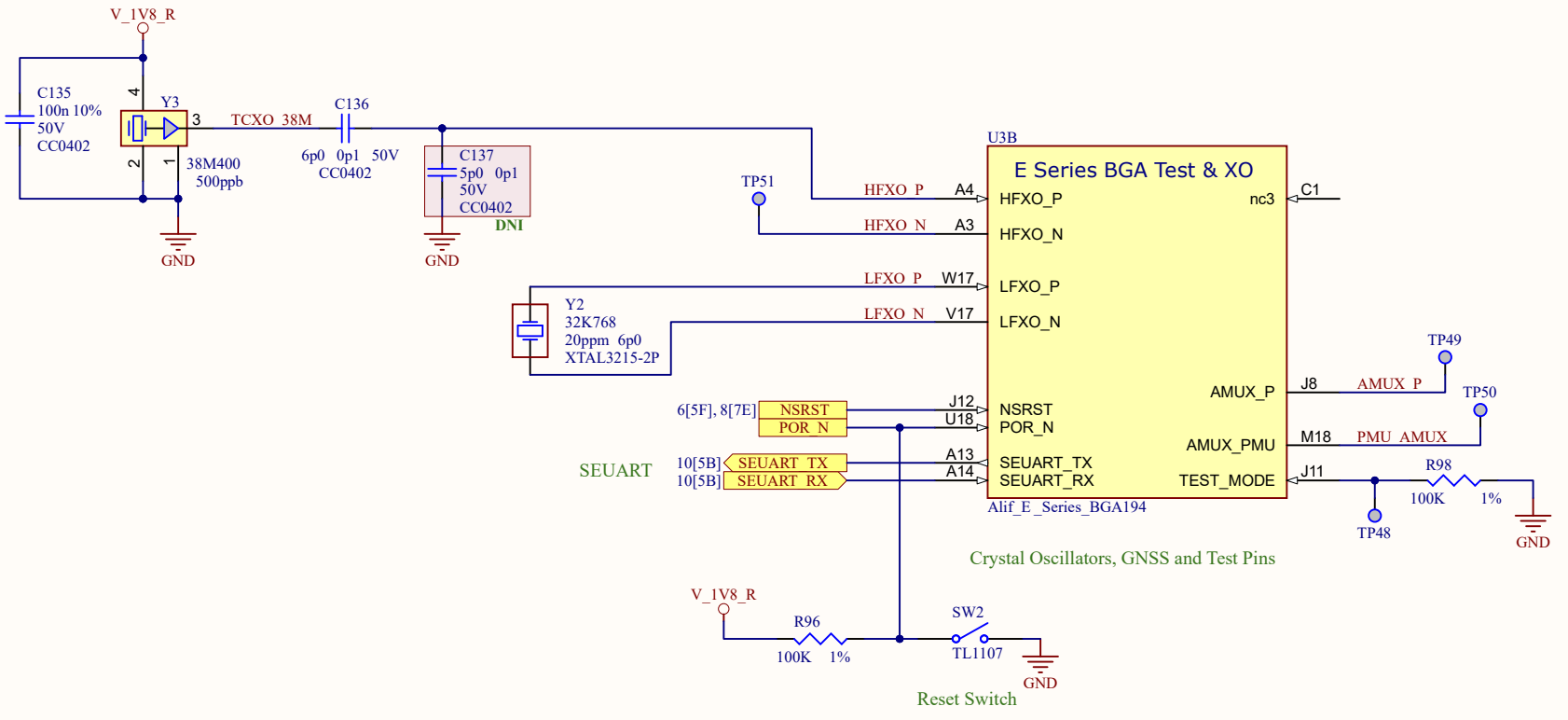
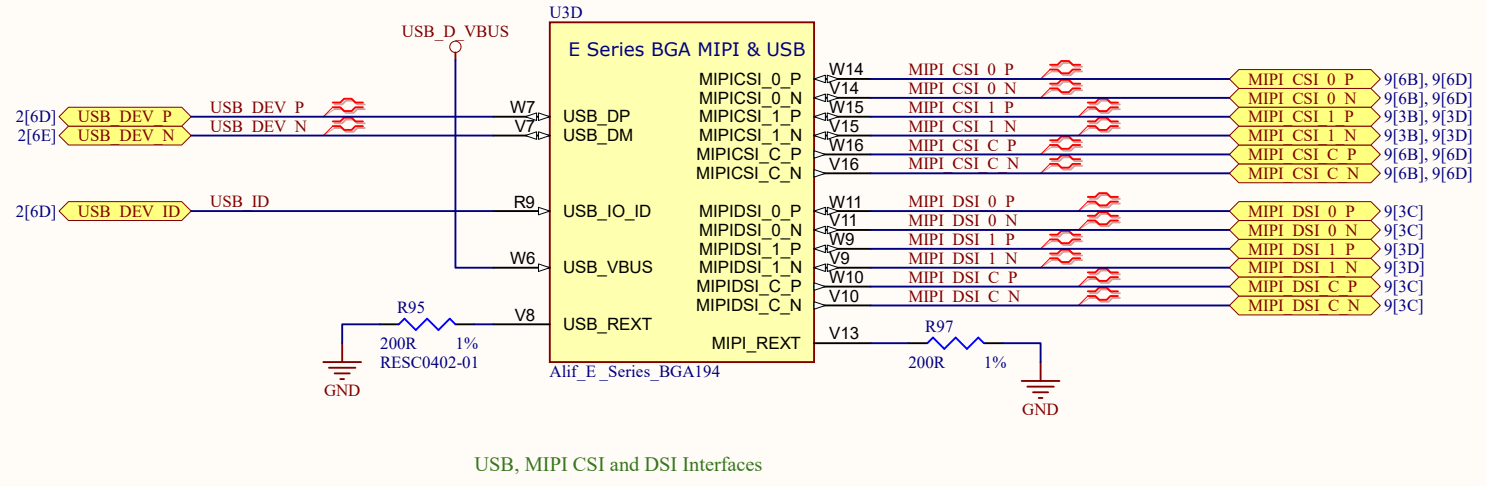


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DSN: K Braun	--/--	PROJECT REVISION: n/a	DOCUMENT REVISION: Not in version control	DESIGN ITEM: Not in version control
CHK: n/a	--/--	TITLE		
REFERENCE DOCUMENTS				
BOM:	251-00301	ENSEMBLE DEV KIT BOARD		
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FAB DWG:	211-00301	SCALE: none	FILE NAME: 3-CPUPower.SchDoc	REV: 3
PCB DWG:	110-00301-C	SHEET 3 OF 12		

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221-00301  
DWG. NO. REV. SMT.

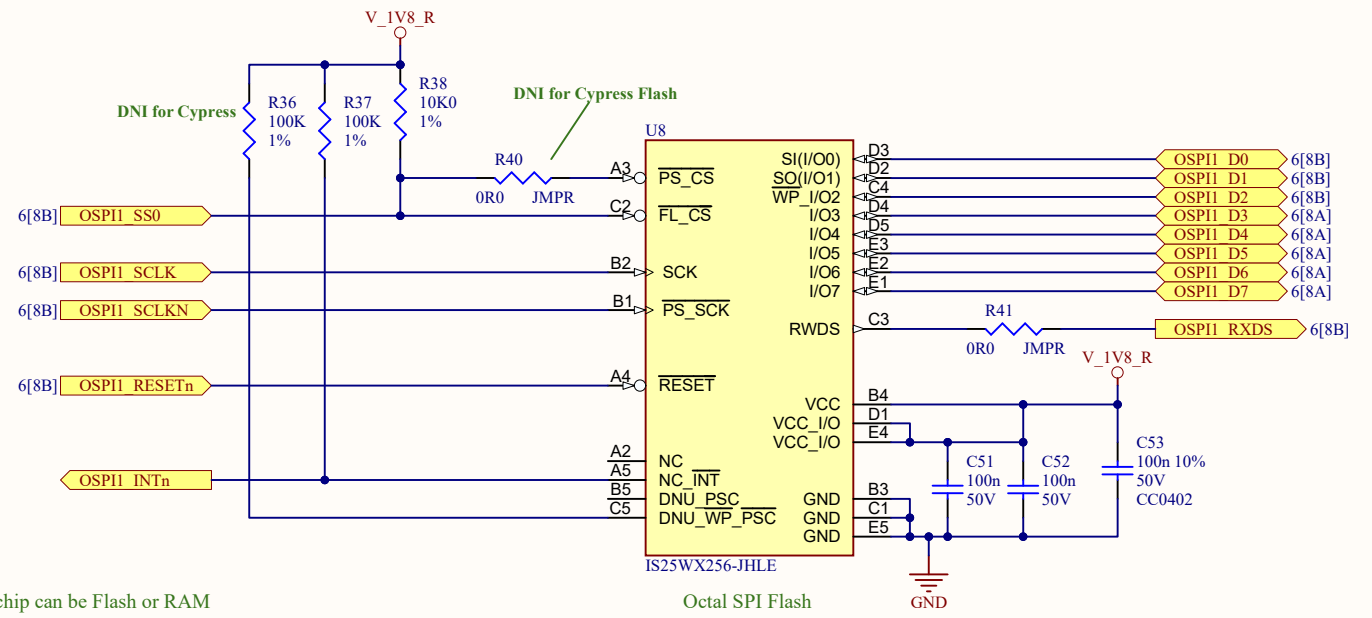
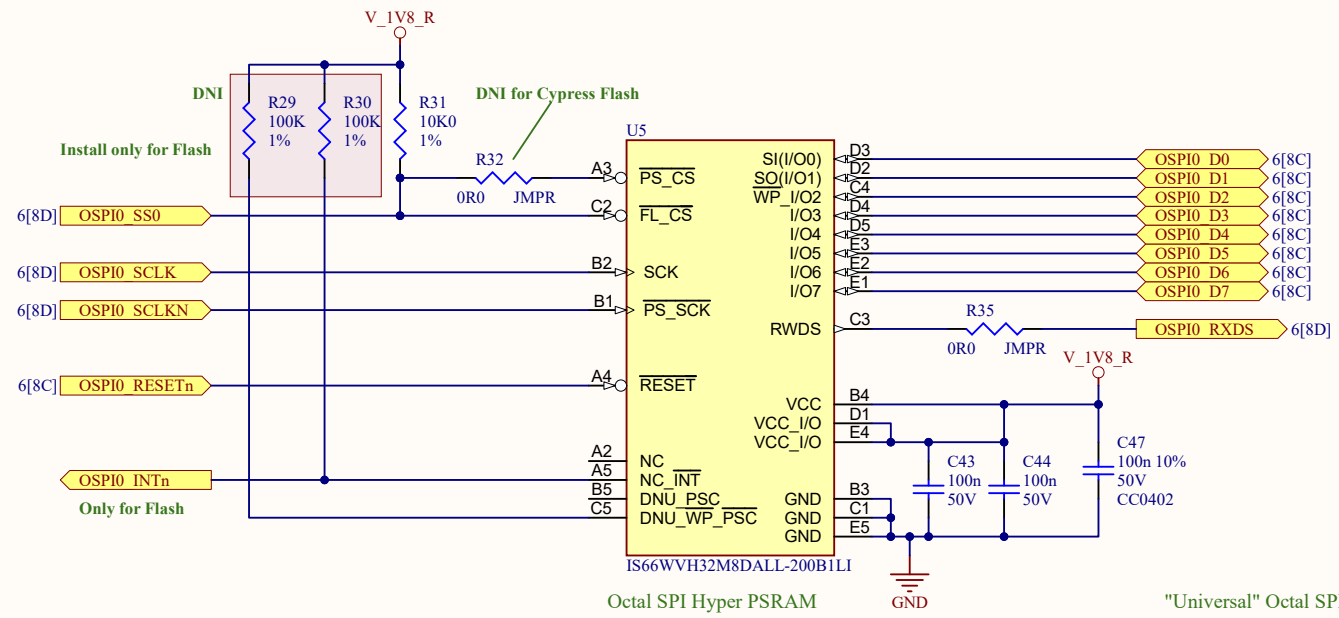
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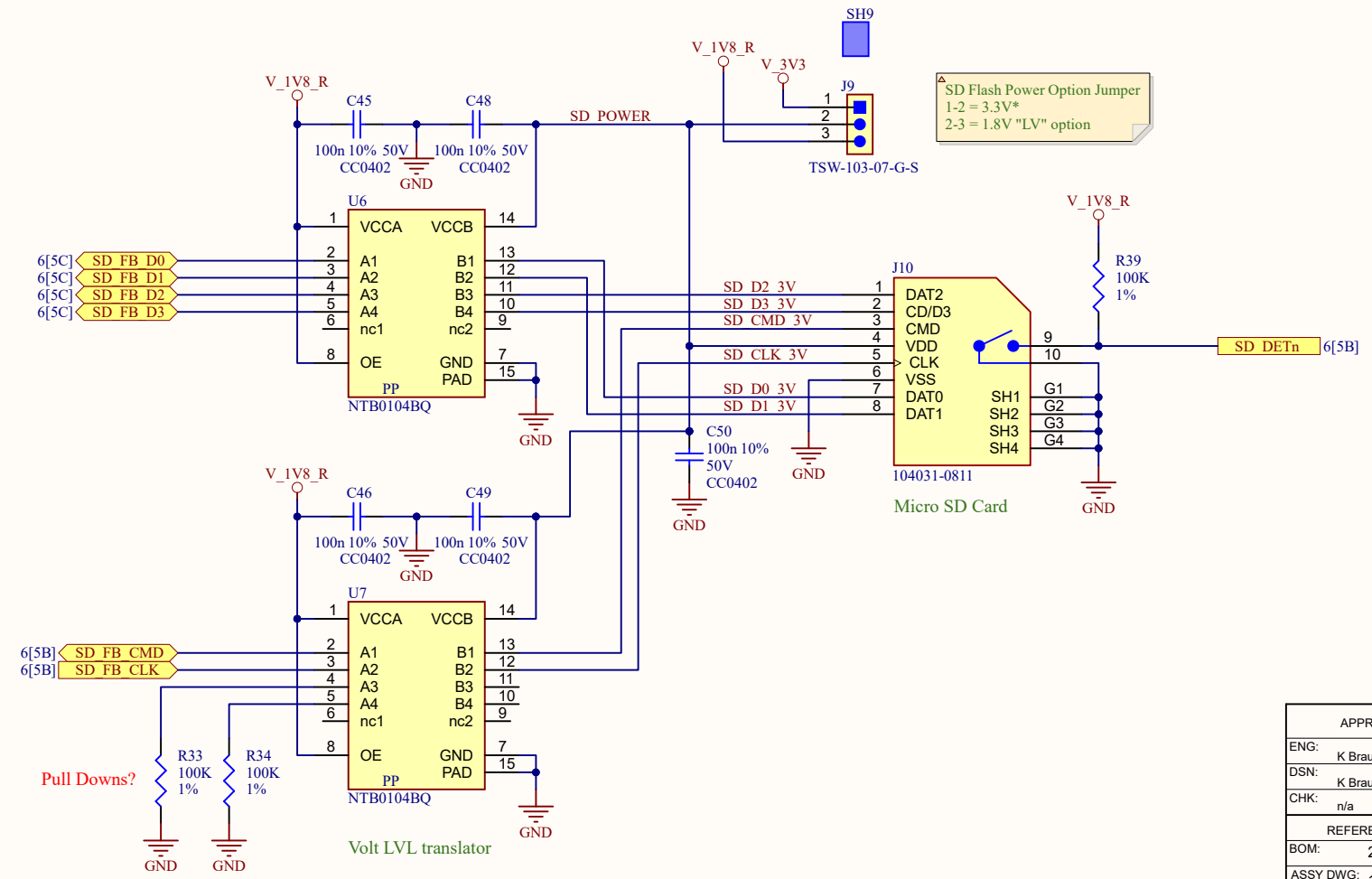
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DSN: K Braun	--/--	PROJECT REVISION: Not in version control	DOCUMENT REVISION: Not in version control	DESIGN ITEM: Not in version control
CHK: n/a	--/--	TITLE: ENSEMBLE DEV KIT BOARD		
REFERENCE DOCUMENTS		BOM: 251-00301		
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FAB DWG: 211-00301	SCALE: none	FILE NAME: 4-CPUMipiXo.SchDoc	SHEET 4 OF 12	
PCB DWG: 110-00301-C				

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"Universal" Octal SPI Devices. Either chip can be Flash or RAM



SD Flash Power Option Jumper  
 1-2 = 3.3V\*  
 2-3 = 1.8V "LV" option

Pull Downs?  
 R33 100K 1%  
 R34 100K 1%

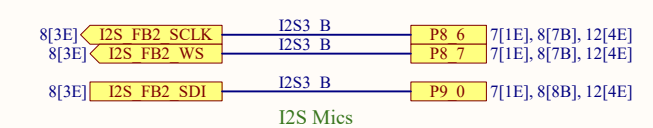
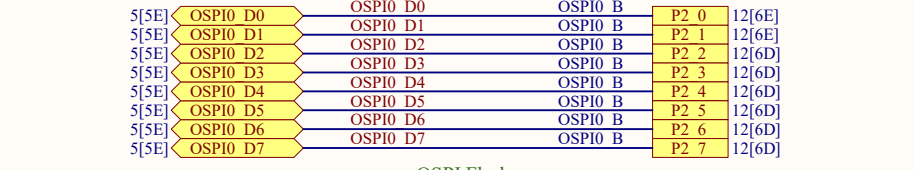
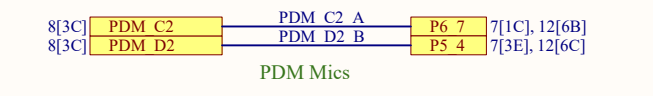
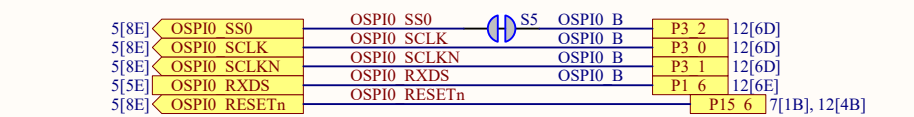
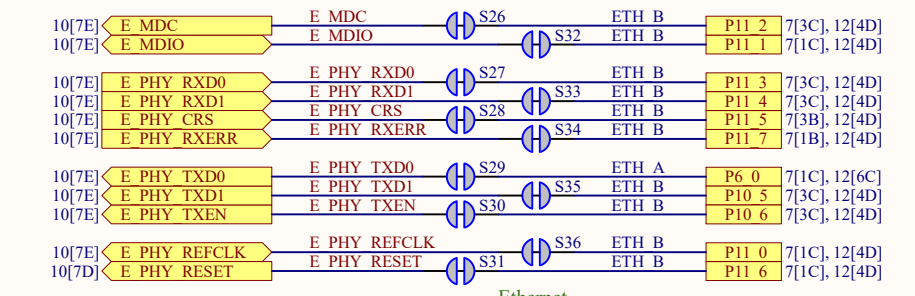
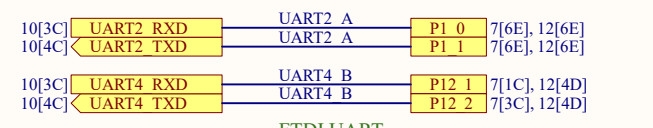
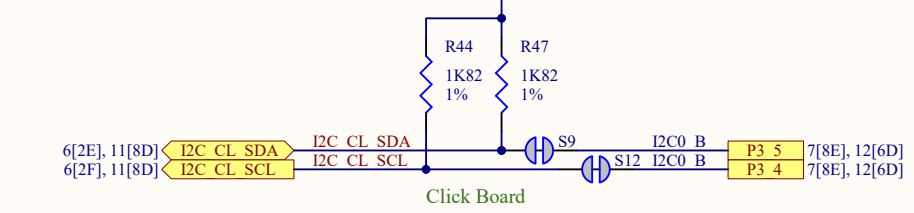
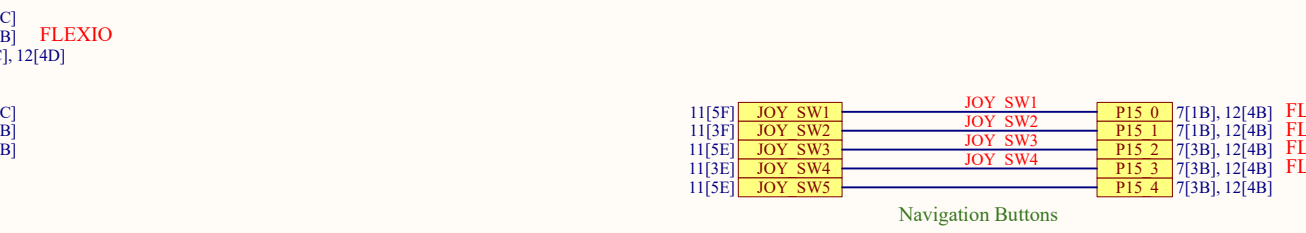
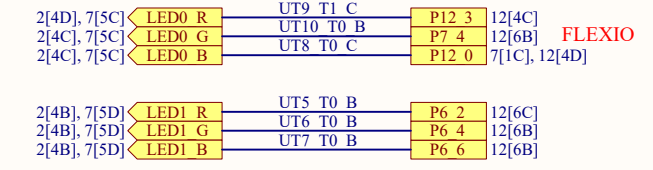
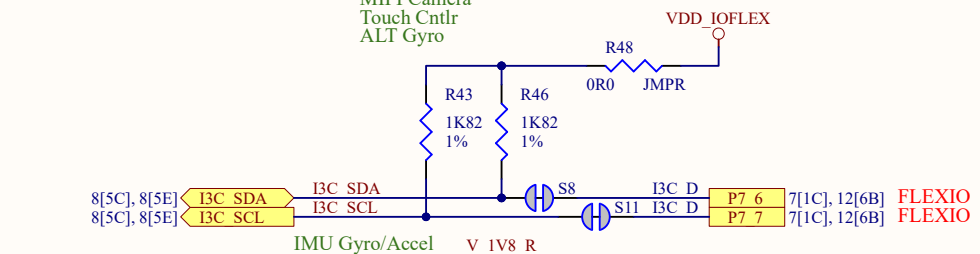
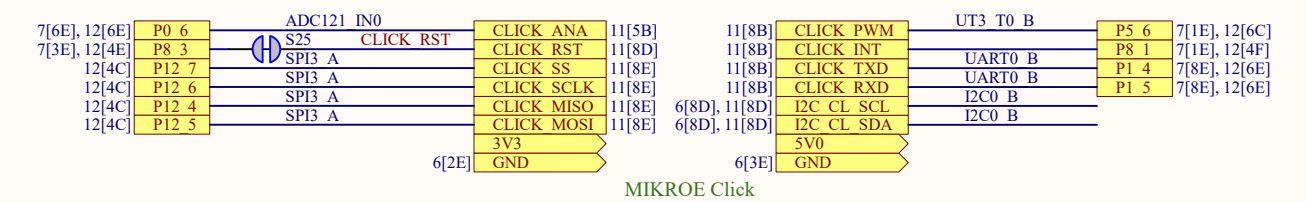
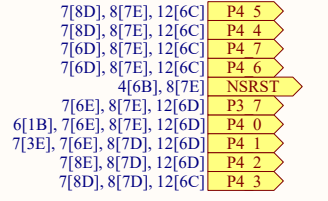
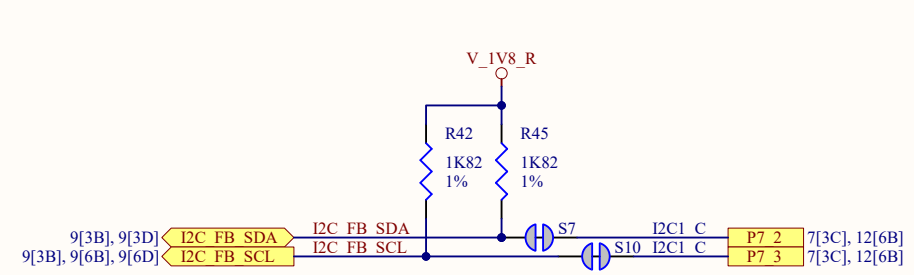
Volt LVL translator

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<b>ENSEMBLE DEV KIT BOARD</b>			
BOM: 251-00301	ASSY DWG: 121-00301	SIZE: B	CAGE CODE: none
FAB DWG: 211-00301	PCB DWG: 110-00301-C	SCALE: none	FILE NAME: 5-Memory.SchDoc
		DWG NO.: 221-00301	REV: 5
		SHEET: 5	OF: 12

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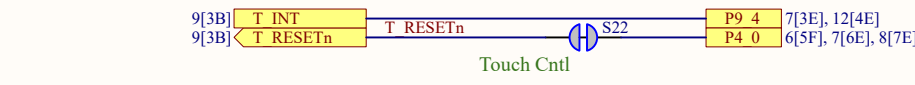
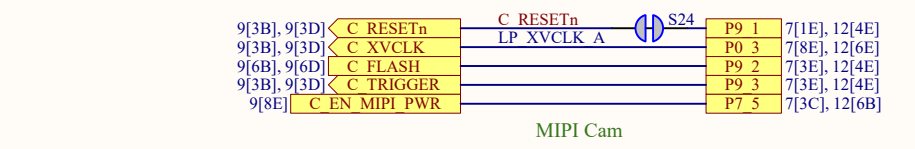
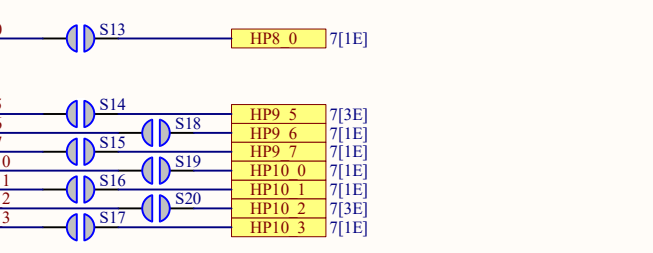
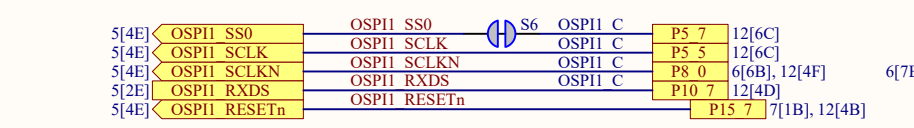
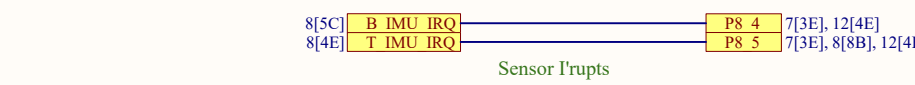
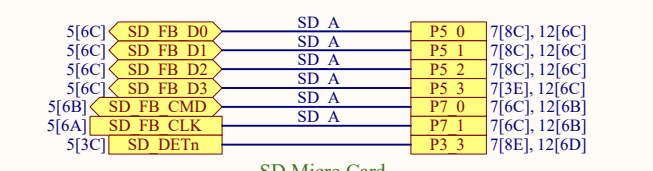
REVISION	DESCRIPTION	DATE	APPROVED

JTAG0\_TRST (no need)  
 JTAG0\_TMS  
 JTAG0\_TCK  
 JTAG0\_TDO  
 JTAG0\_TDI  
 JTAG0\_NSRST  
 JTAG0\_TRACECLK  
 JTAG0\_TDATA0  
 JTAG0\_TDATA1  
 JTAG0\_TDATA2  
 JTAG0\_TDATA3



OSPI0\_B and OSPI1\_C are tuned in the B0 silicon for maximum performance

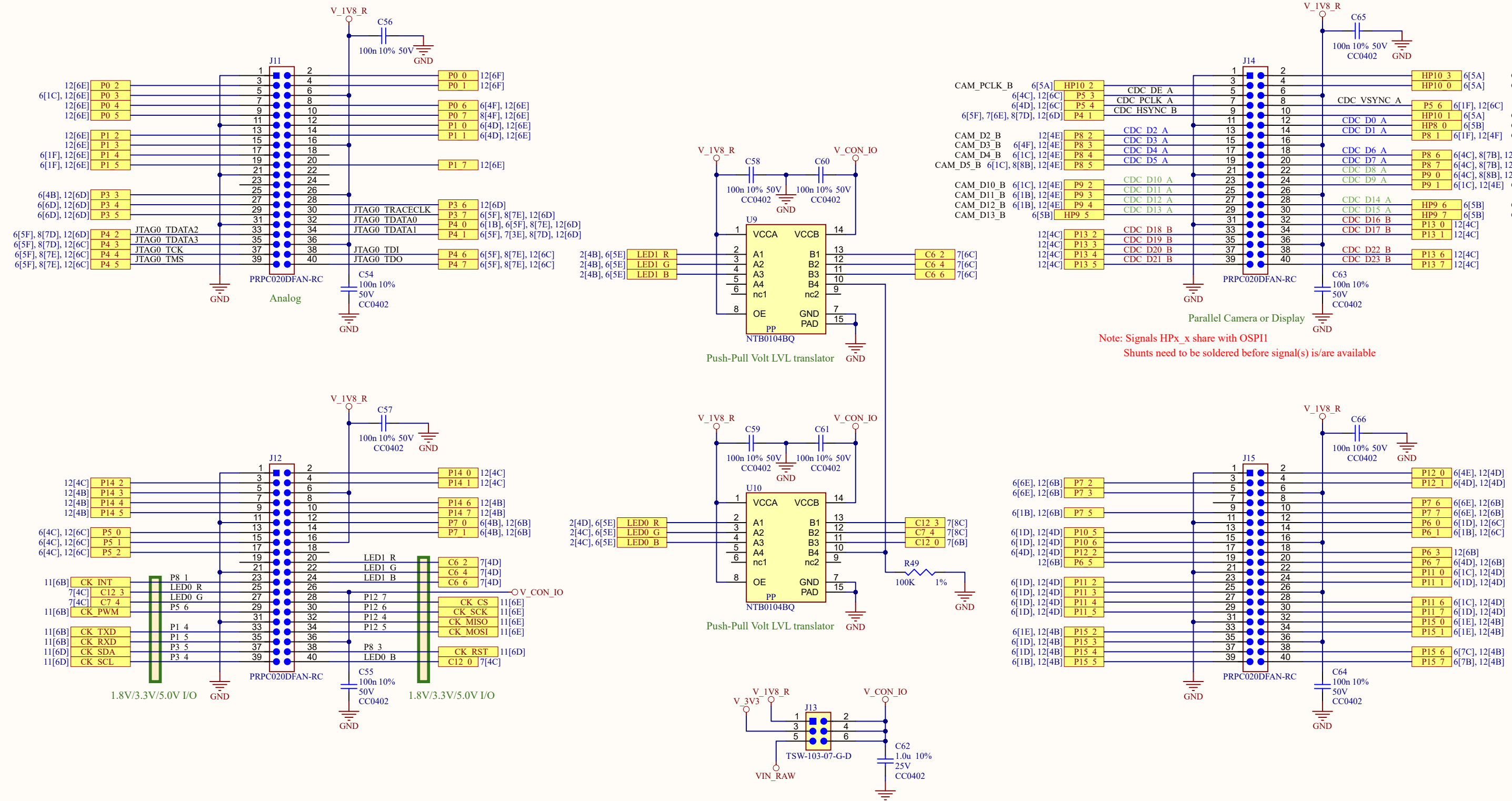
Note: OSPI1\_RXDS\_C is "not" bi-directional (A and B are ok) Therefore, OSPI1\_C cannot be used for HyperRAM



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CHK: n/a	--/--	TITLE	DESIGN ITEM: Not in version control
<b>ENSEMBLE DEV KIT BOARD</b>			
BOM: 251-00301	SIZE: B	CAGE CODE: none	DWG NO.: 221-00301
ASSY DWG: 121-00301	FAB DWG: 211-00301	SCALE: none	REV: 6 OF 12
PCB DWG: 110-00301-C	FILE NAME: 6-GPIOTranslate.SchDoc	SHEET: 6	OF 12

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Note: Signals HPx\_x share with OSP11  
Shunts need to be soldered before signal(s) is/are available

Connector I/O Voltage  
1-2 = 1.8V  
3-4 = 3.3V  
5-6 = 5.0V

SH13  
J11 1-2 Jumper

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DSN: K Braun	---	TITLE: ENSEMBLE DEV KIT BOARD		
CHK: n/a	---	REFERENCE DOCUMENTS	BOM: 251-00301	
ASSY DWG: 121-00301		SIZE: B	CAGE CODE: none	DWG NO.: 221-00301
FAB DWG: 211-00301		SCALE: none	FILE NAME: 7-IO Headers.SchDoc	REV: 7 OF 12
PCB DWG: 110-00301-C		SHEET 7 OF 12		

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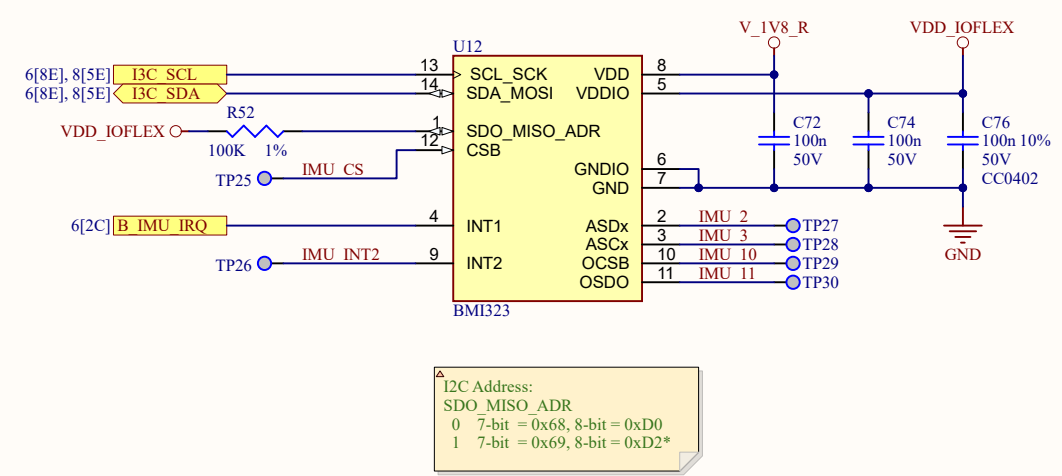
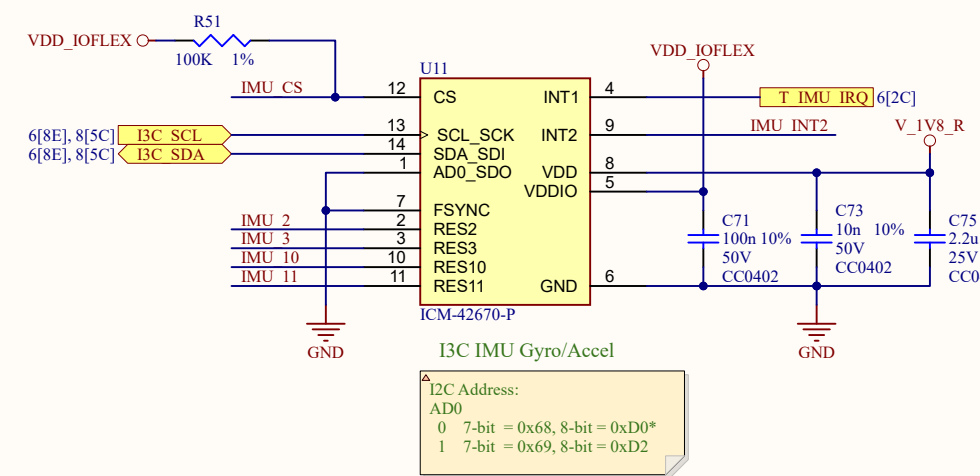
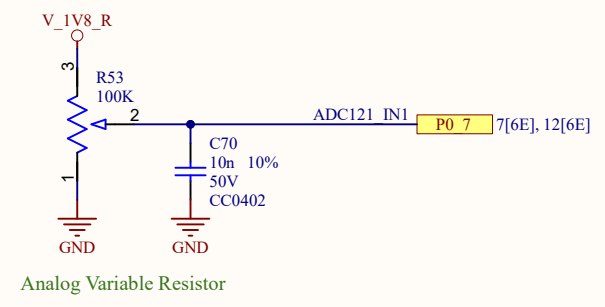
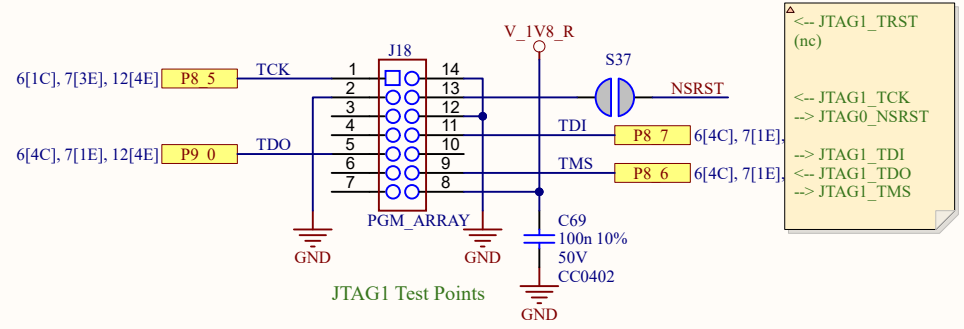
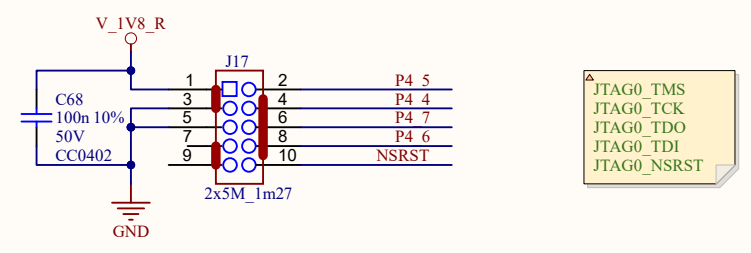
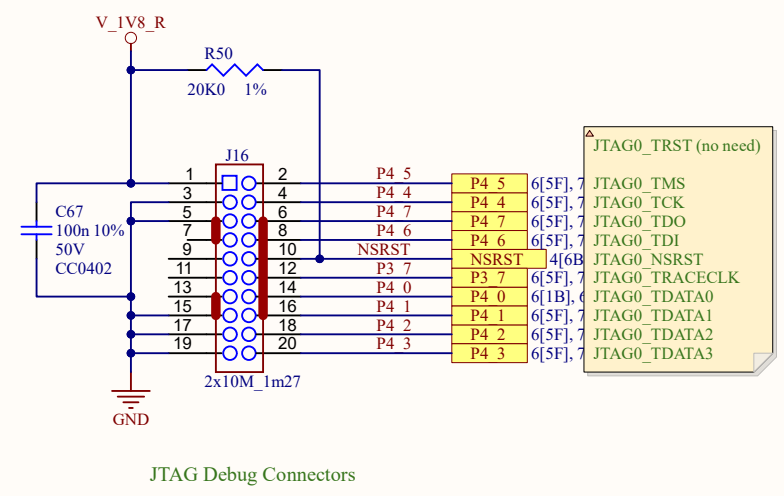
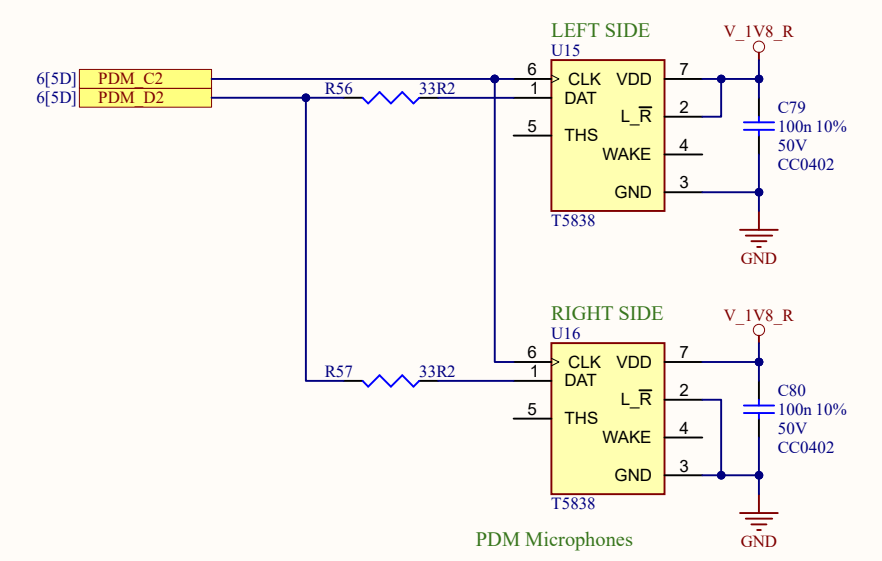
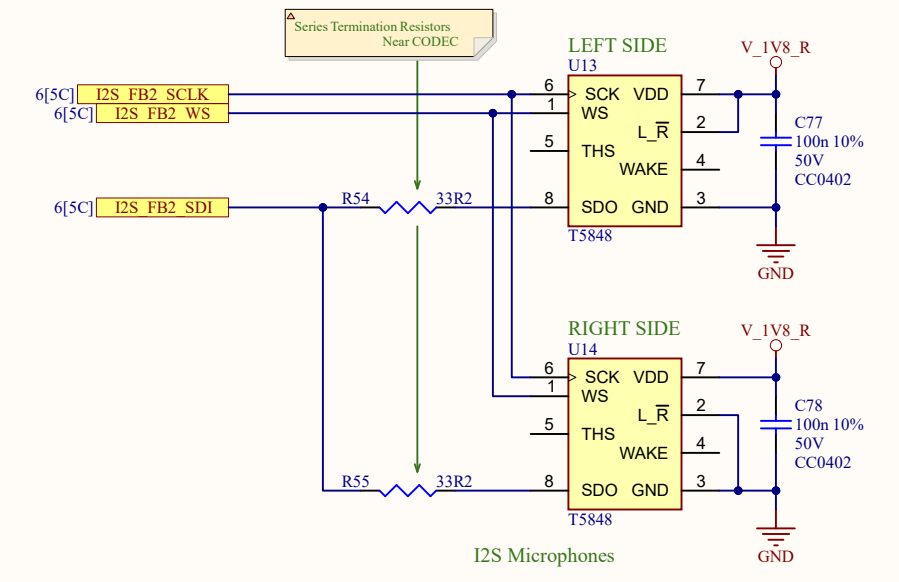


Table 29: Mapping of the secondary interface pins

Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I2C
2	ASDx	Digital I/O	Secondary Magnetometer interface	MOSI	SISO	SDA
3	ASCx	Digital I/O	Secondary Magnetometer interface	SCK	SCK	SCL
10	OCSB	Digital in	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital out	Secondary OIS interface	MISO	DNC	DNC

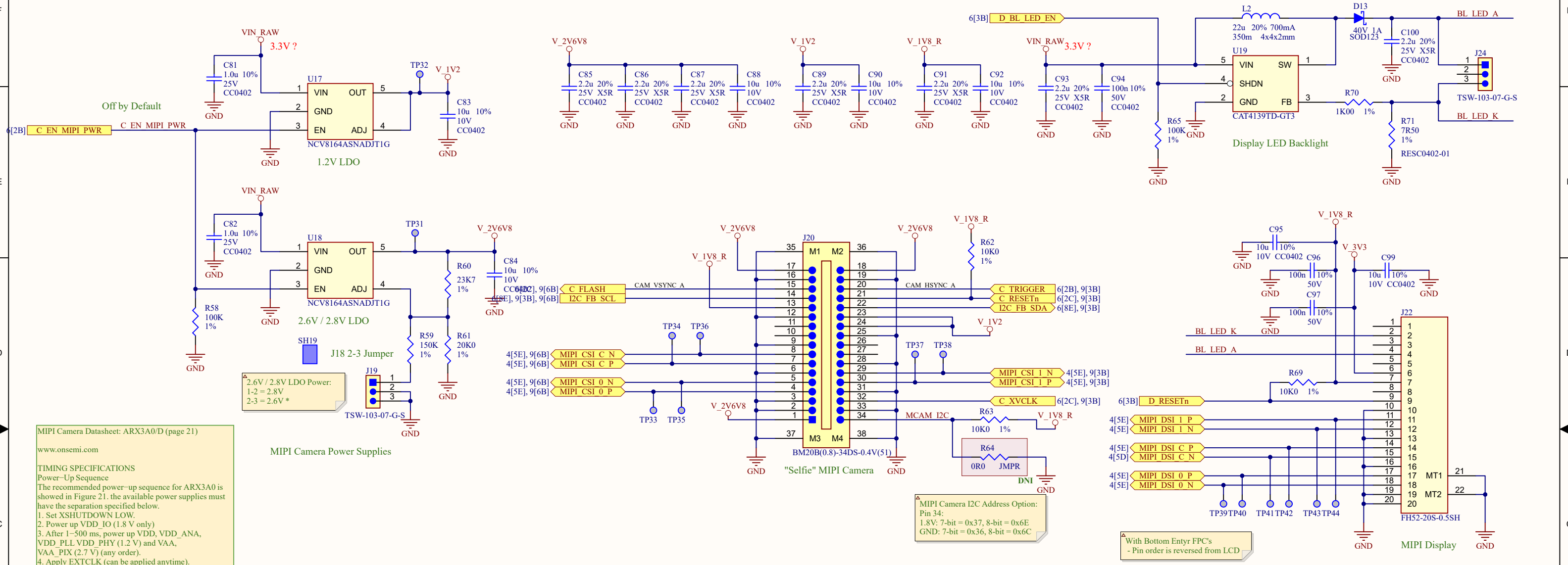


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DSN: K Braun	--/--	PROJECT REVISION: Not in version control	DOCUMENT REVISION: Not in version control	DESIGN ITEM: Not in version control	
CHK: n/a	--/--	TITLE			
<b>ENSEMBLE DEV KIT BOARD</b>					
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.	REV
BOM: 251-00301		B	none	221-00301	
ASSY DWG: 121-00301					
FAB DWG: 211-00301					
PCB DWG: 110-00301-C		SCALE: none	FILE NAME: 8-SensorsAndJTAG.SchDoc	SHEET 8	OF 12



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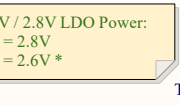
REVISION	DESCRIPTION	DATE	APPROVED



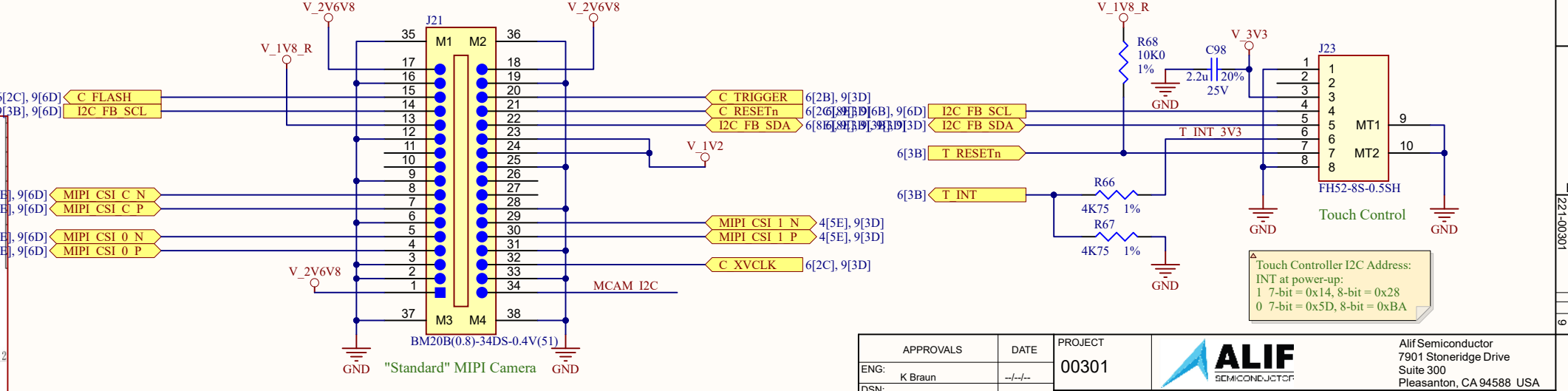
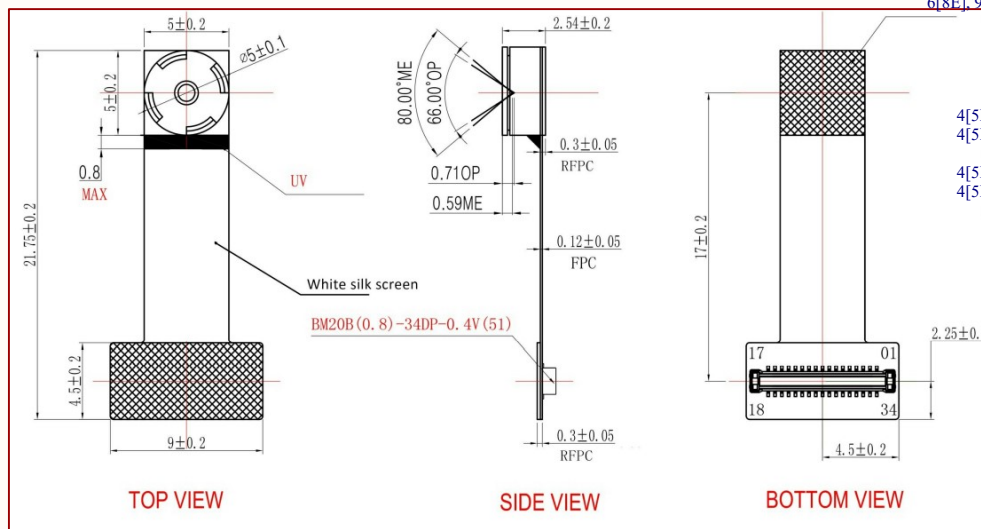
MIPI Camera Datasheet: ARX3A0/D (page 21)  
www.onsemi.com

**TIMING SPECIFICATIONS**  
Power-Up Sequence  
The recommended power-up sequence for ARX3A0 is shown in Figure 21. the available power supplies must have the separation specified below.

1. Set XSHUTDOWN LOW.
2. Power up VDD\_IO (1.8 V) only
3. After 1-500 ms, power up VDD, VDD\_ANA, VDD\_PLL, VDD\_PHY (1.2 V) and VAA, VAA\_PIX (2.7 V) (any order).
4. Apply EXTCLK (can be applied anytime).
5. After 1-500 ms, set XSHUTDOWN.
6. HOST configuration through I2C (PLL, output, etc).
7. Set stream = 1 (R0x301A[2]).
8. PLL internally enables and locks.
9. ARX3A0 enters streaming mode.



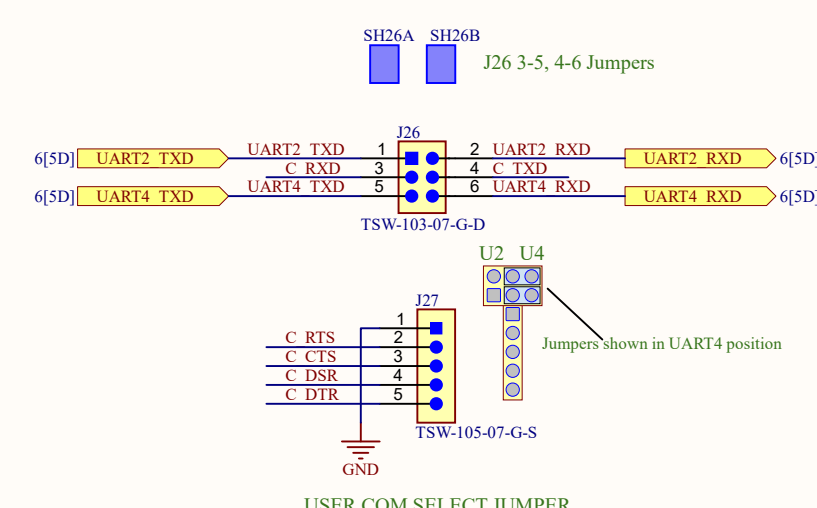
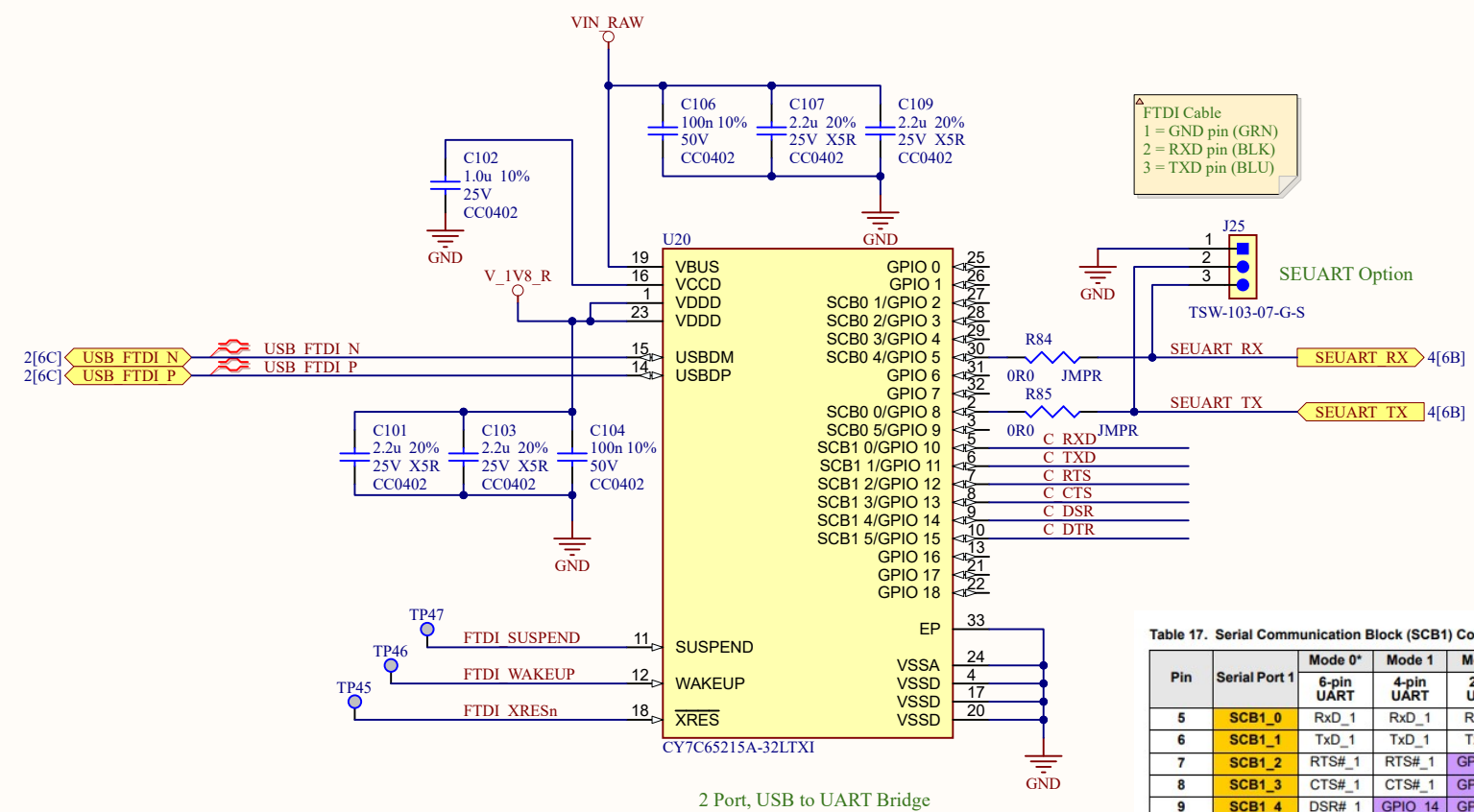
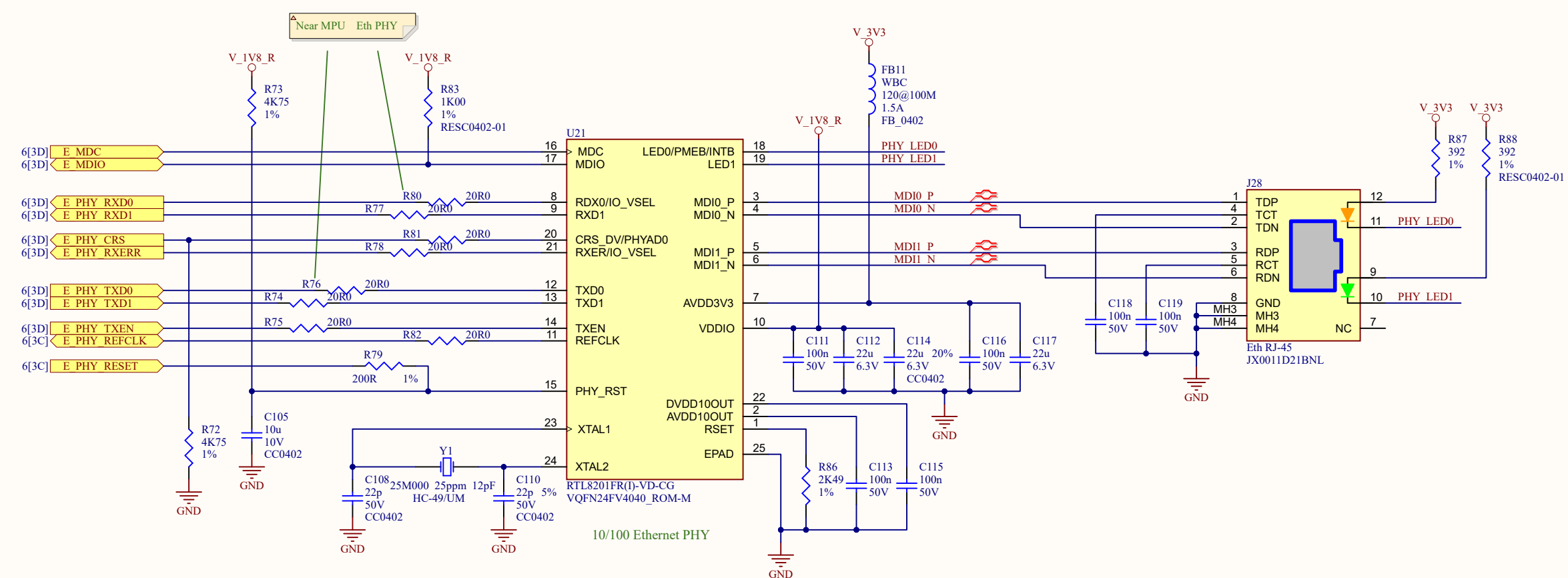
MIPI Camera Power Supplies



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BOM: 251-00301	ENSEMBLE DEV KIT BOARD			
ASSY DWG: 121-00301	SIZE: B	CAGE CODE: none	DWG NO.: 221-00301	REV
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**Table 17. Serial Communication Block (SCB1) Configuration**

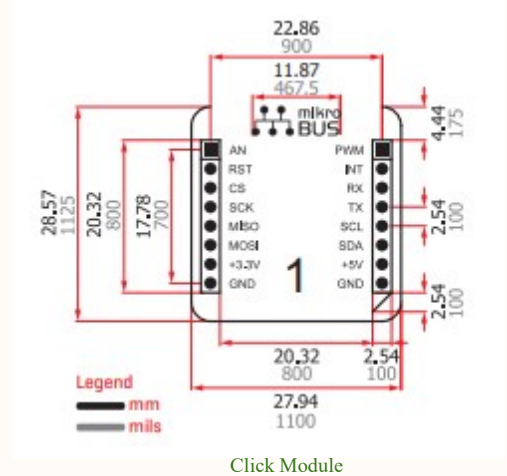
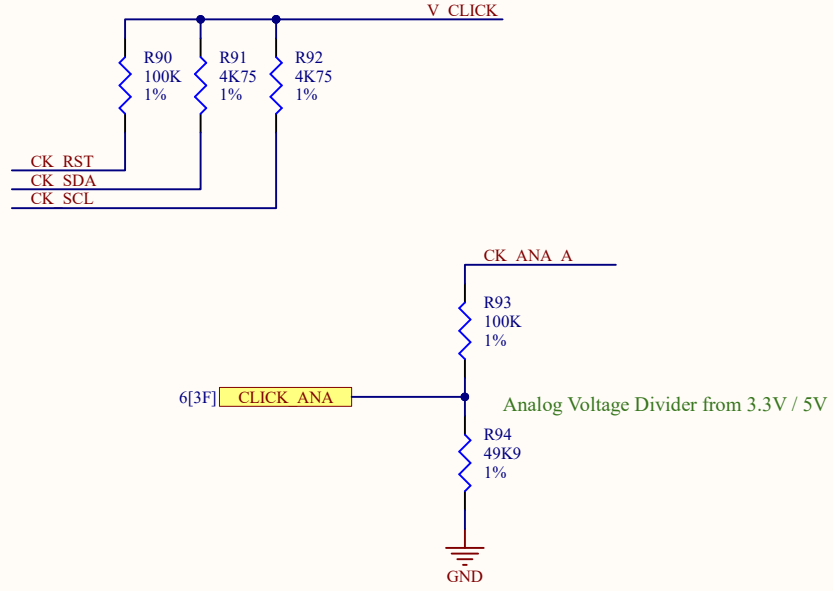
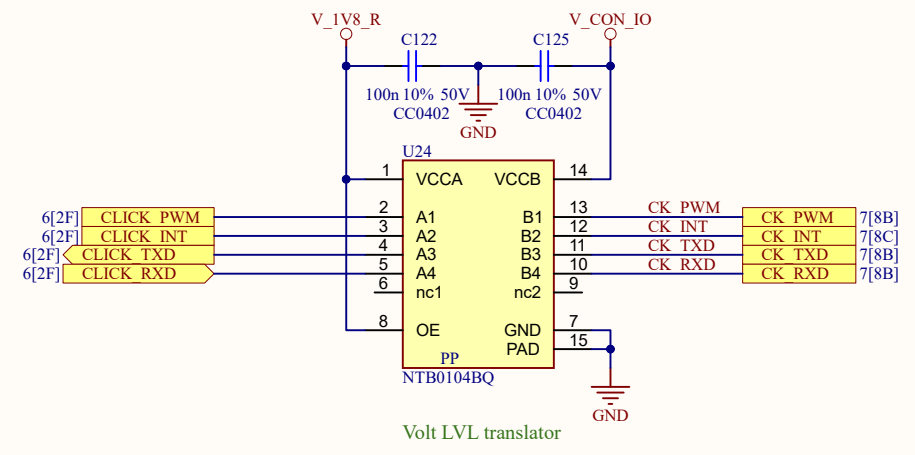
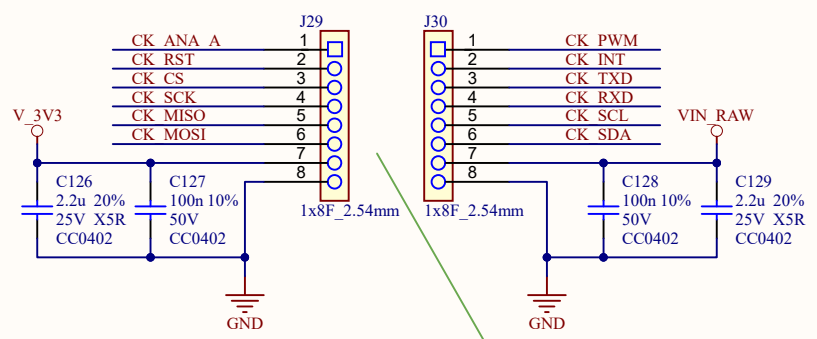
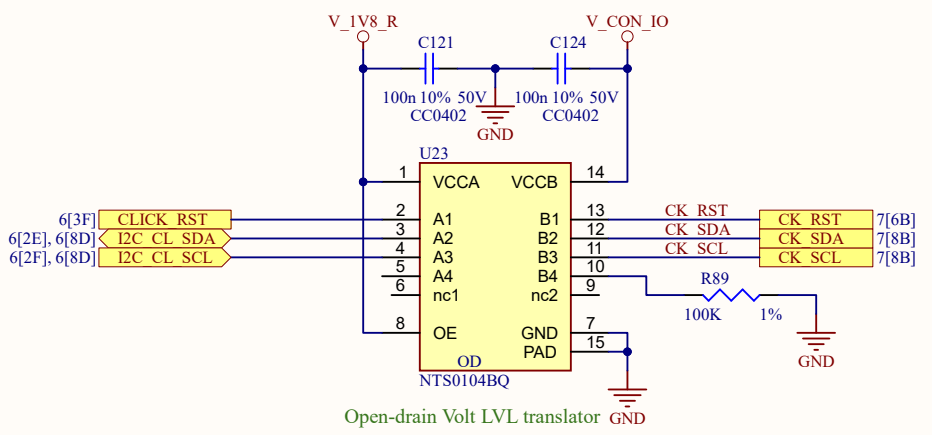
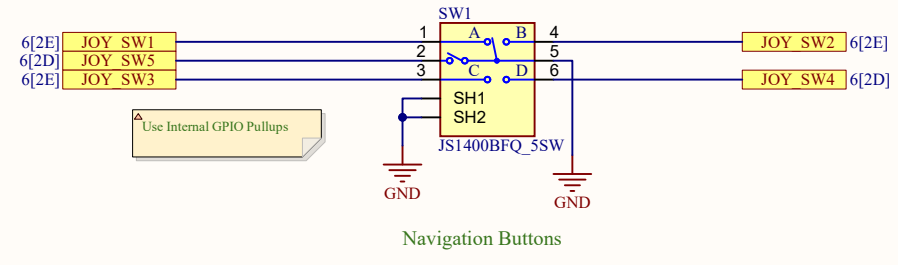
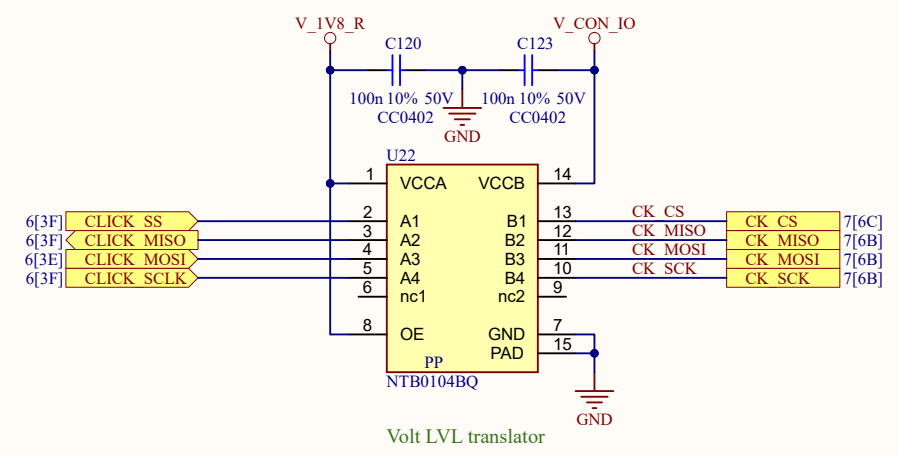
Pin	Serial Port 1	Mode 0*	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
5	SCB1_0	RxD_1	RxD_1	RxD_1	MISO_IN_1	MISO_OUT_1	SCL_OUT_1	SCL_IN_1	TDO
6	SCB1_1	TxD_1	TxD_1	TxD_1	MOSI_OUT_1	MOSI_IN_1	SDA_1	SDA_1	TDI
7	SCB1_2	RTS#_1	RTS#_1	GPIO_12	SSEL_OUT_1	SSEL_IN_1	GPIO_12	GPIO_12	TMS
8	SCB1_3	CTS#_1	CTS#_1	GPIO_13	SCLK_OUT_1	SCLK_IN_1	GPIO_13	GPIO_13	TCK
9	SCB1_4	DSR#_1	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	TRST#
10	SCB1_5	DTR#_1	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15

\*Note: Device configured in Mode 0 as default. Other modes can be configured via Cypress-supplied configuration utility.

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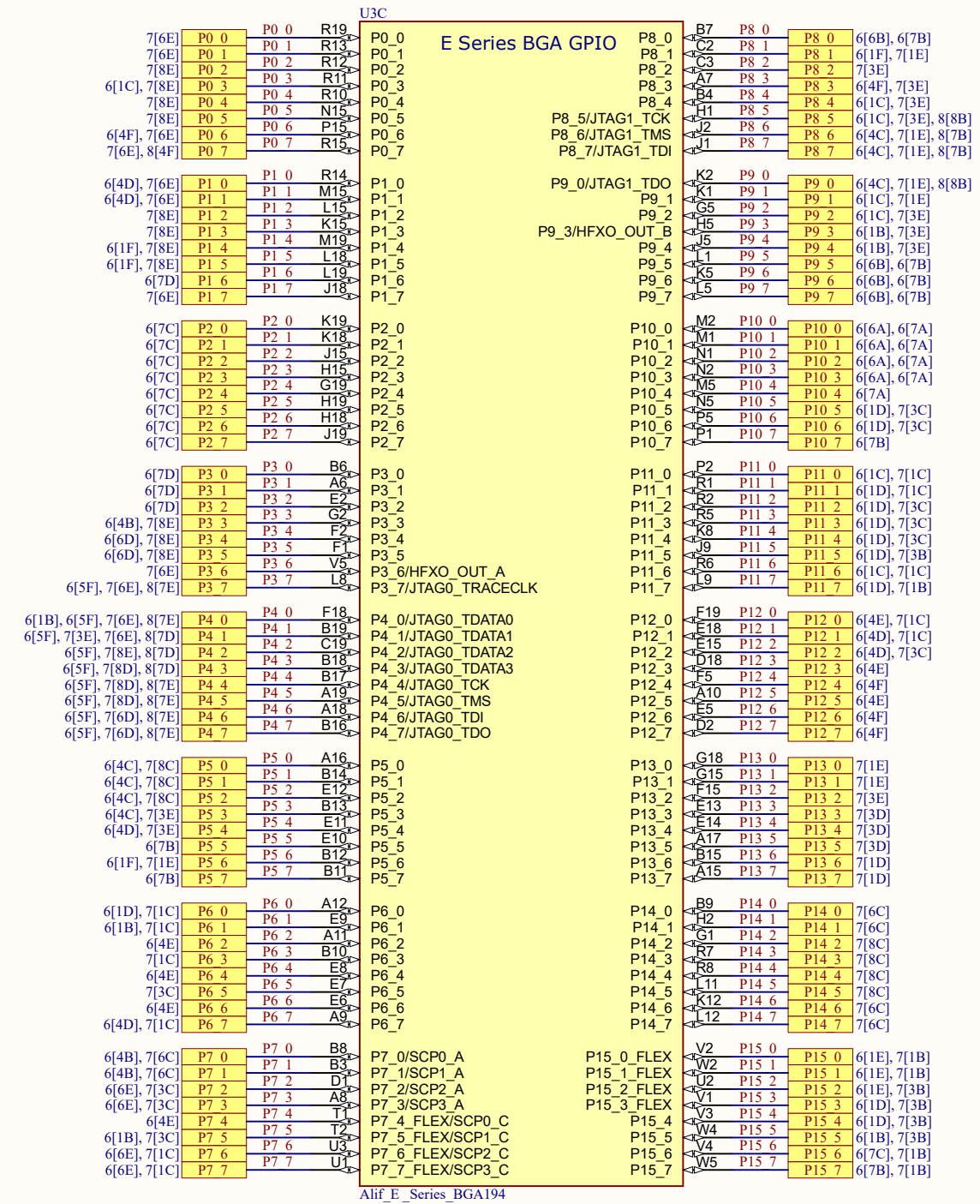
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BOM: 251-00301	ASSY DWG: 121-00301	FAB DWG: 211-00301	SCALE: none	FILE NAME: 11-Click.SchDoc
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REFERENCE DOCUMENTS		ENSEMBLE DEV KIT BOARD		
BOM: 251-00301	ASSY DWG: 121-00301	SIZE: B	CAGE CODE: none	DWG NO.: 221-00301
FAB DWG: 211-00301	PCB DWG: 110-00301-C	SCALE: none	FILE NAME: 12-CPU_GPIO.SchDoc	REV: 12
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