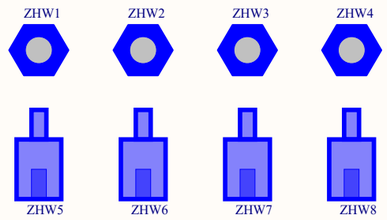
REVISION	DESCRIPTION	DATE	APPROVED

Revision History:

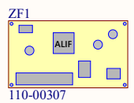
REV	DATE	Description:
A	24-MAR-2023	Initial Release, Taken from Flatboard Design
	14-APR-2023	Added OSPI HyperRAM Removed Coin Cell circuit
B	15-JUN-2023	Fixed swapped MIPI_CSI_C pair with MIPI_CSI_0 pair on BGA194 Add pullup to NSRST to U21 Removed UART4 option on U21 Realigned U21 GPIO assignments On P_9 and P_10 for Target JTAG connections.
	18-AUG-2023	Changed the MIPI DSI connectors to have top pins (was bottom) Changed nylon hardware standoff length
	07-SEP-2023	Changed C35 (VREG_AON) to 1.0uF
	12-SEP-2023	Changed OSPI Flash and HyperRAM to 64MB devices. Swapped USB_DEV_ID resistor divider for 1.8V signaling
C	20-SEP-2023	Fixed UART0 and UART2 swapped signals Changed USB power input pin
	03-OCT-2023	Added Cypress FTDI Controller, jumpers out for JLink-OB E1 (U21) with 0 ohm resistors
D	09-JAN-2024	Addrd TPs for RF SPI. PCB changes for Microphones Added DNI caps to MIPI CSI pairs
	25-JAN-2024	Design Review: Remove MIPI caps, GND TEST_MODE, change TP49 & TP50 to header pins

Required 2.54mm Shunts:

J3	VDD_3V3 Current Measurement
J4	VDD_1V8 Current Measurement
J5-1-2	FLEXIO = 1.8V * default
J5-2-3	FLEXIO = 3.3V
J6-1-2	WIFI in run mode * default
J6-2-3	WIFI in programming mode
J11-1-2	Camera Analog V = 2.8V
J11-2-3	Camera Analog V = 2.6V * default
J21	VDD_3V3 USB Current Measurement
SW3-A	JLink-OB E1 (and Cypress FTDI) run
SW3_B	JLink-OB E1 (and Cypress FTDI) hold-in reset
J15-1-3 & 2-4	Target SEUART * default
J15-3-5 & 4-6	Target UART2
J15-5-7 & 6-8	Target UART2
J15-7-9 & 8-10	Target UART4



Nylon Mounting Hardware



Double-Sided foam tape, for mounting LCD to back of PCBA
1/16" Thick, 1/2" Wide, cut to 2" Length

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00307	
ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

PROJECT 00307

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TITLE

APP KIT BOARD

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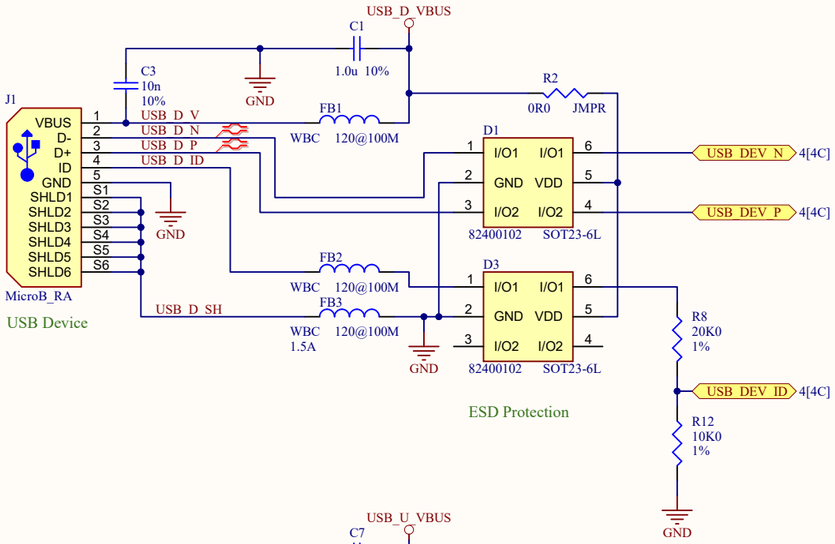

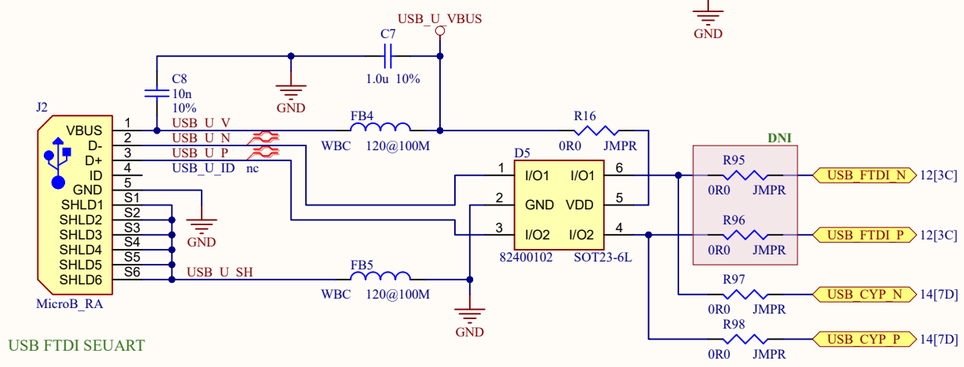

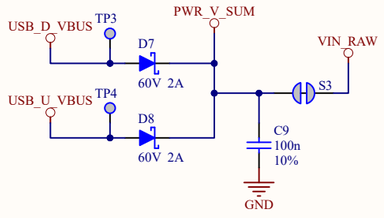

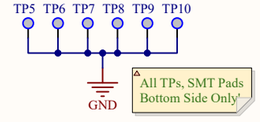

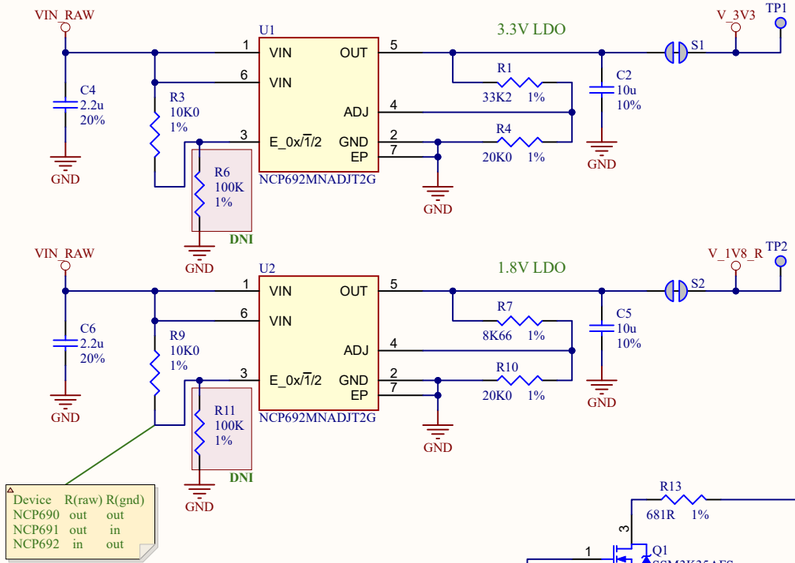

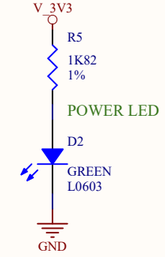

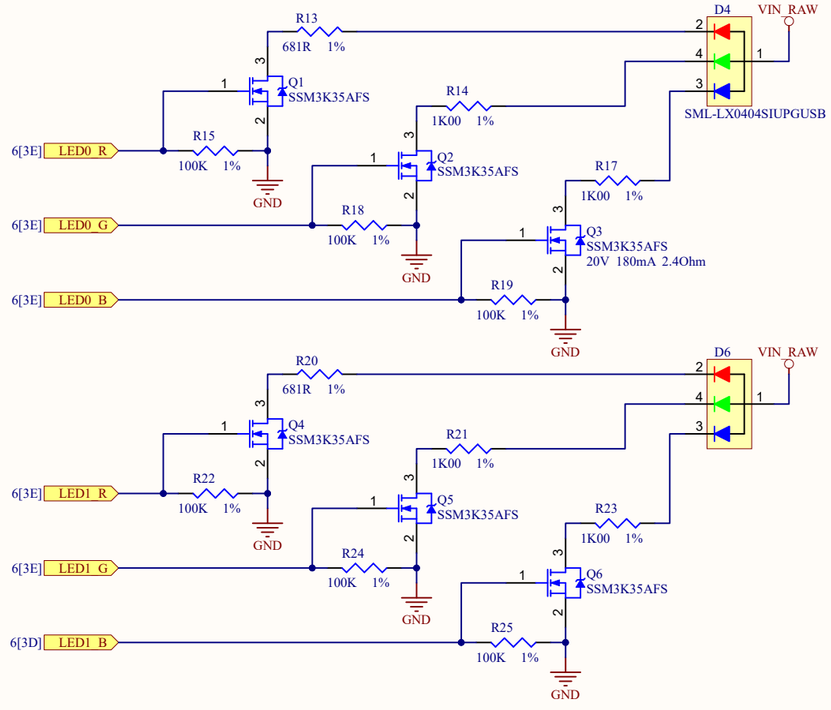

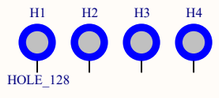

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ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

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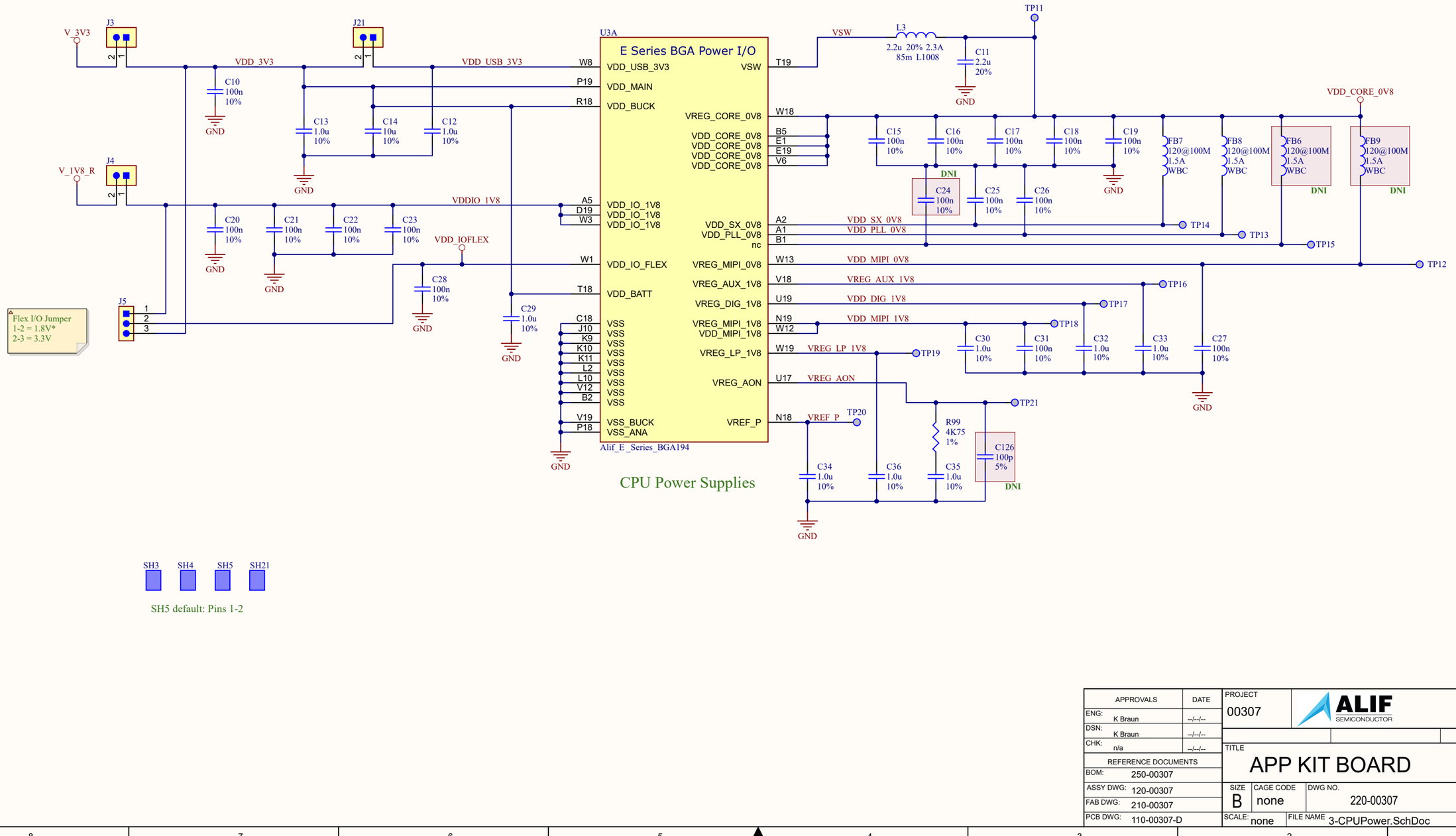

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ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

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DWG NO 220-00307 REV D SHT 3

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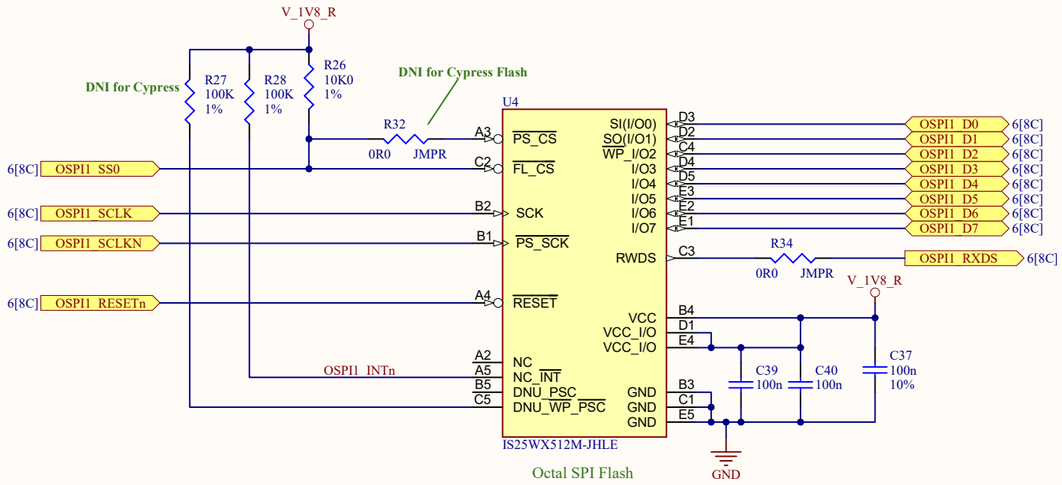
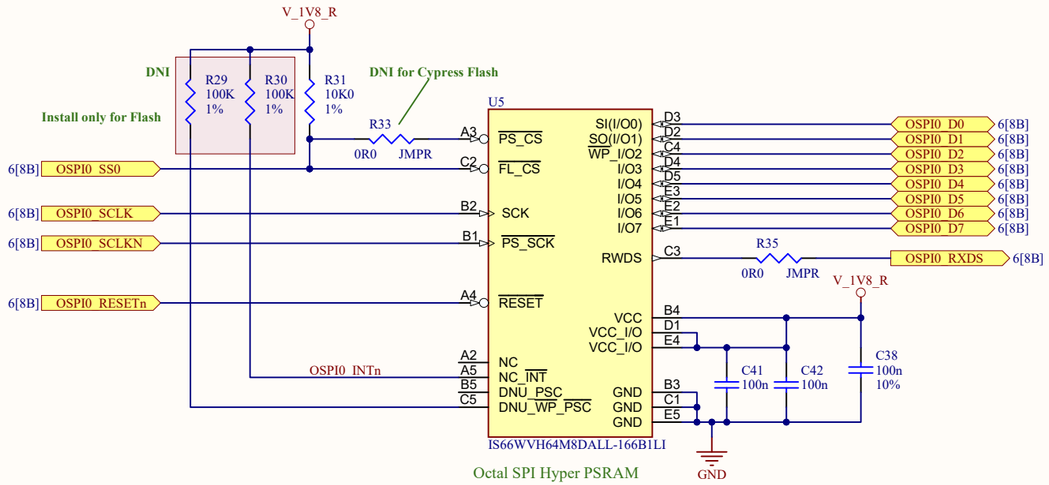
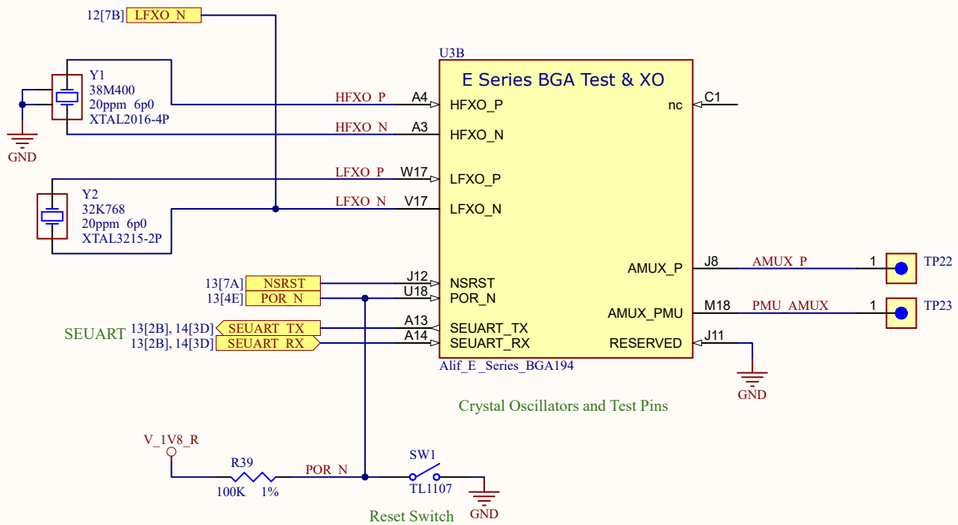
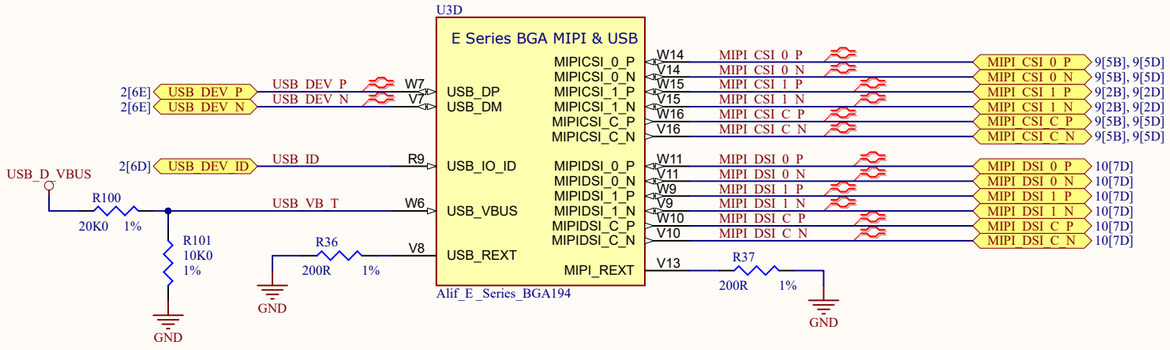




"Universal" Octal SPI Devices. Either chip can be Flash or RAM





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REFERENCE DOCUMENTS

BOM:	250-00307
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DWG NO. 220-00307 REV D SHT 4

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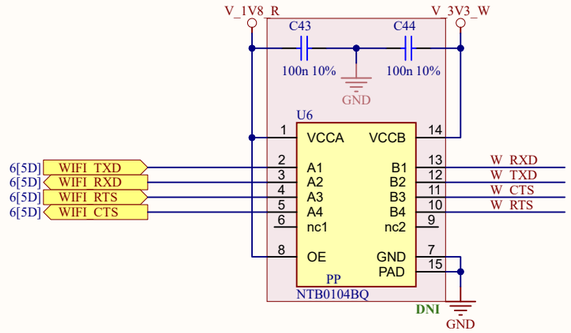
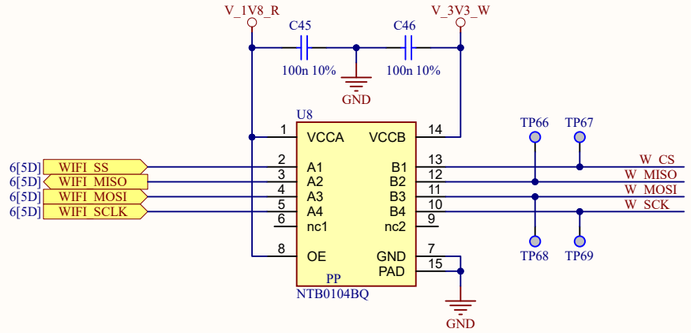
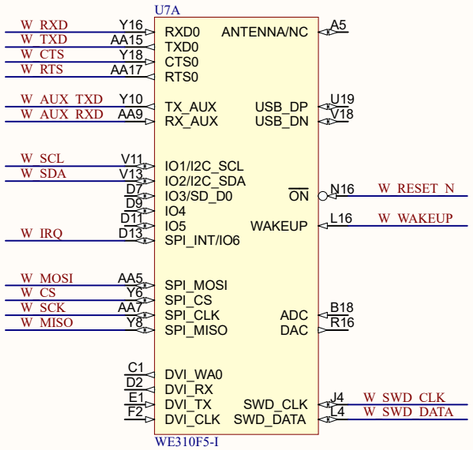
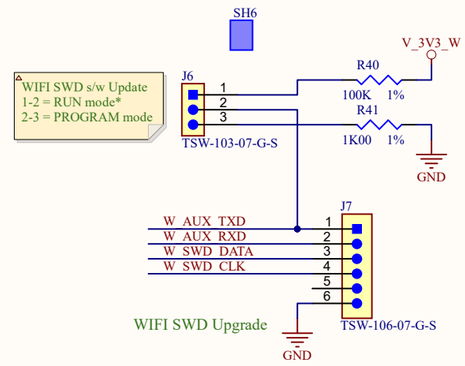




Volt LVL translator



WIFI / BLE Interface



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REFERENCE DOCUMENTS

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PCB DWG:	110-00307-D

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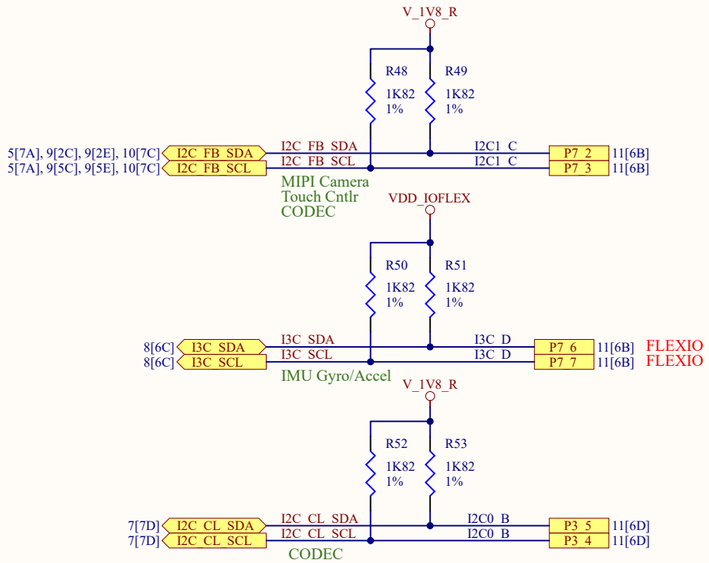

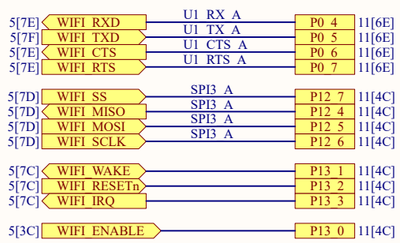

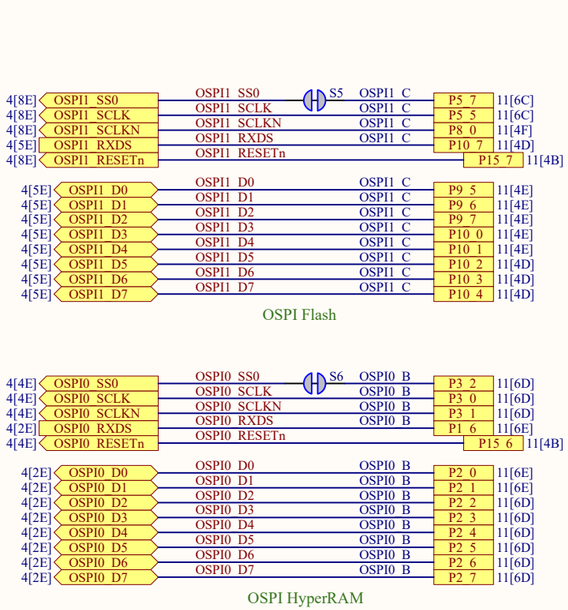

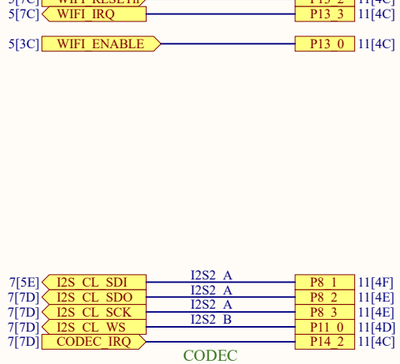

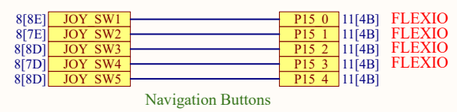

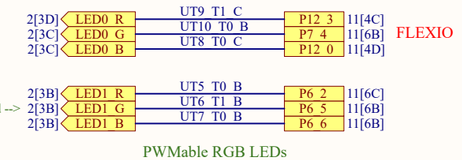

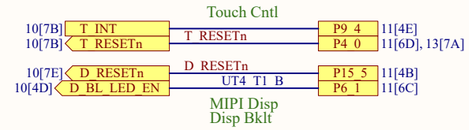

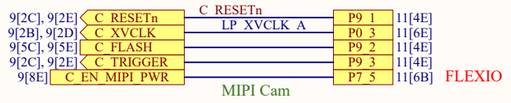

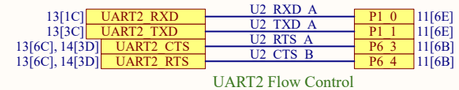

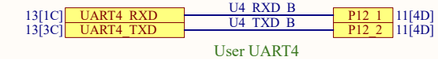

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DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00307	
ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

PROJECT 00307

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TITLE: APP KIT BOARD

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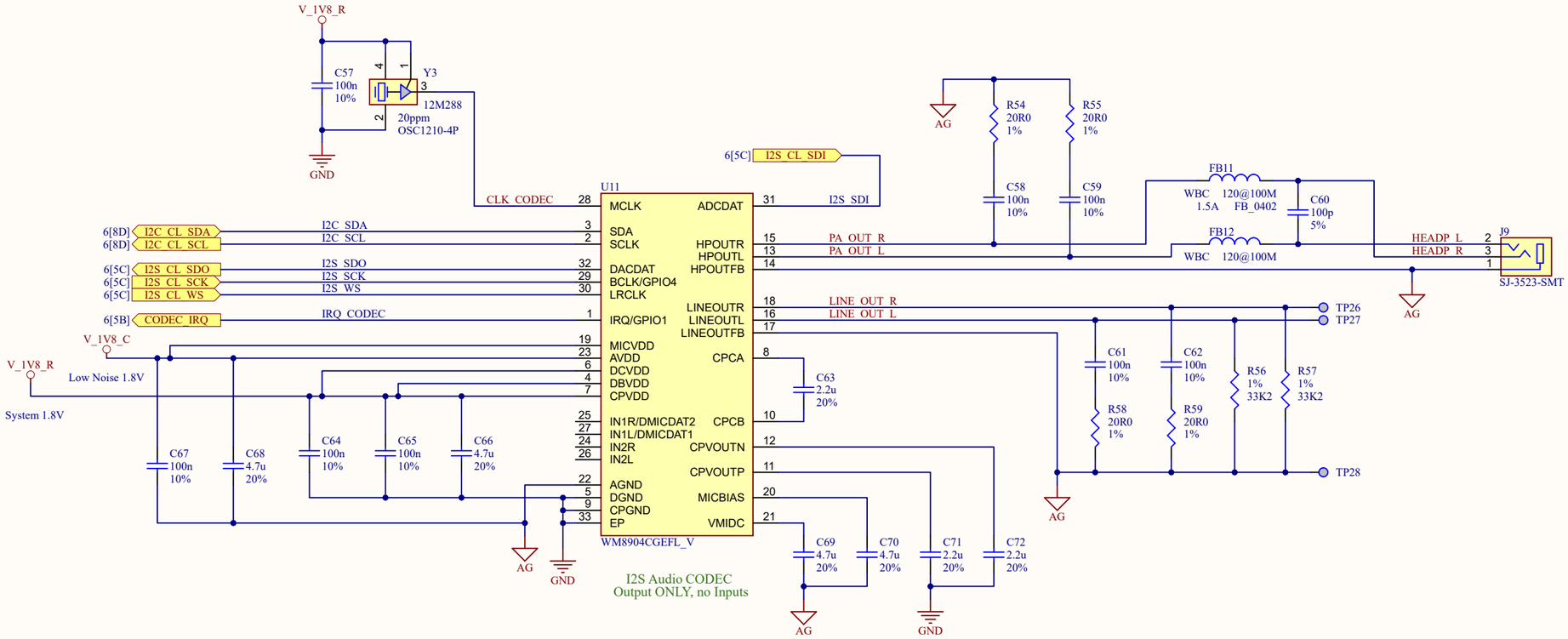
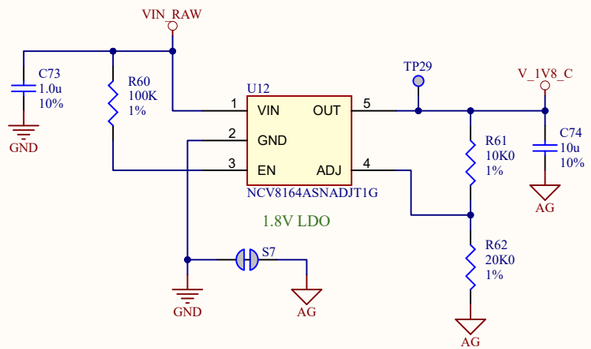
REVISION	DESCRIPTION	DATE	APPROVED





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REFERENCE DOCUMENTS

BOM: 250-00307
ASSY DWG: 120-00307
FAB DWG: 210-00307
PCB DWG: 110-00307-D

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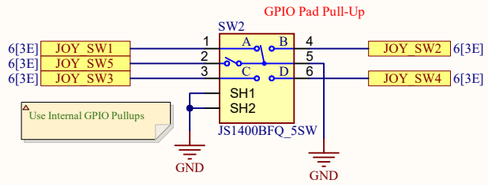
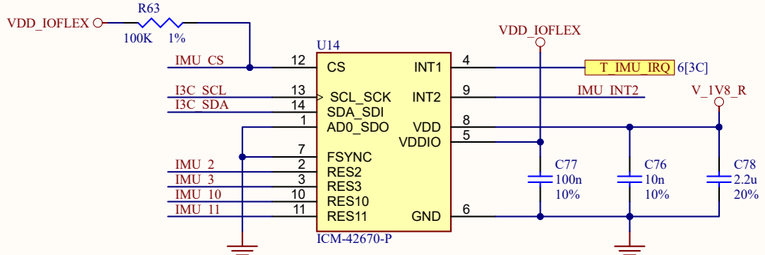
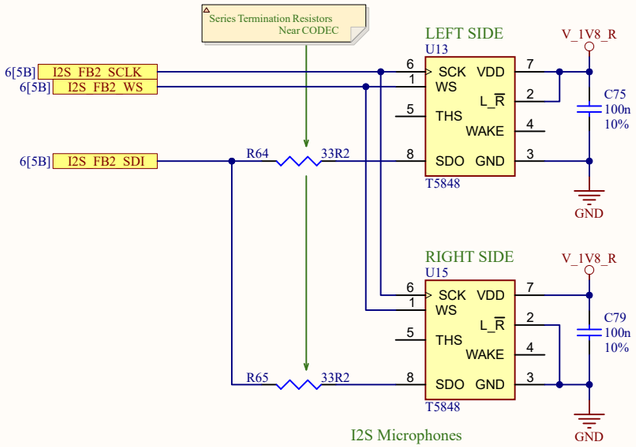


Navigation Buttons

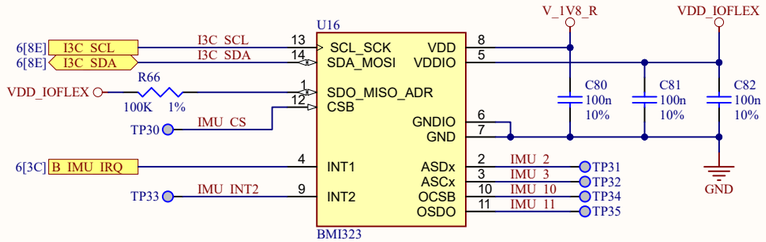


I3C IMU Gyro/Accel

I2C Address:
AD0
0 7-bit = 0x68, 8-bit = 0xD0*
1 7-bit = 0x69, 8-bit = 0xD2



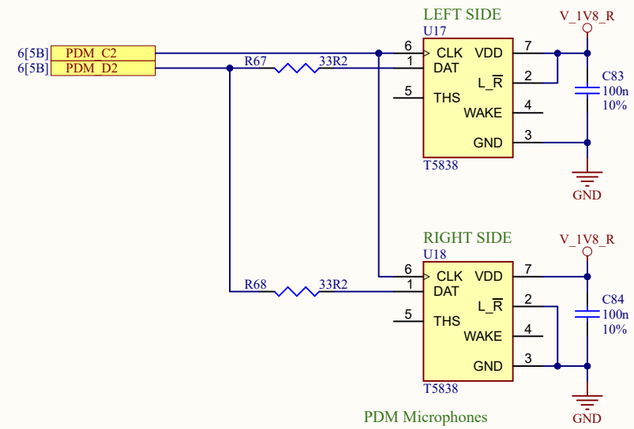
I2S Microphones



I2C Address:
SDO_MISO_ADR
0 7-bit = 0x68, 8-bit = 0xD0
1 7-bit = 0x69, 8-bit = 0xD2*

Table 29: Mapping of the secondary interface pins

Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I2C
2	ASDx	Digital I/O	Secondary Magnetometer interface	MOSI	SISO	SDA
3	ASCx	Digital I/O	Secondary Magnetometer interface	SCK	SCK	SCL
10	OCSB	Digital in	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital out	Secondary OIS interface	MISO	DNC	DNC



PDM Microphones

APPROVALS	DATE
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DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00307	
ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

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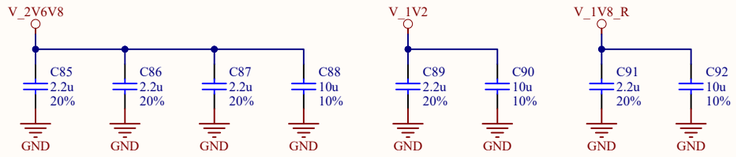
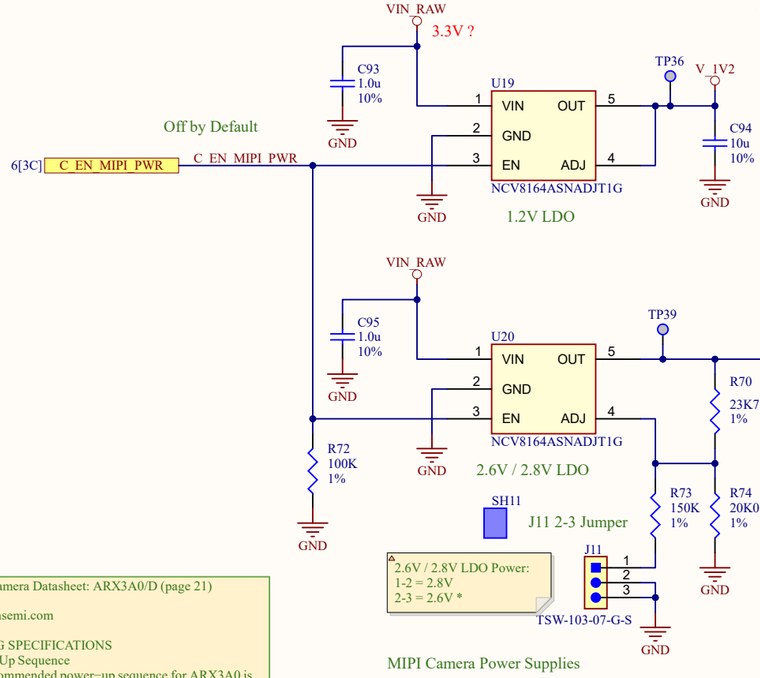
DWG NO 220-00307 REV D 8

REVISION	DESCRIPTION	DATE	APPROVED





MIPI Camera Datasheet: ARX3A0/D (page 21)

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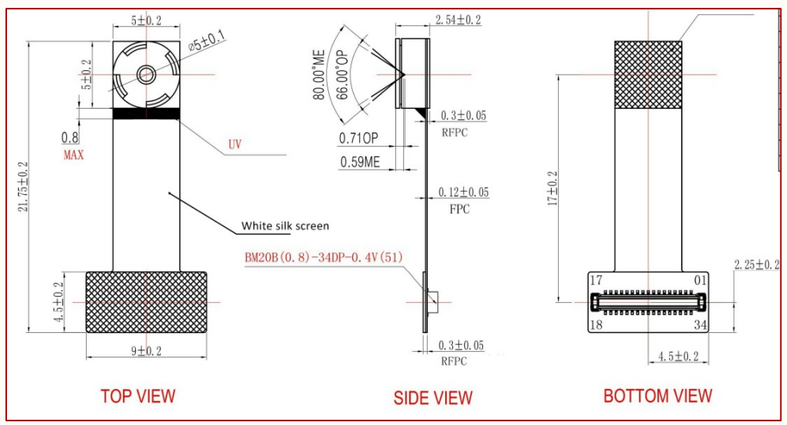
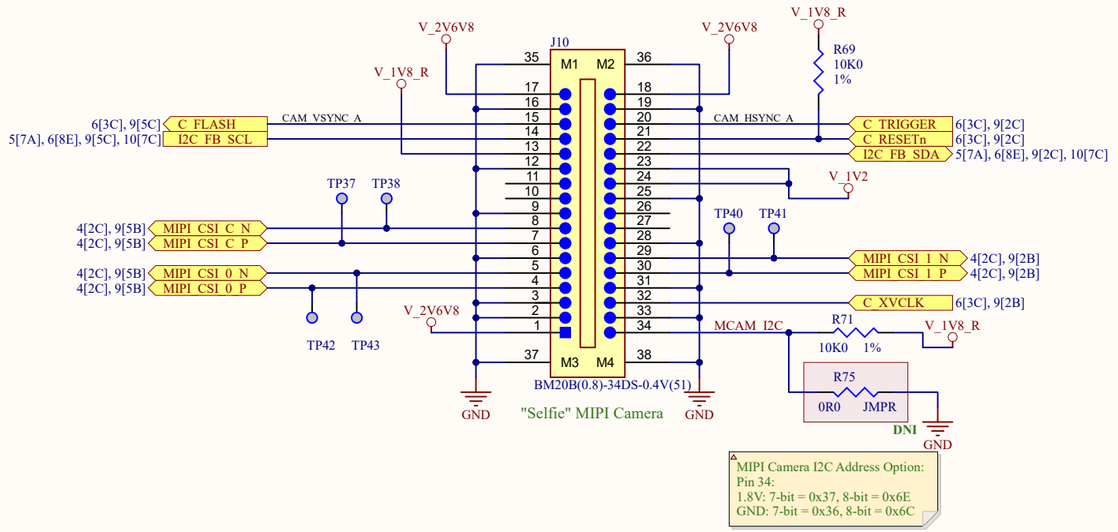
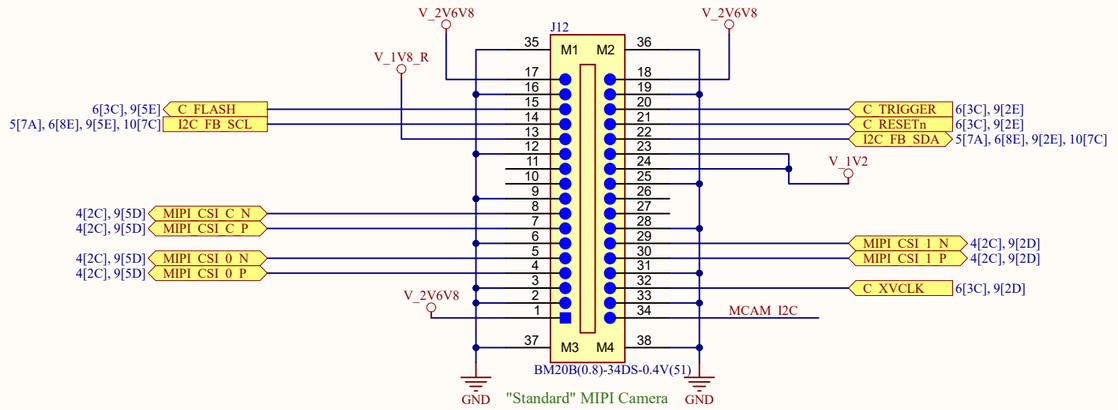
TIMING SPECIFICATIONS
Power−Up Sequence
The recommended power−up sequence for ARX3A0 is showed in Figure 21. the available power supplies must have the separation specified below.
1. Set XSHUTDOWN LOW.
2. Power up VDD_IO (1.8 V only)
3. After 1−500 ms, power up VDD, VDD_ANA, VDD_PLL VDD_PHY (1.2 V) and VAA, VAA_PIX (2.7 V) (any order).
4. Apply EXTCLK (can be applied anytime).
5. After 1−500 ms, set XSHUTDOWN.
6. HOST configuration through I2C (PLL, output, etc).
7. Set stream = 1 (R0x301A[2]).
8. PLL internally enables and locks.
9. ARX3A0 enters streaming mode.







APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00307	
ASSY DWG: 120-00307	
FAB DWG: 210-00307	
PCB DWG: 110-00307-D	

PROJECT 00307

ALIF SEMICONDUCTOR

Alif Semiconductor
7901 Stoneridge Drive
Suite 300
Pleasanton, CA 94588 USA

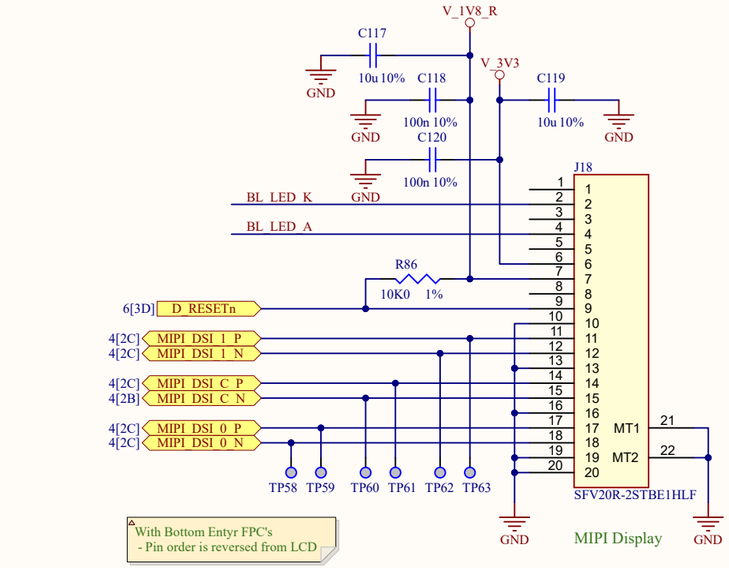
TITLE: APP KIT BOARD

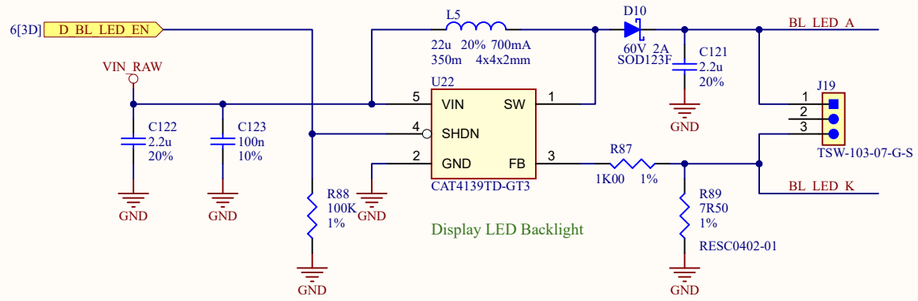
SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

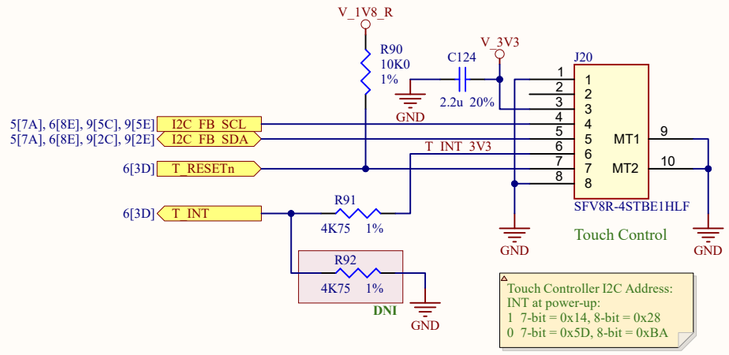
SCALE: none | FILE NAME 9-MIPI_CSI.SchDoc | SHEET 9 OF 14

DWG NO. 220-00307 REV D SHT 9

REVISION	DESCRIPTION	DATE	APPROVED







APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00307
ASSY DWG:	120-00307
FAB DWG:	210-00307
PCB DWG:	110-00307-D

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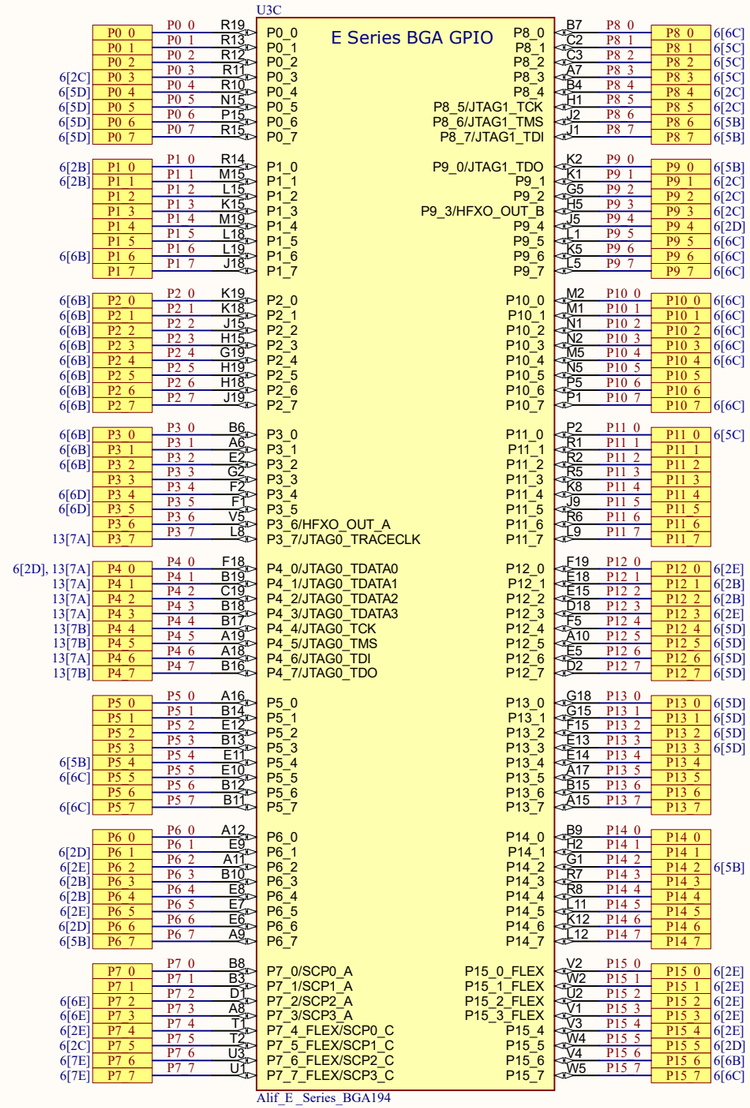
SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

SCALE: none FILE NAME 10-MIPI_DSI.SchDoc SHEET 10 OF 14

DWG NO. 220-00307 REVISION D 10

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00307
ASSY DWG:	120-00307
FAB DWG:	210-00307
PCB DWG:	110-00307-D

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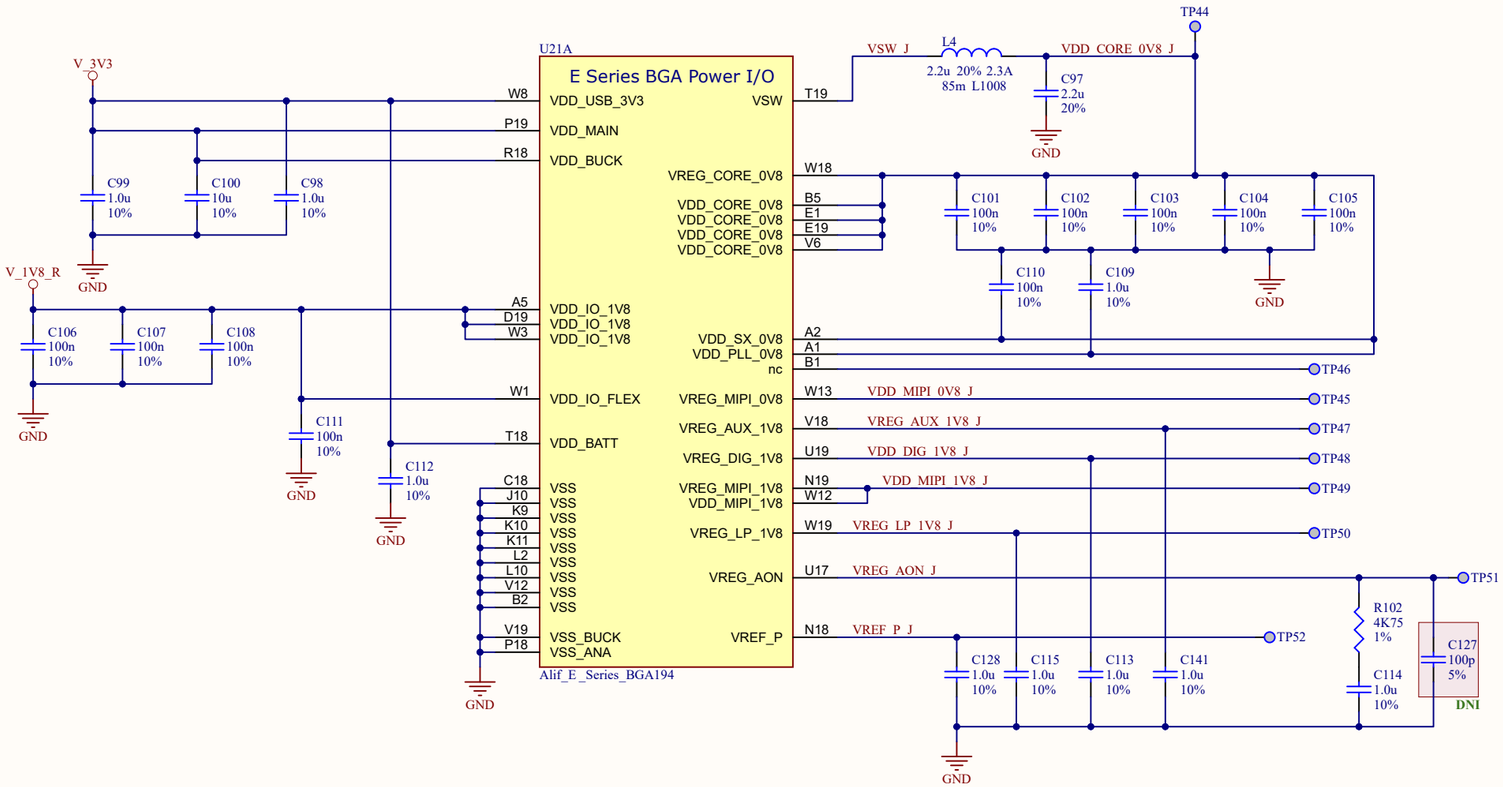
SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

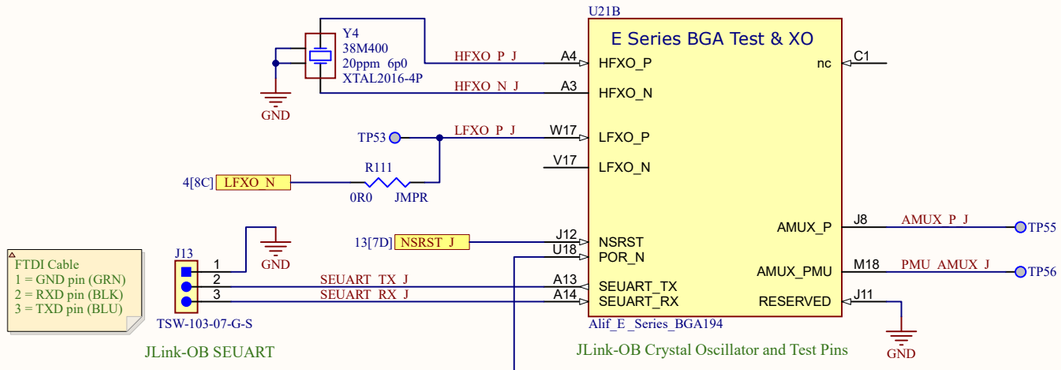
SCALE: none | FILE NAME 11-CPU_GPIO.SchDoc | SHEET 11 OF 14

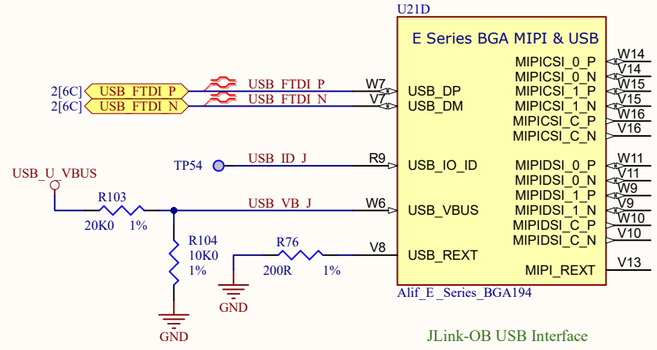
DWG NO 220-00307 REV D SHT 11

REVISION	DESCRIPTION	DATE	APPROVED

JLink-OB E1 CPU Power Supplies







APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS	
BOM:	250-00307
ASSY DWG:	120-00307
FAB DWG:	210-00307
PCB DWG:	110-00307-D

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TITLE: APP KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

SCALE: none | FILE NAME 12-JLINK_1.SchDoc | SHEET 12 OF 14

DWG NO 220-00307 | REV D | SHT 12

REVISION	DESCRIPTION	DATE	APPROVED

220-00307 DWG. NO. | D REV | 13 SHT

U21C

E Series BGA GPIO

Alif_E_Series_BGA194

UART1_RX_A Target TDO P4_7

UART2_A C_RXD C_TXD

UART2_A 6[3B], 14[3D] UART2_CTS JLink RTS 0R0 R109

UART2_B 6[3B], 14[3D] UART2_RTS JLink CTS 0R0 R110

UT10_0_B LED0_G_J

P4_6 Target TDI

P4_7 Target TDO

P4_4 Target TCK

NSRST Target NSRST

POR_N 4[7B]

P4_5 Target TMS

LED0_B_J UT8_0_C

LED0_R_J UT9_1_C

TCK_J TMS_J TDI_J TDO_J

JOY_SW1_J SW4

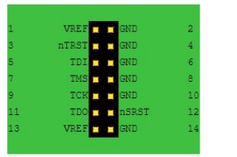
JOY_SW2_J SW5

TL1107

GPIO Pad Pull-Up

JLink-OB User Switches

ARM14 JTAG header pinout



V_1V8_R

J14

R94 100K 1%

NSRST_J 12[6B]

TDI_J TMS_J TCK_J TDO_J

PGM_ARRAY

GND

"Plug Of Nails" connector
JLink-OB JTAG0 Test Points

<-- JTAG1_TRST (nc)

<-- JTAG1_TCK
--> JTAG0_NSRST

--> JTAG1_TDI
<-- JTAG1_TDO
--> JTAG1_TMS

V_1V8_R

R85 100K 1%

J17

C116 10% 100n

P4_5 11[6C]
P4_4 11[6C]
P4_7 11[6C]
P4_6 11[6C]
NSRST NSRST 4[7B]
P3_7 11[6D]
P4_0 6[2D], 11[6D]
P4_1 11[6D]
P4_2 11[6D]
P4_3 11[6C]

2x10M_1m27

GND

"Target E3" JTAG0 Debug Connector

JTAG0 Signals in Parallel with
JLink-OB E1 Programmer

JTAG0_TRST (no need)

JTAG0_TMS
JTAG0_TCK
JTAG0_TDO
JTAG0_TDI
JTAG0_NSRST
JTAG0_TRACECLK
JTAG0_TDATA0
JTAG0_TDATA1
JTAG0_TDATA2
JTAG0_TDATA3

D9 VIN_RAW

R79 681R 1%

Q9 SSM3K35AFS

R80 1K00 1%

LED0_R_J

R81 100K 1%

Q10 SSM3K35AFS

R82 1K00 1%

LED0_G_J

R83 100K 1%

Q11 SSM3K35AFS

LED0_B_J

R84 100K 1%

GND

JLink-OB E1 LED Drivers

Target UART Connections to JLink-OB

SH15A SH15B

J15

SEU_TXD C_RXD UART2_TXD UART4_TXD

SEU_RXD C_TXD UART2_RXD UART4_RXD

14[4C] C_RXD
6[3B] UART2_TXD
6[3B] UART4_TXD

C_TXD 14[4D]
UART2_RXD 6[3B]
UART4_RXD 6[3B]

TSW-105-07-G-D

Target UART Selection
1-3 & 2-4 = SEUART
3-5 & 4-6 = UART2
5-7 & 6-8 = UART2
7-9 & 8-10 = UART4

SEUART Manual
Override Option

J16

TSW-103-(

FTDI Cable
1 = GND pin (GRN)
2 = RXD pin (BLK)
3 = TXD pin (BLU)

SEU_RXD S8 SEUART_RX SEUART_RX 4[7B], 14[3D]

SEU_TXD S9 SEUART_TX SEUART_TX 4[7B], 14[3D]

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM: 250-00307
ASSY DWG: 120-00307
FAB DWG: 210-00307
PCB DWG: 110-00307-D

PROJECT 00307

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TITLE

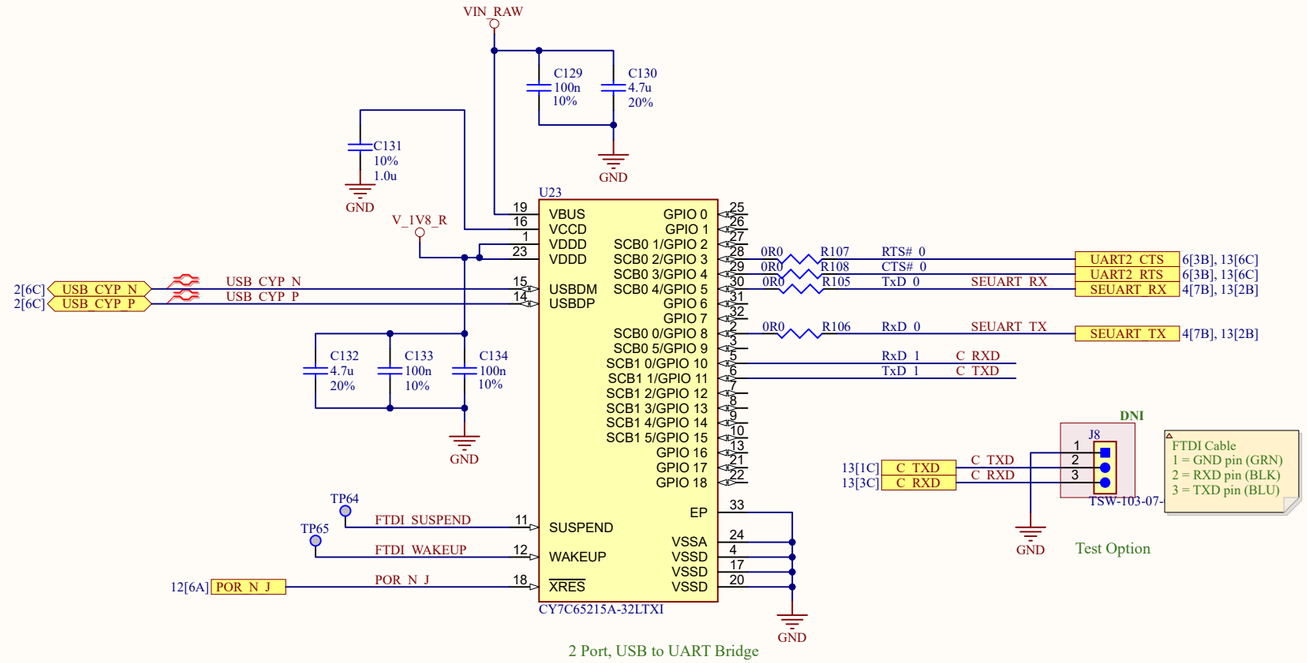
APP KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

SCALE: none FILE NAME 13-JLINK_2.SchDoc SHEET 13 OF 14

DWG NO. 220-00307 REV D SHT 13

REVISION	DESCRIPTION	DATE	APPROVED



2 Port, USB to UART Bridge

Table 17. Serial Communication Block (SCB1) Configuration

Pin	Serial Port 1	Mode 0* 6-pin UART	Mode 1 4-pin UART	Mode 2 2-pin UART	Mode 3 SPI Master	Mode 4 SPI Slave	Mode 5 I²C Master	Mode 6 I²C Slave	Mode 7 JTAG Master
5	SCB1_0	RxD_1	RxD_1	RxD_1	MISO_IN_1	MISO_OUT_1	SCL_OUT_1	SCL_IN_1	TDO
6	SCB1_1	TxD_1	TxD_1	TxD_1	MOSI_OUT_1	MOSI_IN_1	SDA_1	SDA_1	TDI
7	SCB1_2	RTS#_1	RTS#_1	GPIO_12	SSEL_OUT_1	SSEL_IN_1	GPIO_12	GPIO_12	TMS
8	SCB1_3	CTS#_1	CTS#_1	GPIO_13	SCLK_OUT_1	SCLK_IN_1	GPIO_13	GPIO_13	TCK
9	SCB1_4	DSR#_1	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	TRST#
10	SCB1_5	DTR#_1	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15

*Note: Device configured in Mode 0 as default. Other modes can be configured via Cypress-supplied configuration utility.

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM: 250-00307
ASSY DWG: 120-00307
FAB DWG: 210-00307
PCB DWG: 110-00307-D

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Pleasanton, CA 94588 USA

TITLE: APP KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00307	D

SCALE: none | FILE NAME 14-CypressSEUART.SchDoc | SHEET 14 OF 14

DWG NO. 220-00307 REV D 14