

REVISION	DESCRIPTION	DATE	APPROVED

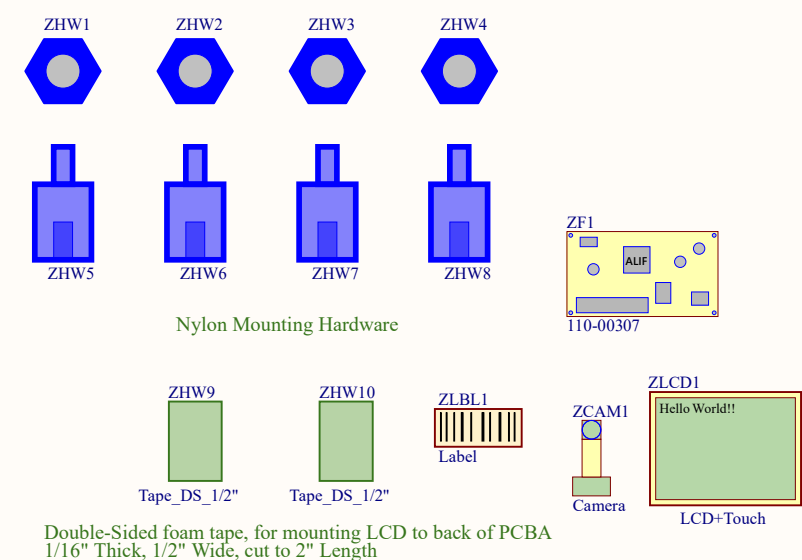
Note: Items in this schematic may be inconsistent with the Alif PCB Layout Guidelines, AAPN0027. If a discrepancy is seen between the schematic and AAPN0027, AAPN0027 takes precedence.

Revision History:

REV	DATE	Description:
A	24-MAR-2023	Initial Release, Taken from Flatboard Design
B	14-APR-2023	Added OSPI HyperRAM
		Removed Coin Cell circuit
	15-JUN-2023	Fixed swapped MIPI_CSI_C pair with MIPI_CSI_0 pair on BGA194
		Add pullup to NSRST to U21
C		Removed UART4 option on U21
		Realigned U21 GPIO assignments On P_9 and P_10 for Target JTAG connections.
	18-AUG-2023	Changed the MIPI DSI connectors to have top pins (was bottom)
		Changed nylon hardware standoff length
	07-SEP-2023	Changed C35 (VREG_AON) to 1.0uF
D	12-SEP-2023	Changed OSPI Flash and HyperRAM to 64MB devices.
		Swapped USB_DEV_ID resistor divider for 1.8V signaling
	20-SEP-2023	Fixed UART0 and UART2 swapped signals
		Changed USB power input pin
	03-OCT-2023	Added Cypress FTDI Controller, jumpers out for JLink-OB E1 (U21) with 0 ohm resistors
	09-JAN-2024	Added TP49 & TP50 to header pins
D1	25-JAN-2024	Design Review: Remove MIPI caps, GND TEST_MODE, change TP49 & TP50 to header pins
	18-APR-2024	Change VREG_AON series resistor R99 & R102 to 1K.
		Added note for VREG_DIG_1V8 for 1.8V operation

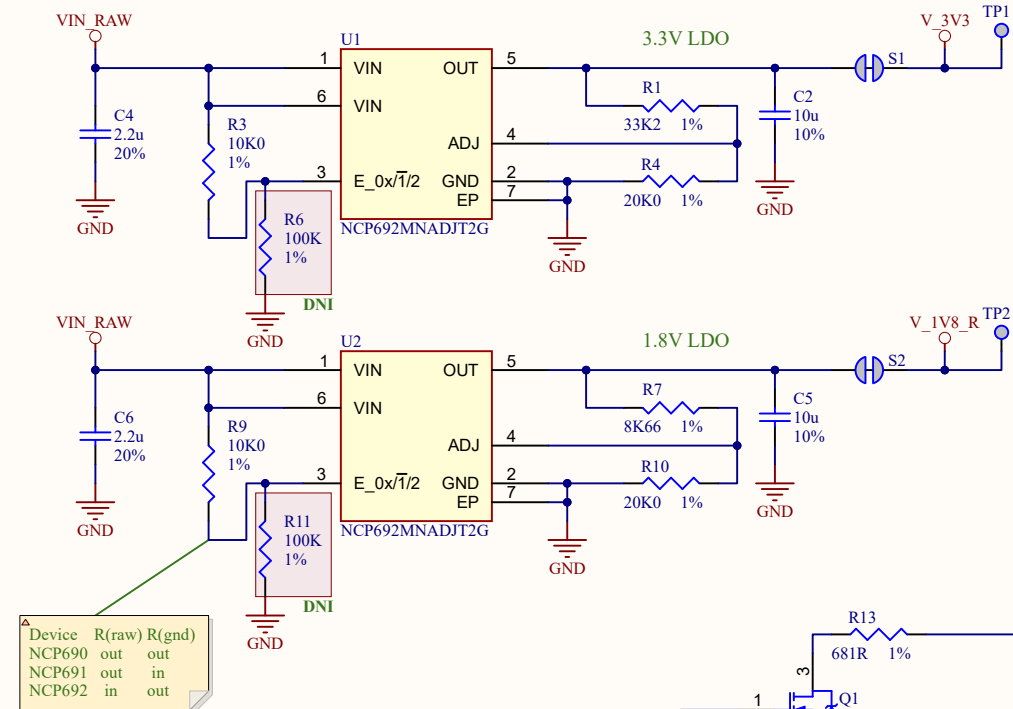
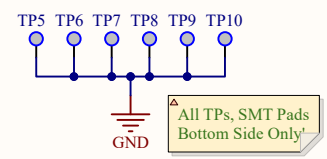
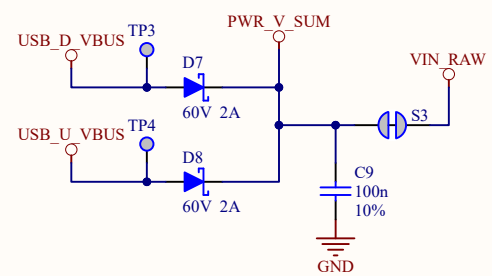
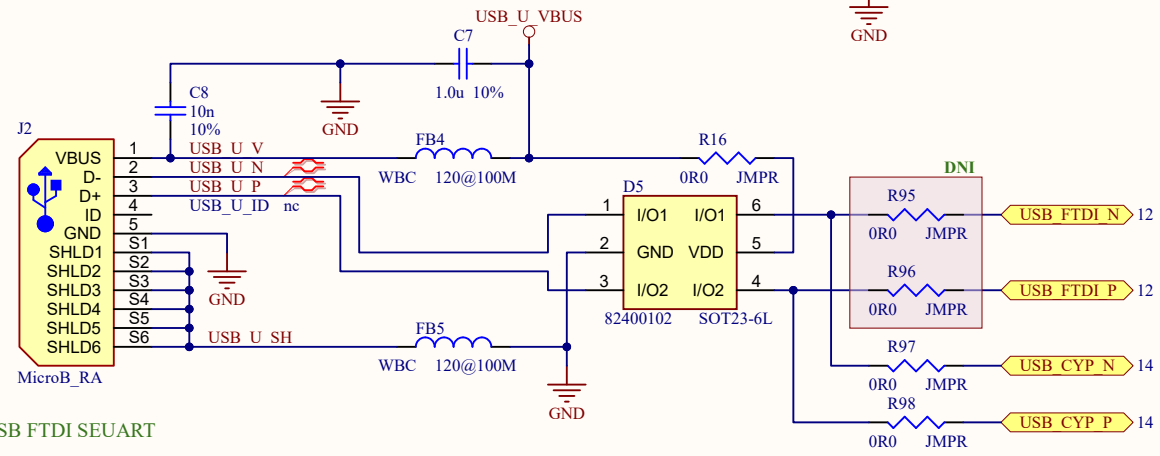
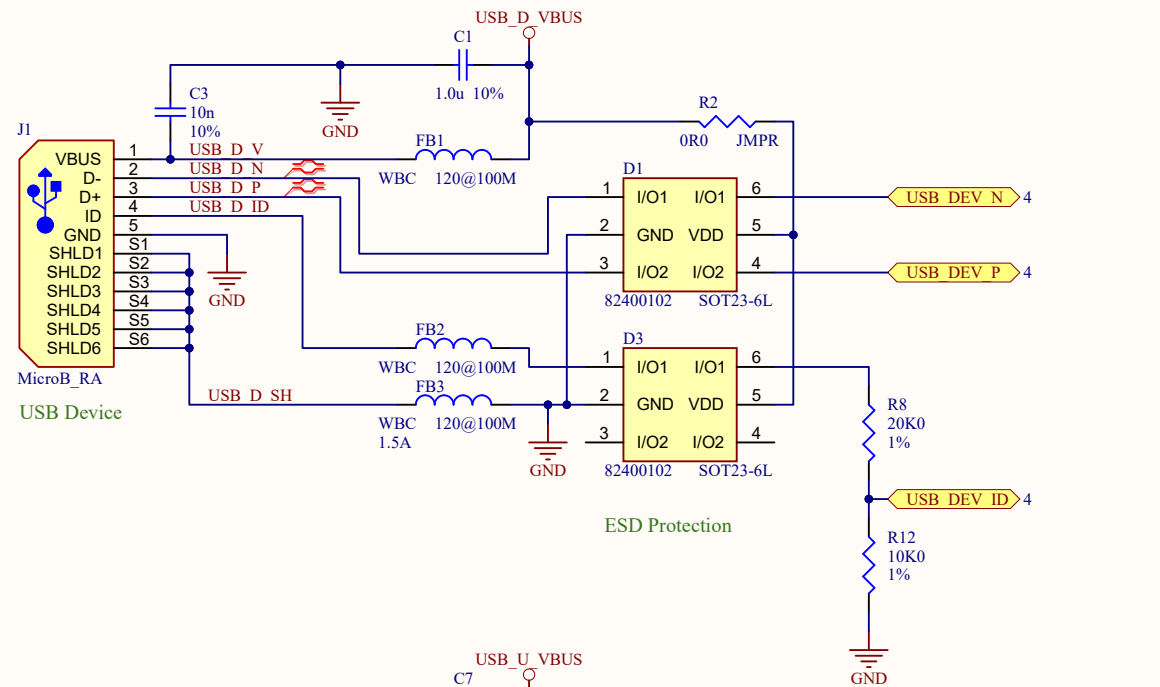
Required 2.54mm Shunts:

J3	VDD_3V3 Current Measurement
J4	VDD_1V8 Current Measurement
J5-1-2	FLEXIO = 1.8V * default
J5-2-3	FLEXIO = 3.3V
J6-1-2	WIFI in run mode * default
J6-2-3	WIFI in programming mode
J11-1-2	Camera Analog V = 2.8V
J11-2-3	Camera Analog V = 2.6V * default
J21	VDD_3V3 USB Current Measurement
SW3-A	JLink-OB E1 (and Cypress FTDI) run
SW3_B	JLink-OB E1 (and Cypress FTDI) hold-in reset
J15-1-3 & 2-4	Target SEUART * default
J15-3-5 & 4-6	Target UART2
J15-5-7 & 6-8	Target UART2
J15-7-9 & 8-10	Target UART4

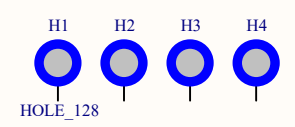
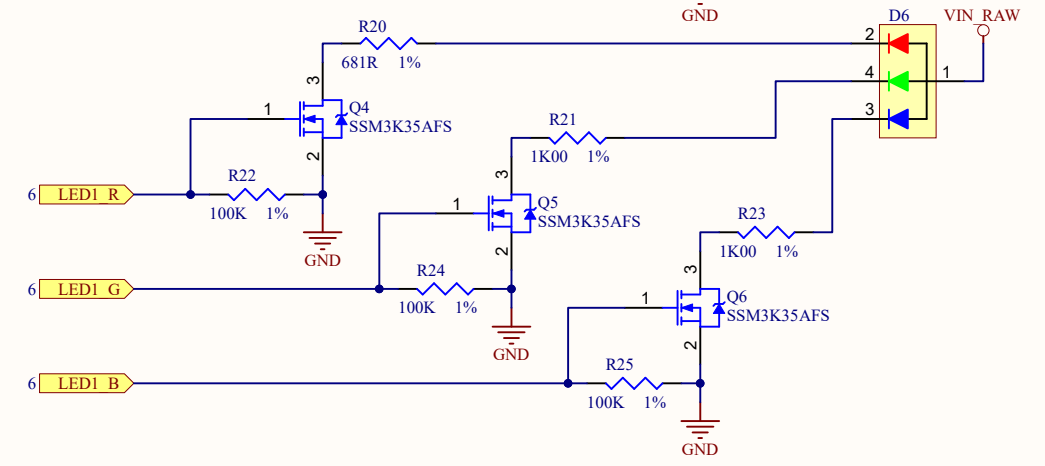
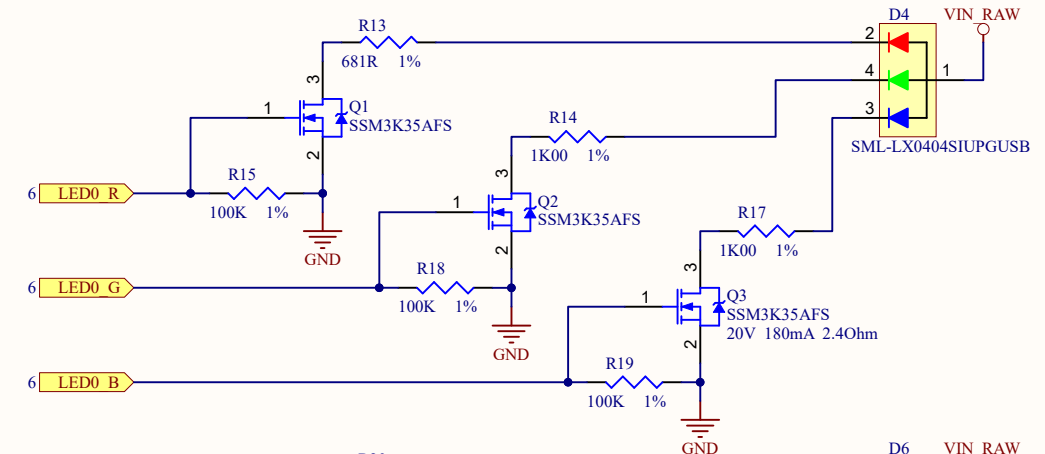
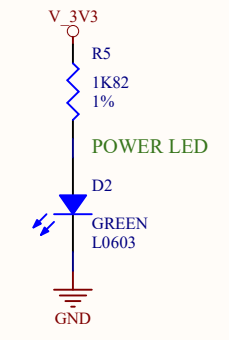


APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR	
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CHK: n/a	--/--	APP KIT BOARD		
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BOM: 250-00307		B	none	220-00307
ASSY DWG: 120-00307	FAB DWG: 210-00307	REV	D1	
PCB DWG: 110-00307-D	SCALE: none	FILE NAME	1-RevisionHistory.SchDoc	SHEET 1 OF 14

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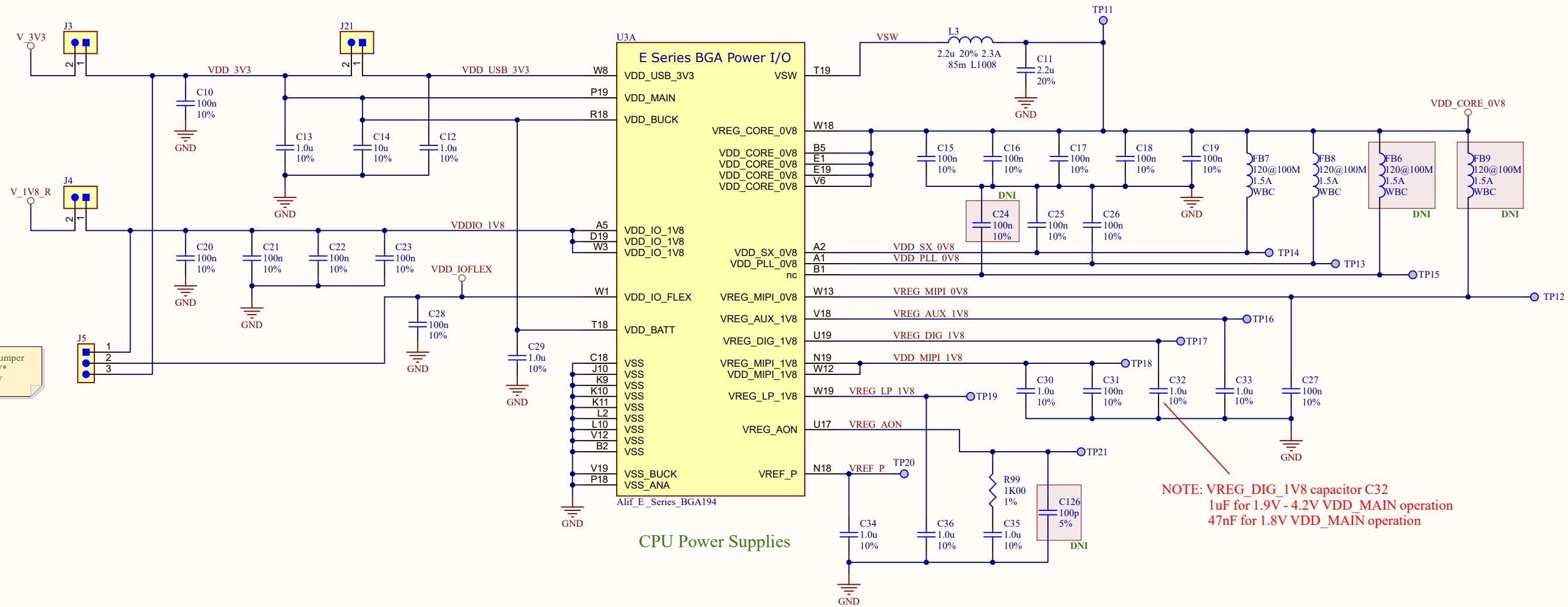


Device	R(raw)	R(gnd)
NCP690	out	out
NCP691	out	in
NCP692	in	out



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FAB DWG: 210-00307					
PCB DWG: 110-00307-D					

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A Flex I/O Jumper
1-2 = 1.8V*
2-3 = 3.3V

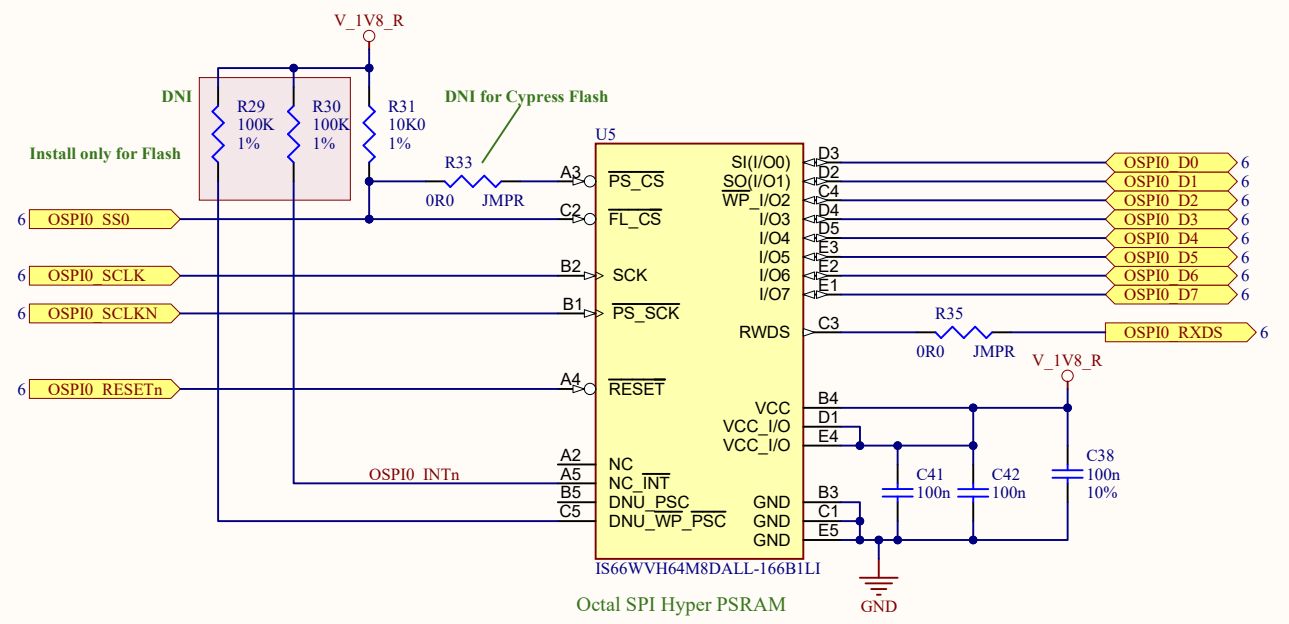
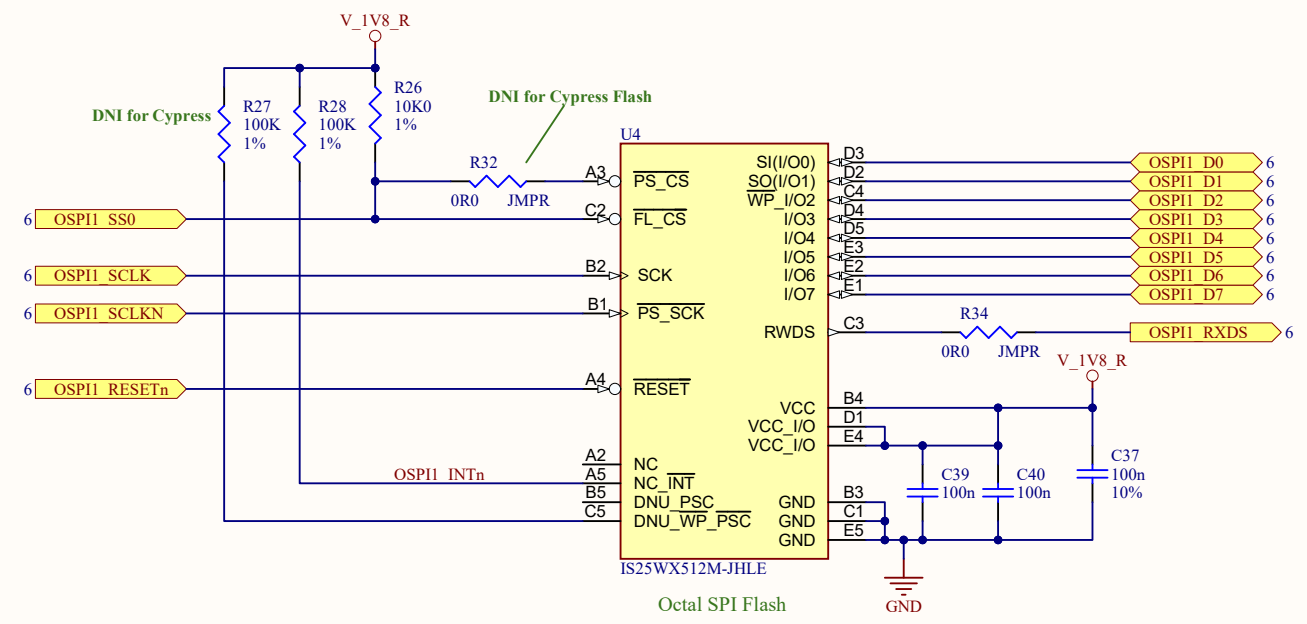
SH3 SH4 SH5 SH21
SH5 default: Pins 1-2

NOTE: VREG_DIG_1V8 capacitor C32
1uF for 1.9V - 4.2V VDD_MAIN operation
47nF for 1.8V VDD_MAIN operation

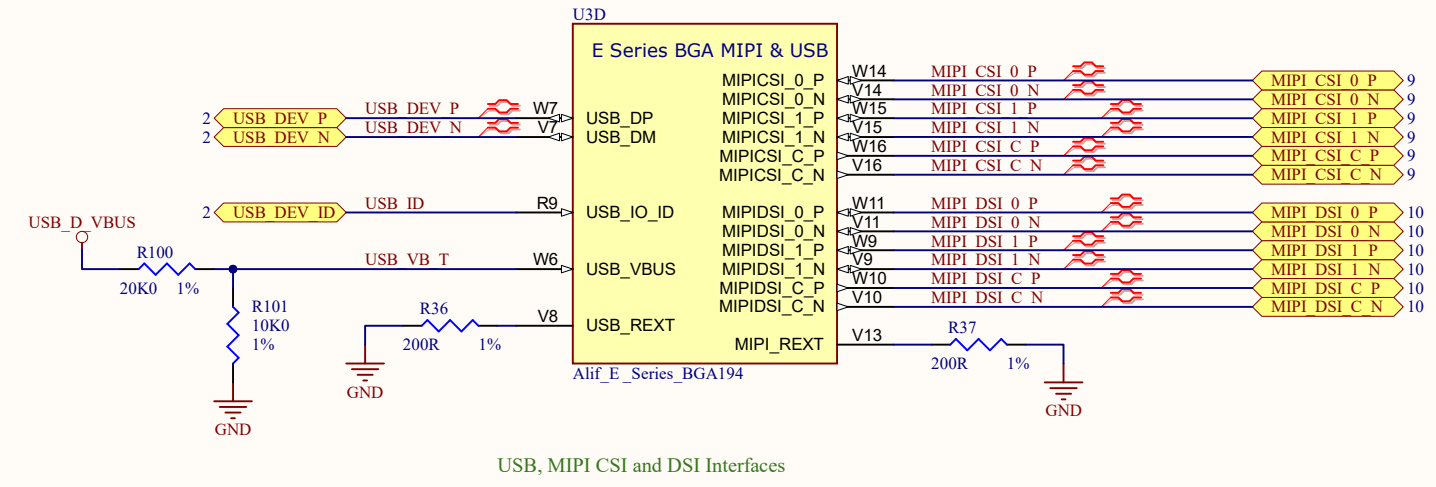
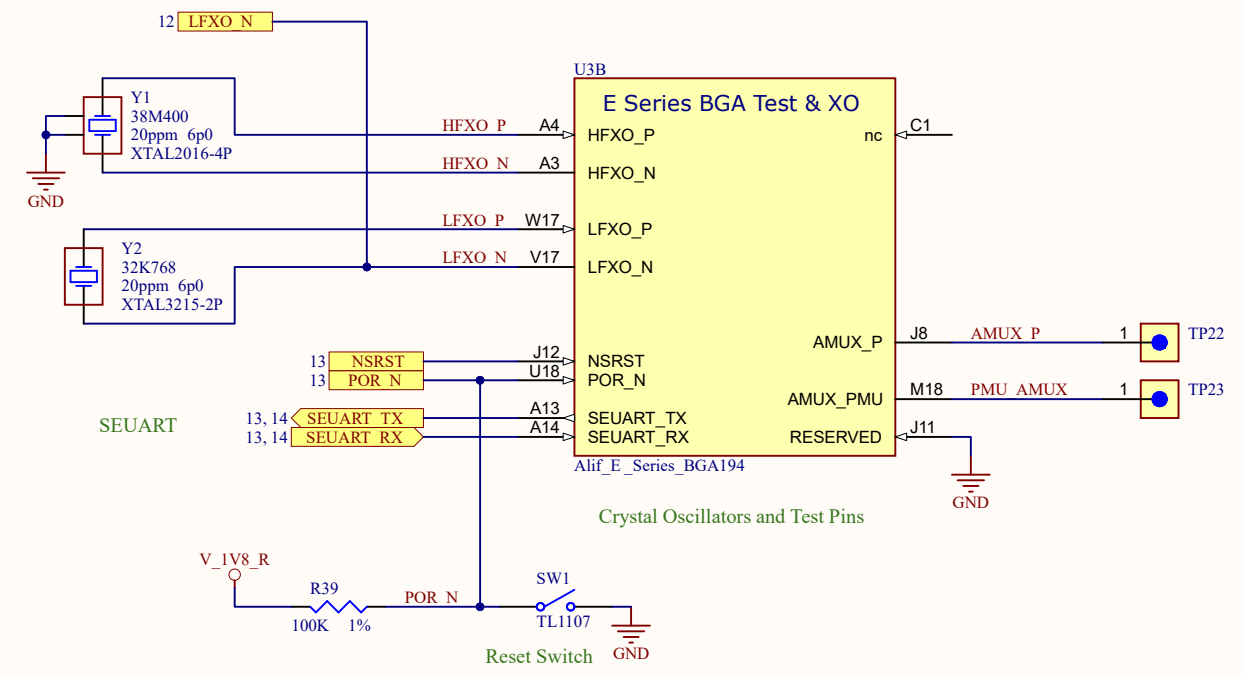
CPU Power Supplies

APPROVALS	DATE	PROJECT			Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
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CHK: n/a	--/--				
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REVISION	DESCRIPTION	DATE	APPROVED

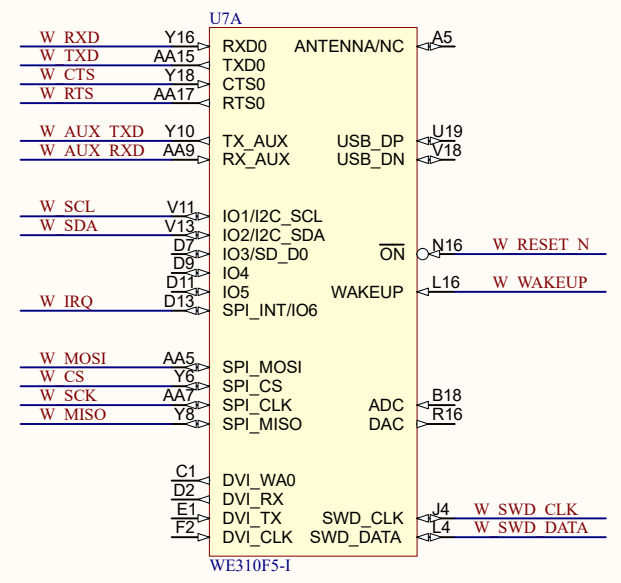
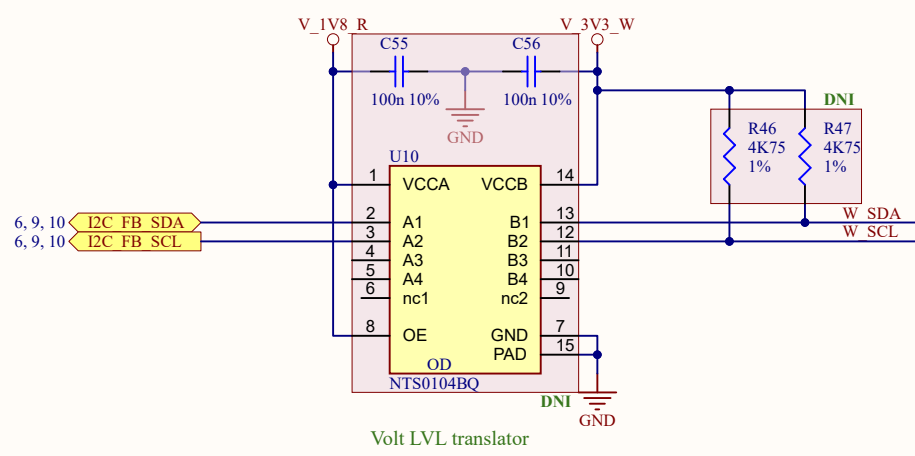
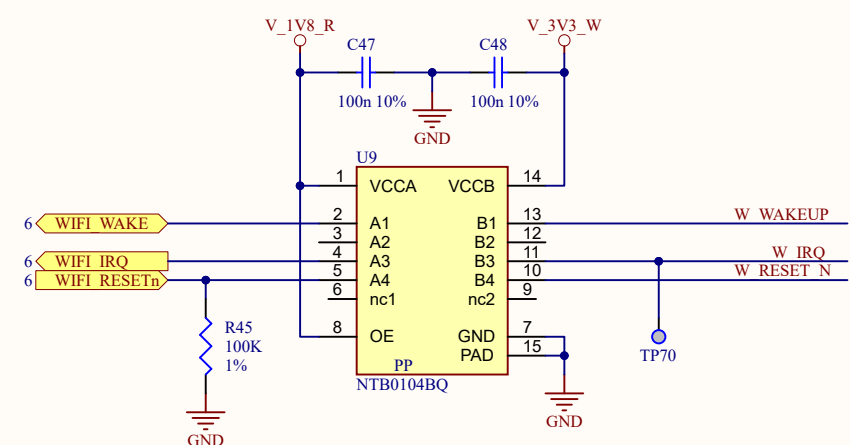
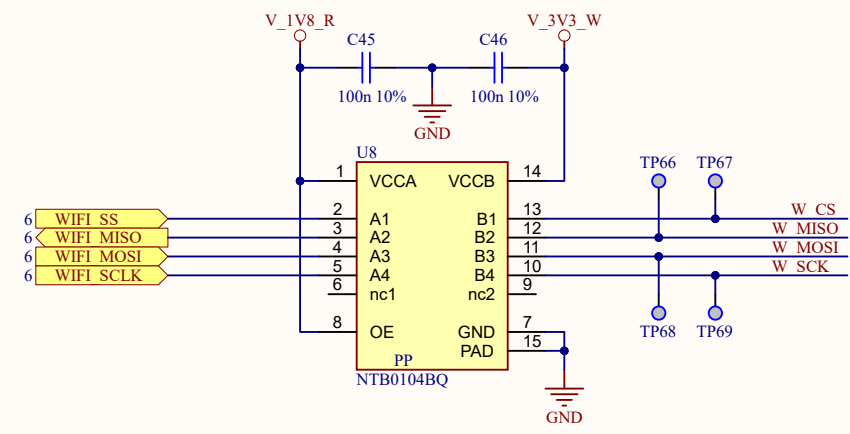
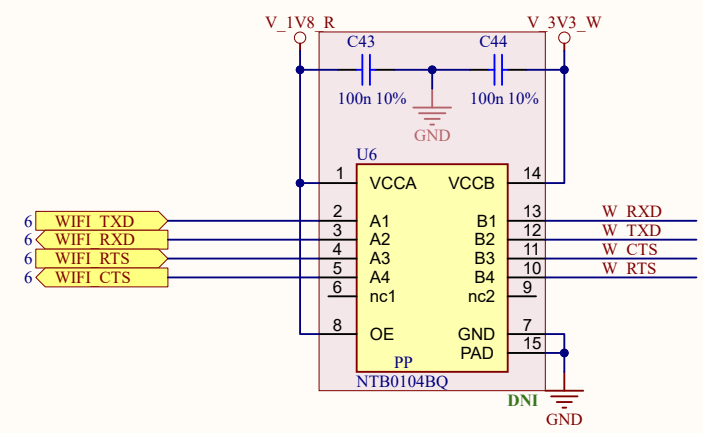


"Universal" Octal SPI Devices. Either chip can be Flash or RAM

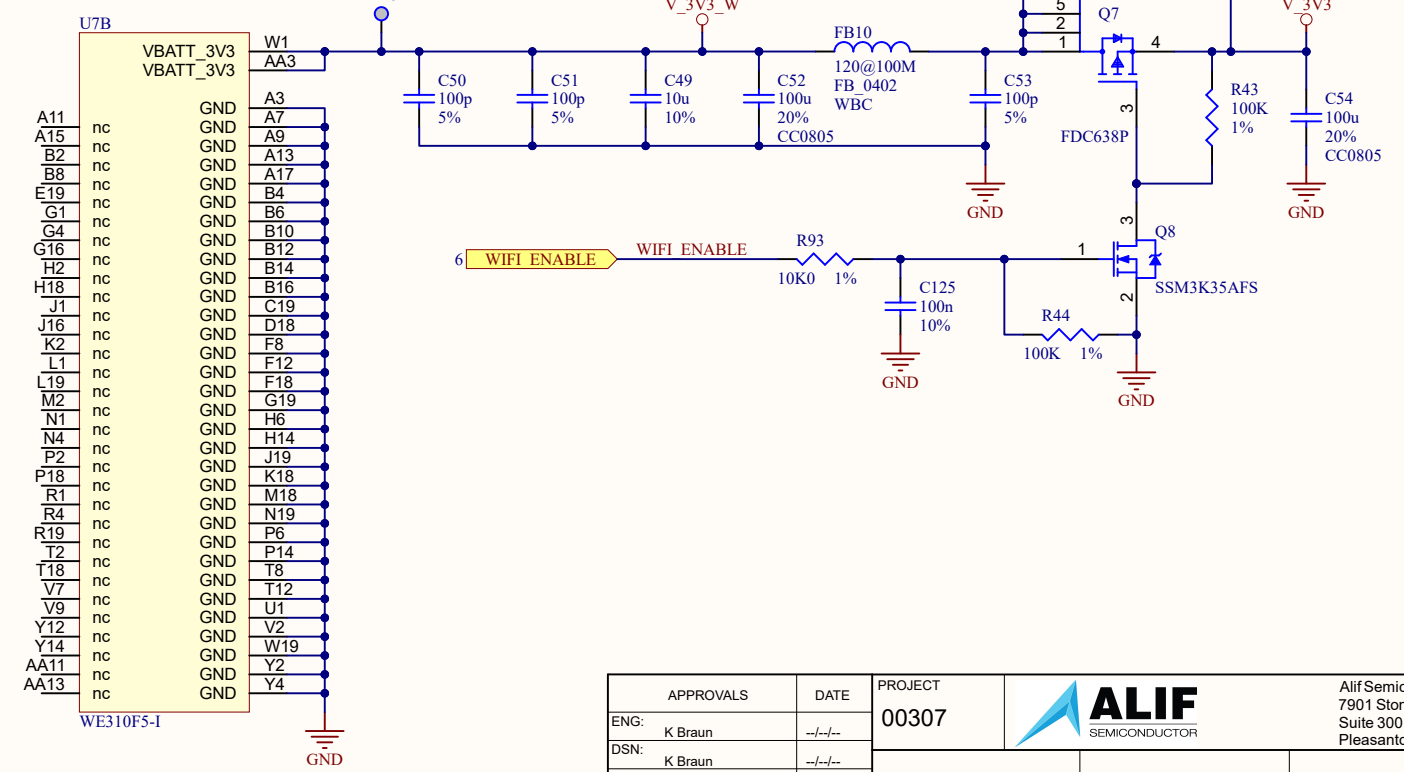
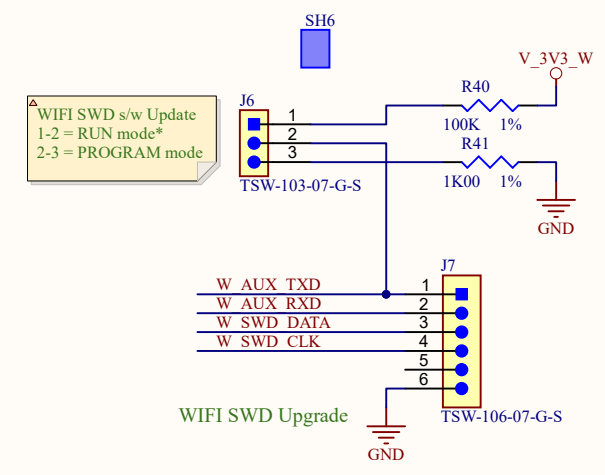


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REVISION	DESCRIPTION	DATE	APPROVED

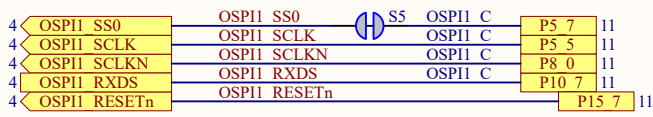
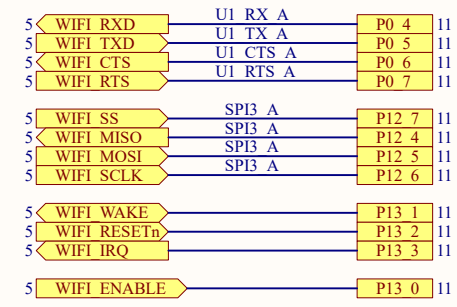
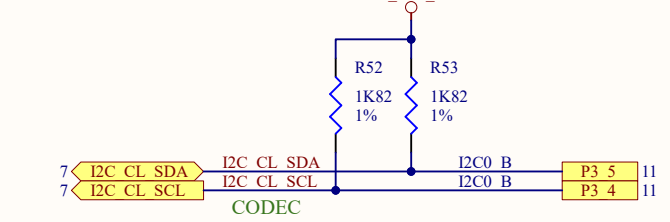
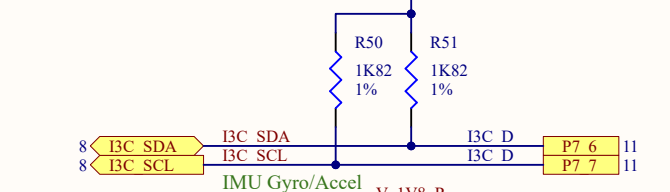
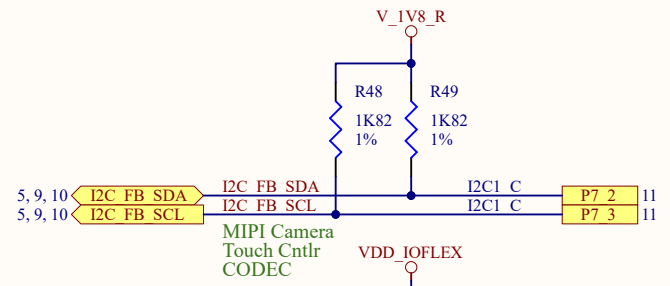


WiFi / BLE Interface

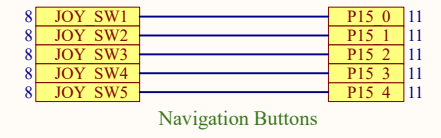
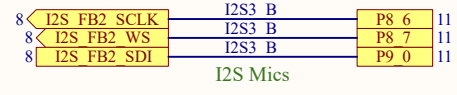
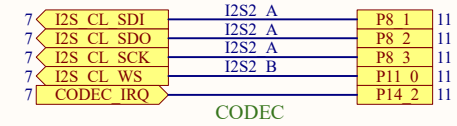


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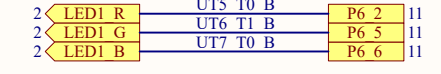
OSPI HyperRAM



Navigation Buttons



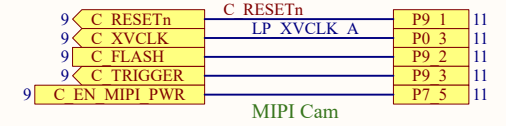
FLEXIO



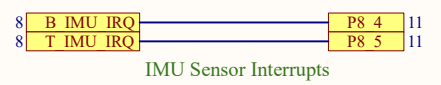
PWMable RGB LEDs



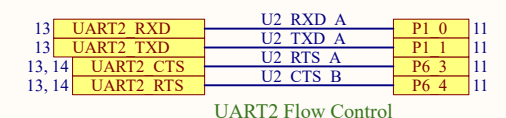
MIPI Disp Disp Bklt



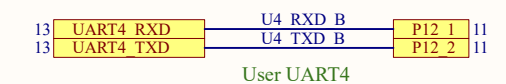
FLEXIO



IMU Sensor Interrupts



UART2 Flow Control

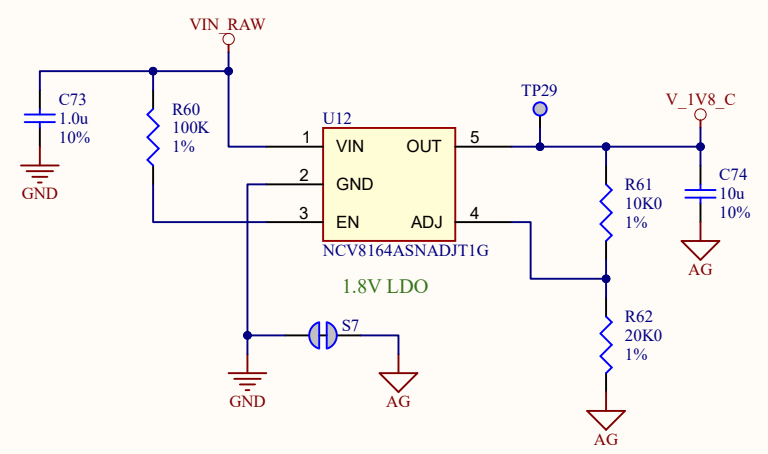
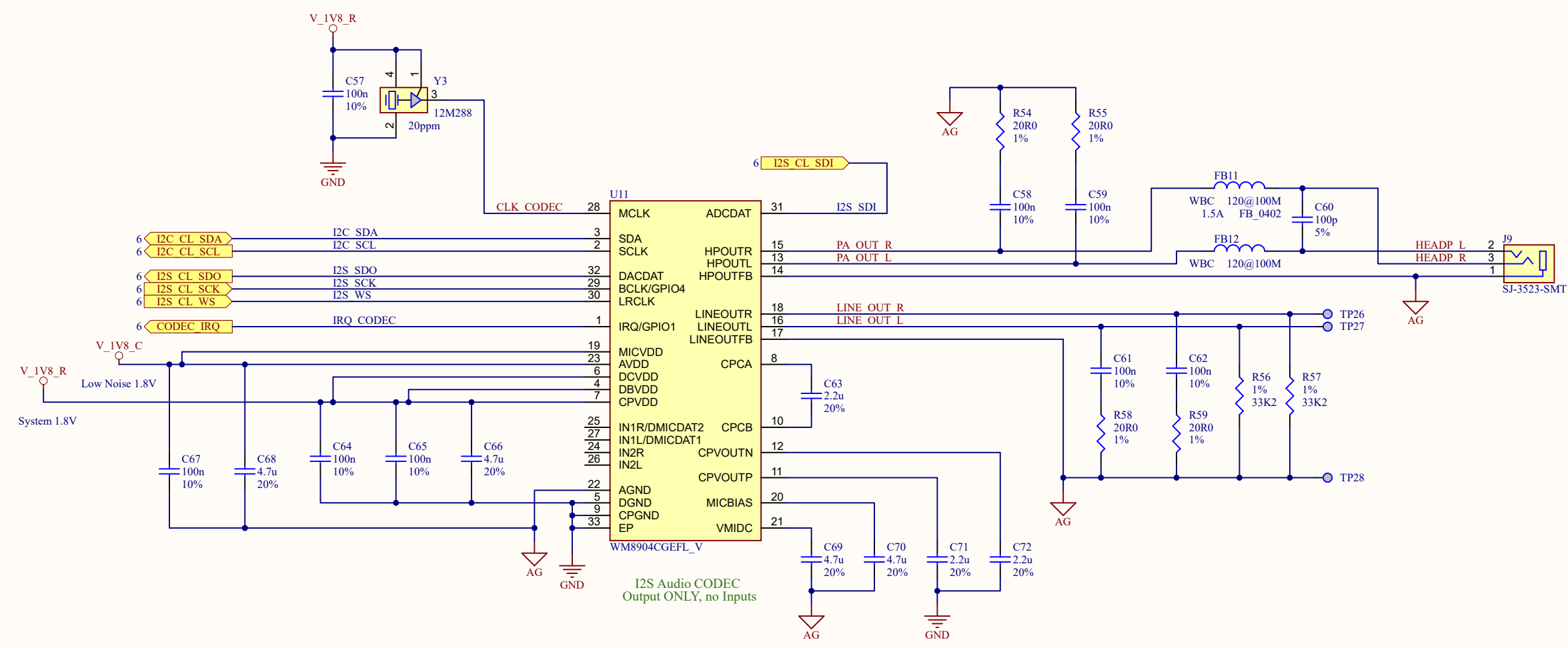


User UART4

UT6_T0_B on Flatboard -->

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DSN: K Braun	--/--		TITLE	
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PCB DWG: 110-00307-D				

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DSN: K Braun	--/--			
CHK: n/a	--/--			
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DWG NO: 220-00307
REV/SHT: D1 7

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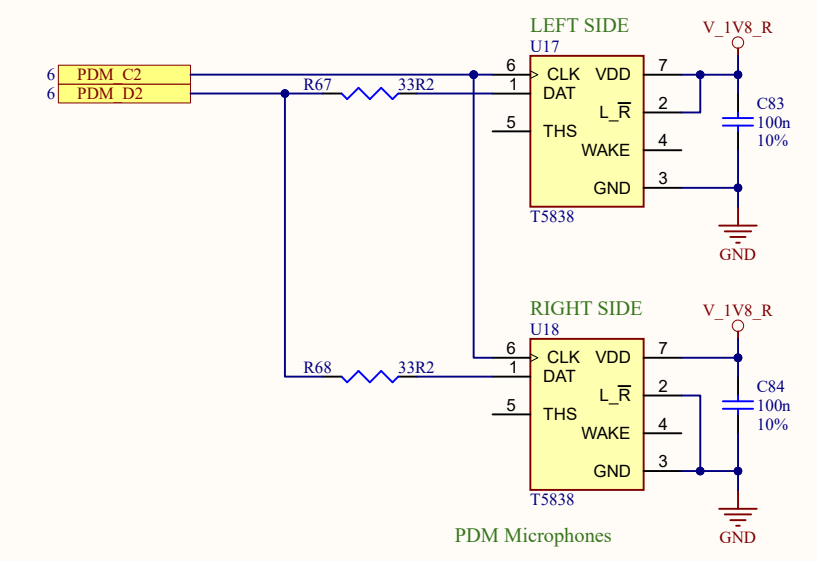
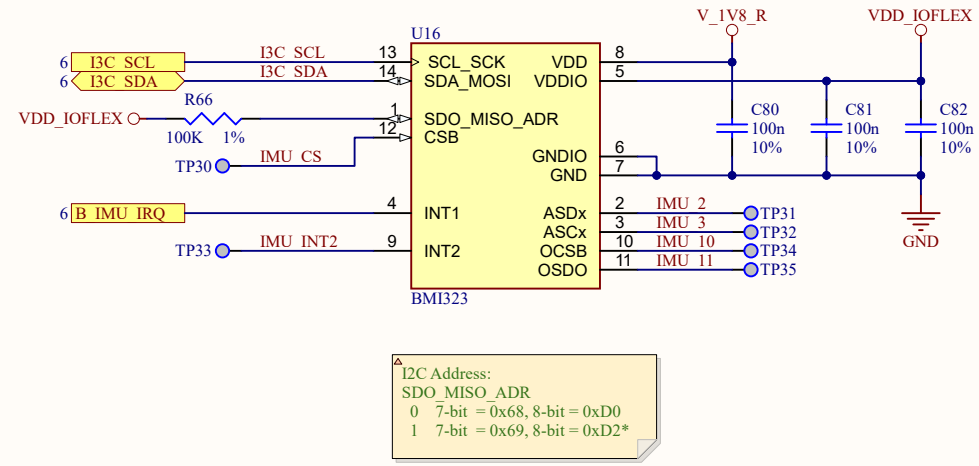
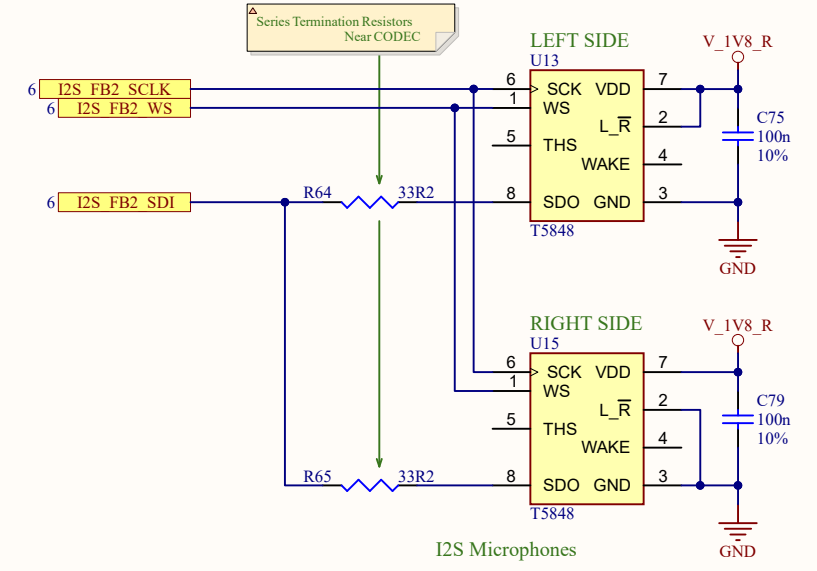
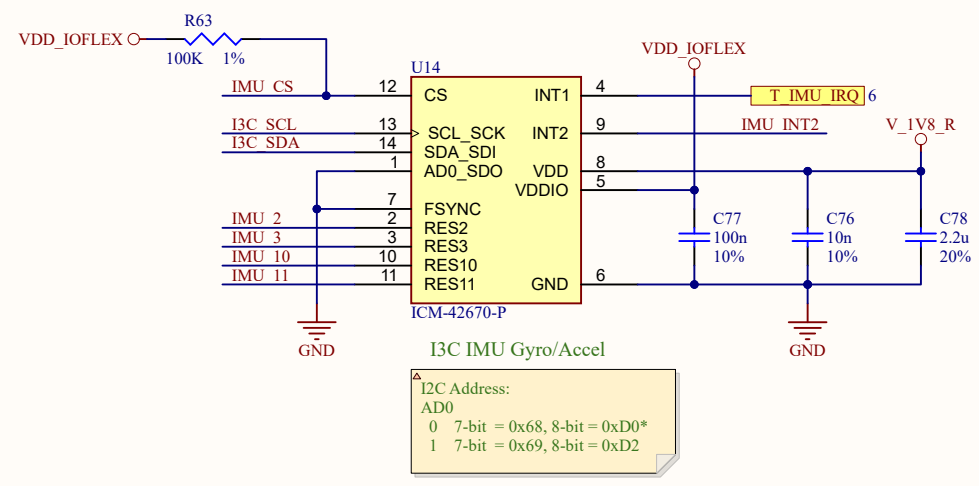
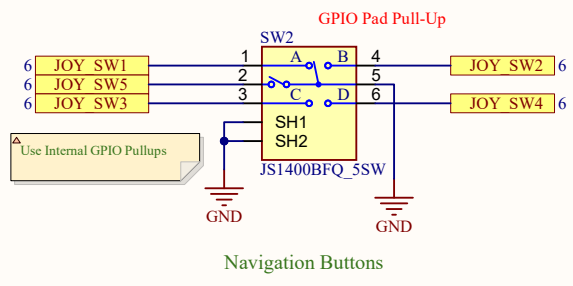
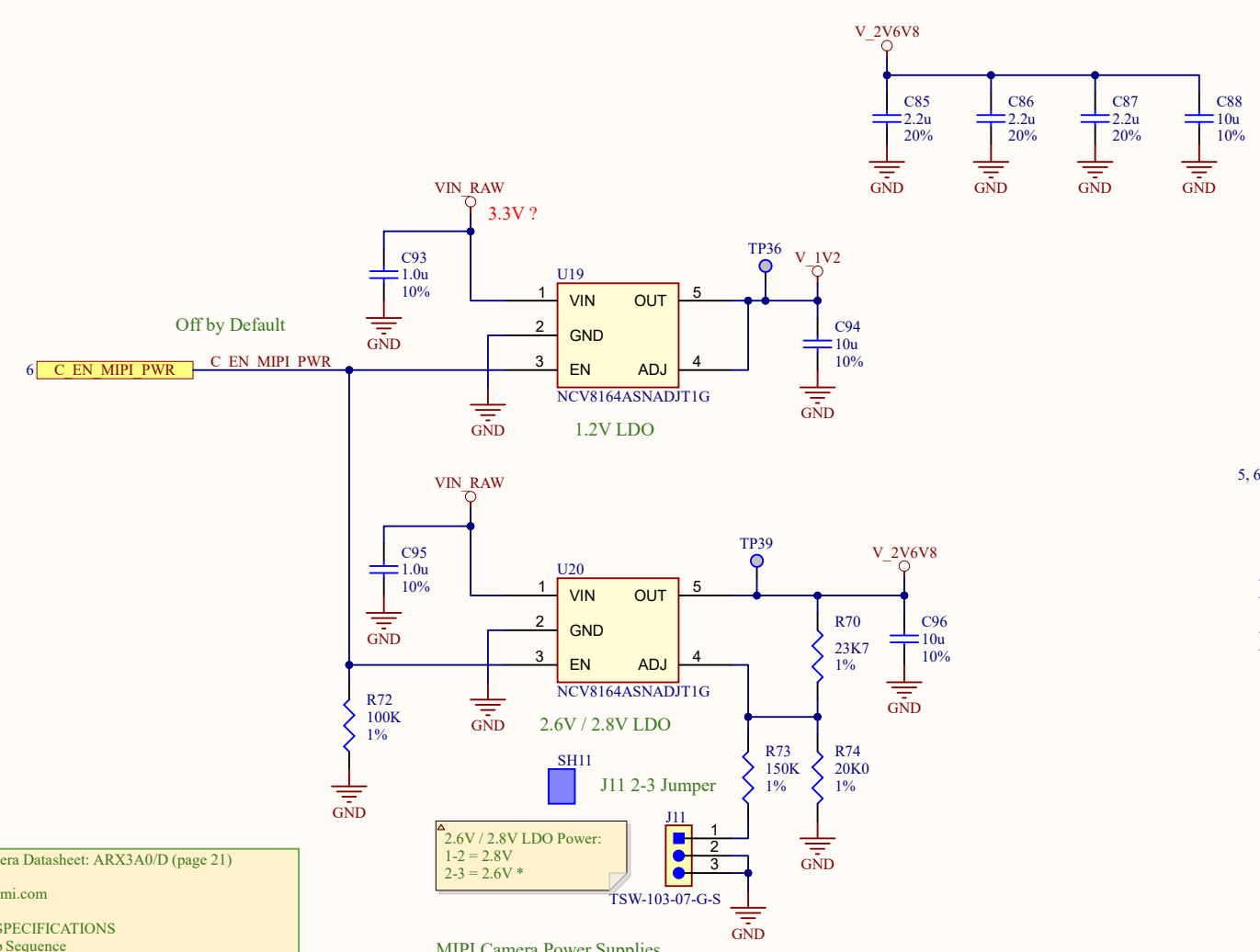


Table 29: Mapping of the secondary interface pins

Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I2C
2	ASDx	Digital I/O	Secondary Magnetometer interface	MOSI	SISO	SDA
3	ASCx	Digital I/O	Secondary Magnetometer interface	SCK	SCK	SCL
10	OCSB	Digital in	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital out	Secondary OIS interface	MISO	DNC	DNC

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ENG: K Braun	--/--	00307	
DSN: K Braun	--/--		
CHK: n/a	--/--		
REFERENCE DOCUMENTS			TITLE
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FAB DWG: 210-00307	B	none	220-00307
PCB DWG: 110-00307-D	SCALE: none	FILE NAME	REV
		8-Sensors.SchDoc	D1
	SHEET 8	OF 14	

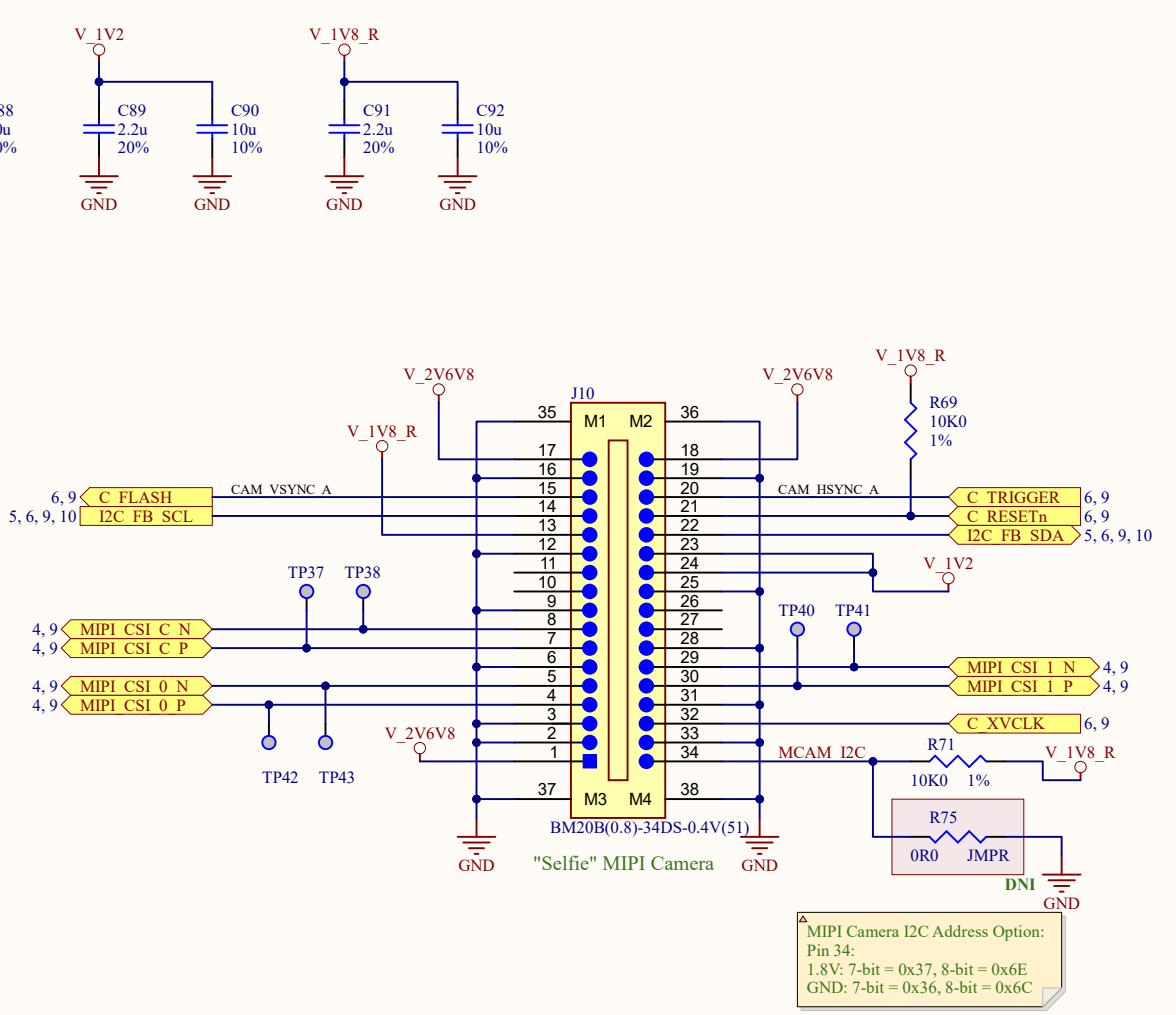
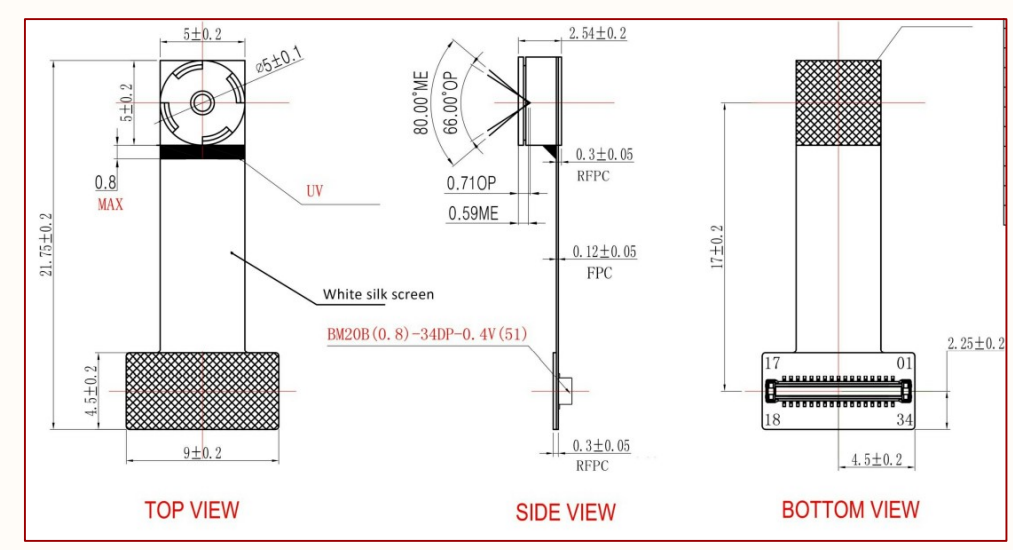


MIPI Camera Datasheet: ARX3A0/D (page 21)
 www.onsemi.com

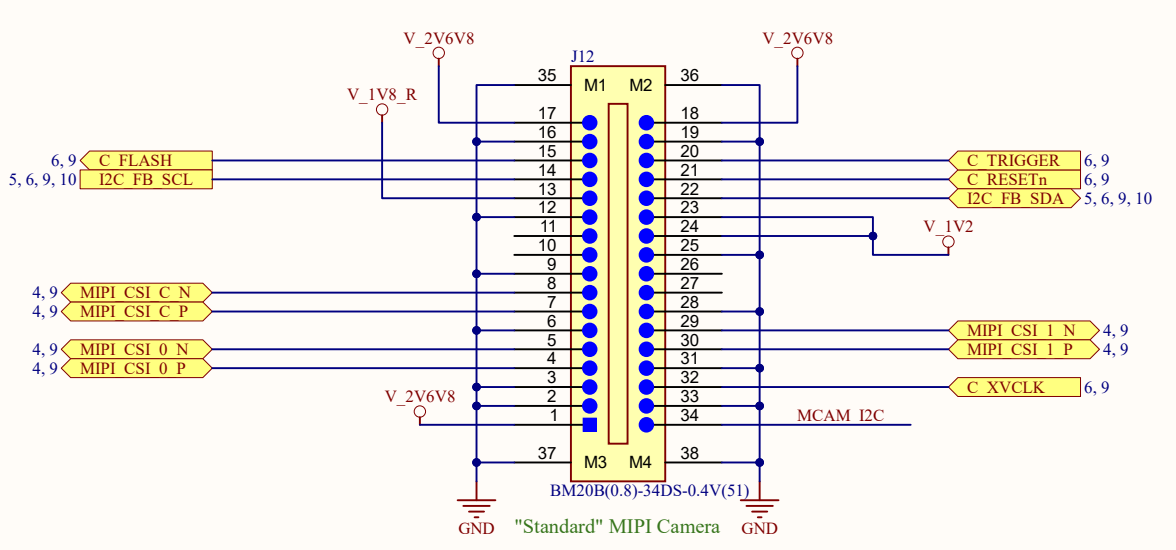
TIMING SPECIFICATIONS
 Power-Up Sequence
 The recommended power-up sequence for ARX3A0 is shown in Figure 21. The available power supplies must have the separation specified below.

1. Set XSHUTDOWN LOW.
2. Power up VDD_IO (1.8 V only)
3. After 1-500 ms, power up VDD, VDD_ANA, VDD_PLL, VDD_PHY (1.2 V) and VAA, VAA_PIX (2.7 V) (any order).
4. Apply EXTCLK (can be applied anytime).
5. After 1-500 ms, set XSHUTDOWN.
6. HOST configuration through I2C (PLL, output, etc).
7. Set stream = 1 (R0x301A[2]).
8. PLL internally enables and locks.
9. ARX3A0 enters streaming mode.

MIPI Camera Power Supplies

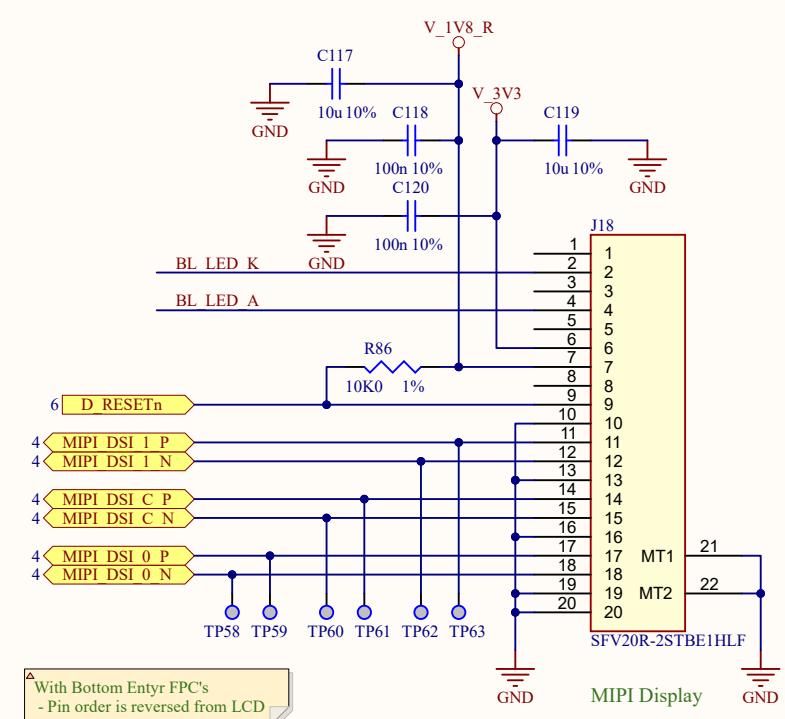


MIPI Camera I2C Address Option:
 Pin 34:
 1.8V: 7-bit = 0x37, 8-bit = 0x6E
 GND: 7-bit = 0x36, 8-bit = 0x6C

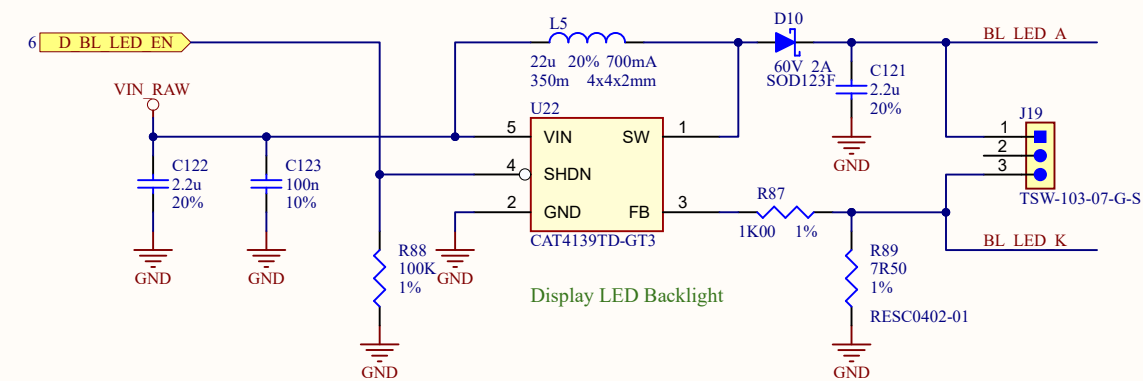


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ENG: K Braun	--/--	00307		
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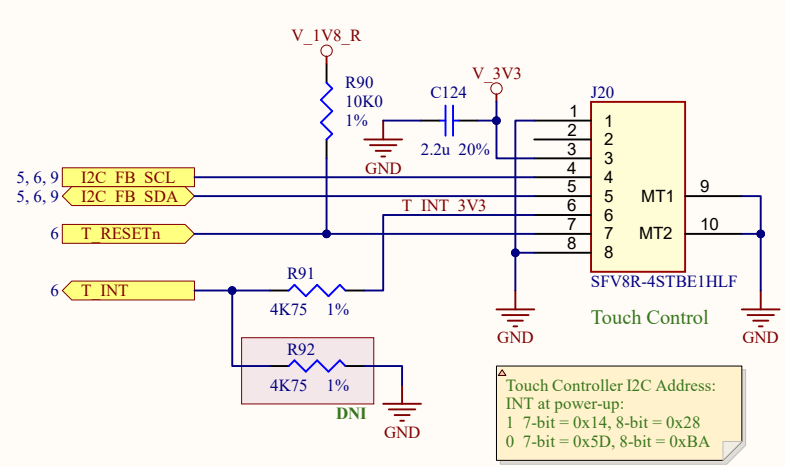
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^A With Bottom Entry FPC's
- Pin order is reversed from LCD



Display LED Backlight

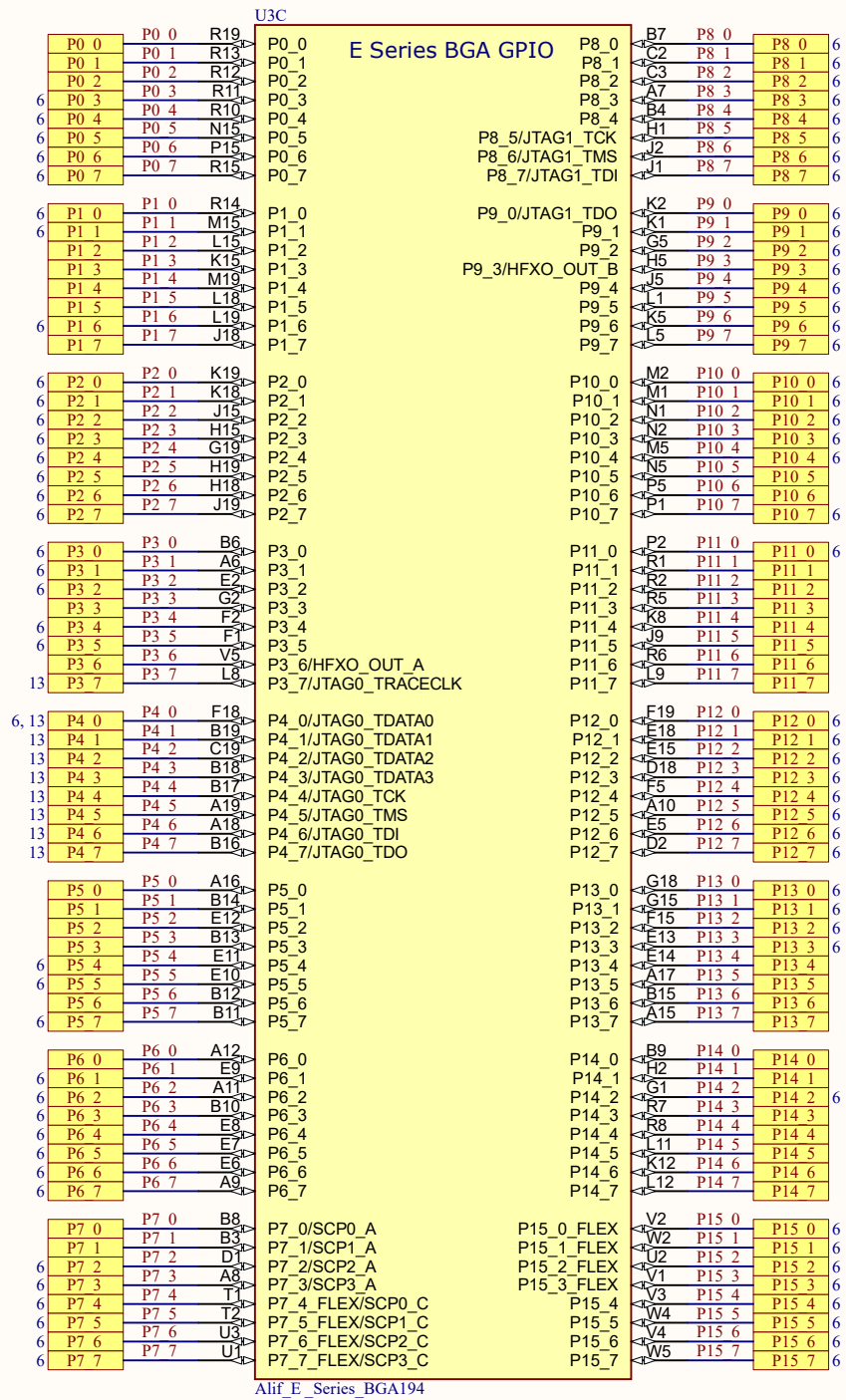


^A Touch Controller I2C Address:
INT at power-up:
1 7-bit = 0x14, 8-bit = 0x28
0 7-bit = 0x5D, 8-bit = 0xBA

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DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00307		APP KIT BOARD			
ASSY DWG: 120-00307		SIZE	CAGE CODE	DWG NO.	REV
FAB DWG: 210-00307		B	none	220-00307	D1
PCB DWG: 110-00307-D		SCALE: none	FILE NAME	10-MIPI DSI.SchDoc	SHEET 10 OF 14

DWG. NO. 220-00307
REV. SMT D1 10

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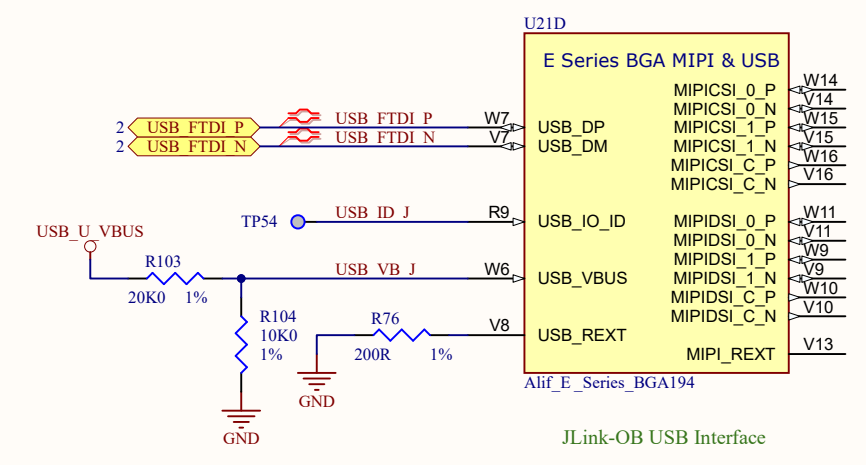
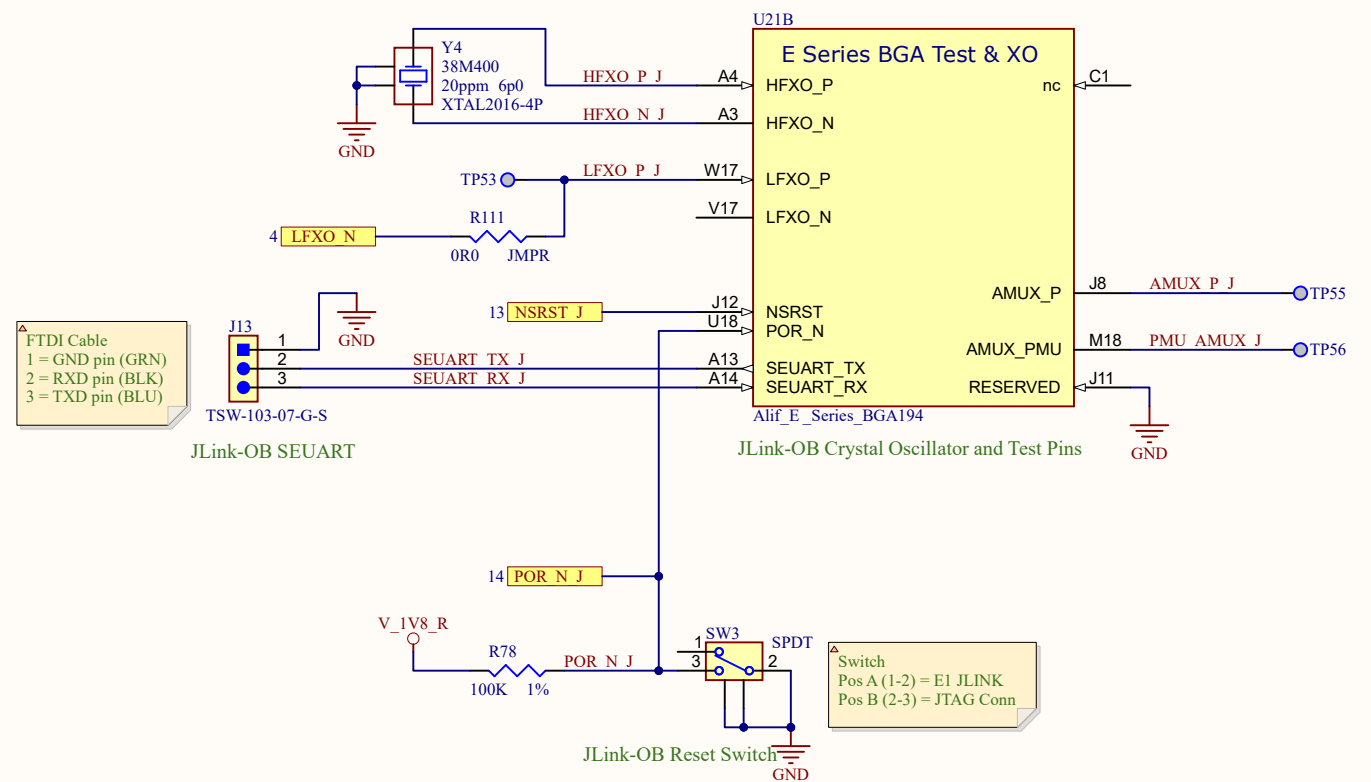
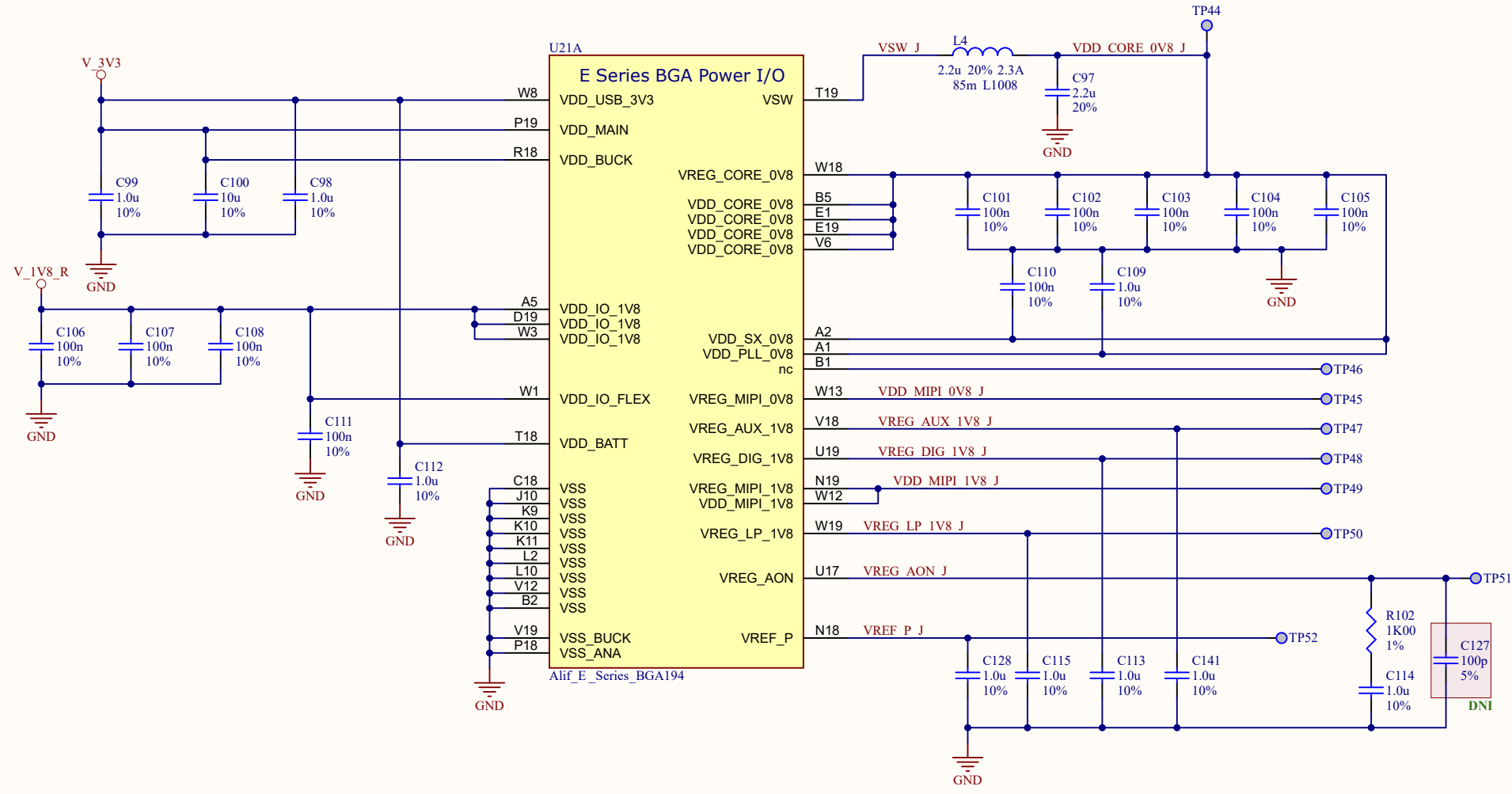


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FAB DWG: 210-00307	SCALE: none	FILE NAME: 11-CPU_GPIO.SchDoc	REV: D1
PCB DWG: 110-00307-D	SHEET 11 OF 14		

DWG NO. 220-00307
REV/SHT D1 11

REVISION	DESCRIPTION	DATE	APPROVED

JLink-OB E1 CPU Power Supplies



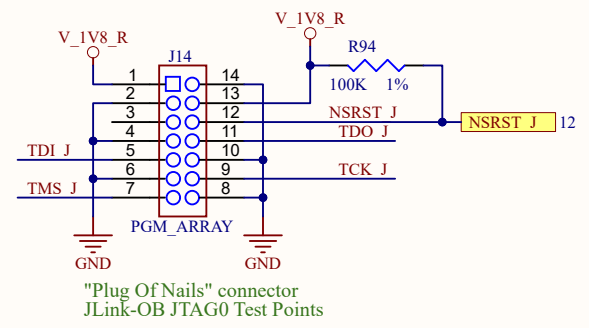
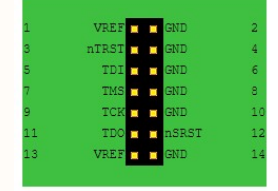
FTDI Cable
1 = GND pin (GRN)
2 = RXD pin (BLK)
3 = TXD pin (BLU)

Switch
Pos A (1-2) = E1 JLINK
Pos B (2-3) = JTAG Conn

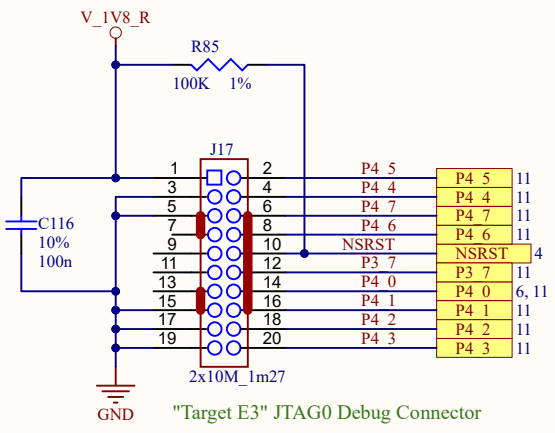
APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00307			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00307	APP KIT BOARD				
ASSY DWG: 120-00307	SIZE: B	CAGE CODE: none	DWG NO: 220-00307	REV: D1	
FAB DWG: 210-00307	SCALE: none	FILE NAME: 12-JLINK_1.SchDoc	SHEET: 12 OF 14		
PCB DWG: 110-00307-D					

REVISION	DESCRIPTION	DATE	APPROVED

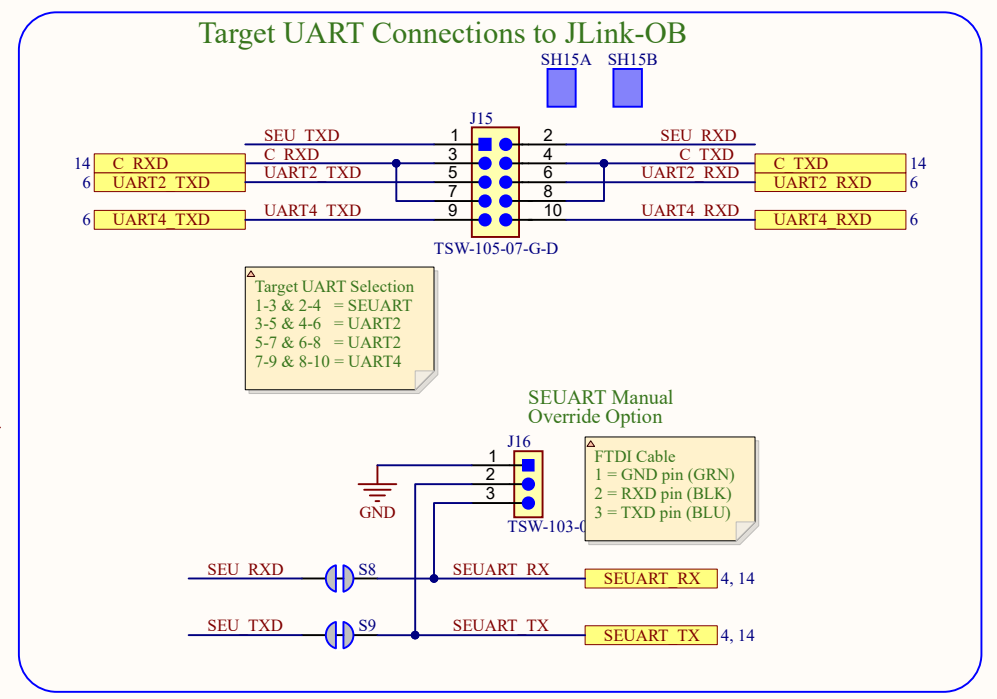
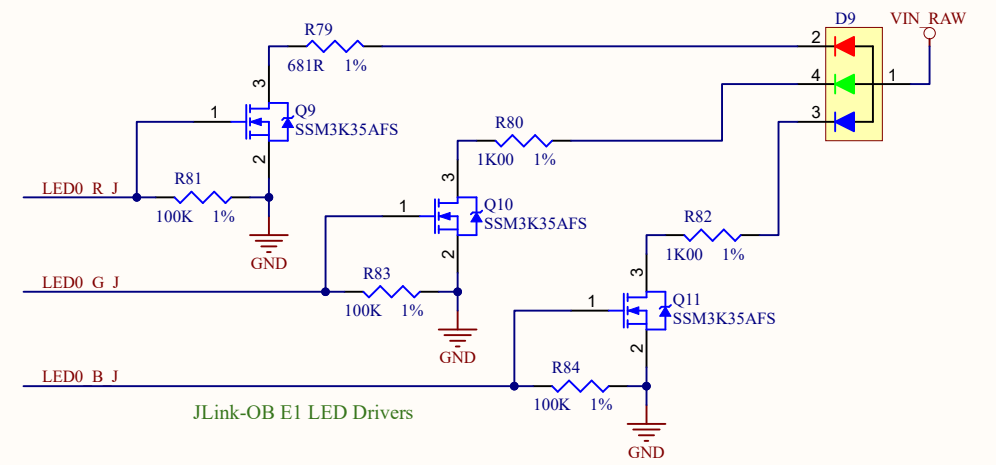
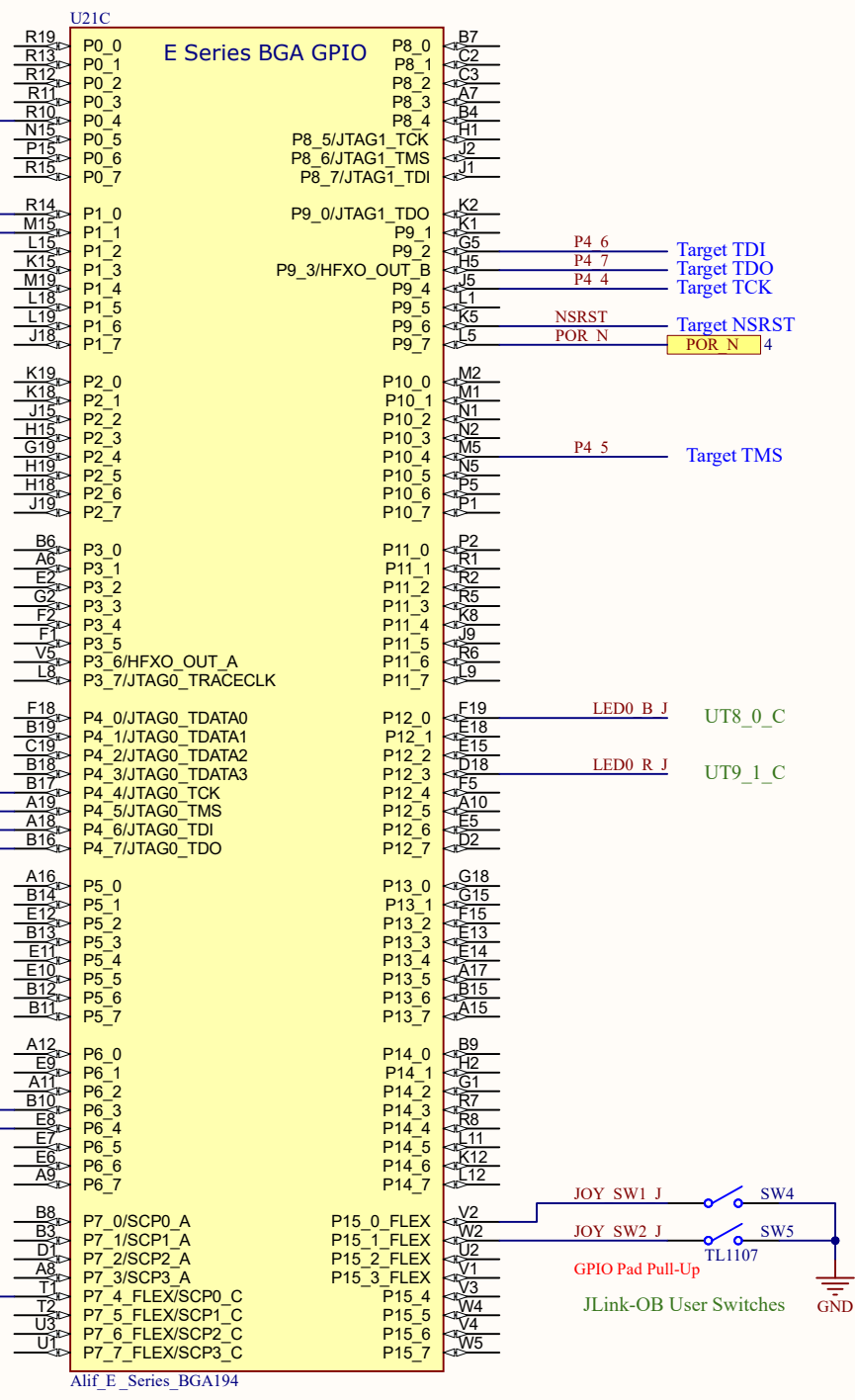
ARM14 JTAG header pinout



A <- JTAG1_TRST (nc)
<- JTAG1_TCK
>- JTAG0_NSRRST
>- JTAG1_TDI
<- JTAG1_TDO
>- JTAG1_TMS



A JTAG0_TRST (no need)
JTAG0_TMS
JTAG0_TCK
JTAG0_TDO
JTAG0_TDI
JTAG0_NSRRST
JTAG0_TRACECLK
JTAG0_TDATA0
JTAG0_TDATA1
JTAG0_TDATA2
JTAG0_TDATA3



APPROVALS	DATE	PROJECT	ALIF SEMICONDUCTOR		Alif Semiconductor 7901 Stoneridge Drive Suite 300 Pleasanton, CA 94588 USA
ENG: K Braun	--/--	00307			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00307	APP KIT BOARD				
ASSY DWG: 120-00307	SIZE: B	CAGE CODE: none	DWG NO.: 220-00307	REV: D1	
FAB DWG: 210-00307	SCALE: none	FILE NAME: 13-JLINK_2.SchDoc	SHEET: 13	OF: 14	
PCB DWG: 110-00307-D					

REVISION	DESCRIPTION	DATE	APPROVED

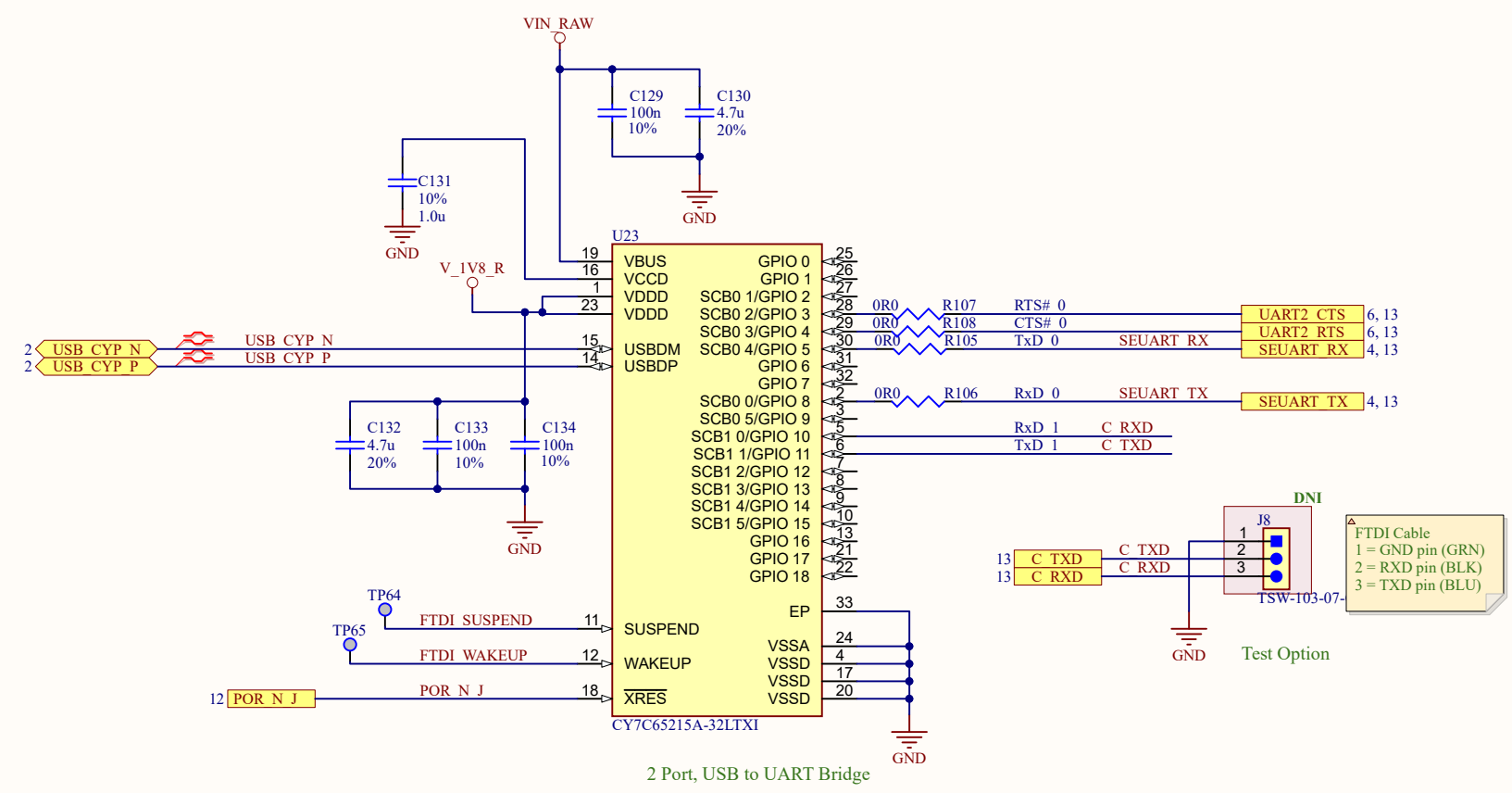


Table 17. Serial Communication Block (SCB1) Configuration

Pin	Serial Port 1	Mode 0*	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
5	SCB1_0	RxD_1	RxD_1	RxD_1	MISO_IN_1	MISO_OUT_1	SCL_OUT_1	SCL_IN_1	TDO
6	SCB1_1	TxD_1	TxD_1	TxD_1	MOSI_OUT_1	MOSI_IN_1	SDA_1	SDA_1	TDI
7	SCB1_2	RTS#_1	RTS#_1	GPIO_12	SSEL_OUT_1	SSEL_IN_1	GPIO_12	GPIO_12	TMS
8	SCB1_3	CTS#_1	CTS#_1	GPIO_13	SCLK_OUT_1	SCLK_IN_1	GPIO_13	GPIO_13	TCK
9	SCB1_4	DSR#_1	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	TRST#
10	SCB1_5	DTR#_1	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15

*Note: Device configured in Mode 0 as default. Other modes can be configured via Cypress-supplied configuration utility.

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ENG: K Braun	--/--	00307			
DSN: K Braun	--/--				
CHK: n/a	--/--				
REFERENCE DOCUMENTS		TITLE			
BOM: 250-00307		APP KIT BOARD			
ASSY DWG: 120-00307	SIZE: B	CAGE CODE: none	DWG NO.: 220-00307	REV: D1	
FAB DWG: 210-00307	SCALE: none	FILE NAME: 14-CypressSEUART.SchDoc	SHEET: 14	OF: 14	
PCB DWG: 110-00307-D					

DWG. NO. 220-00307
REV. SHT D1 14